Δ-Source Impedance Network

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***Abstract*—Impedance networks have been already investigated in various literature with the main goals of increasing the attainable voltage gain and reducing the components number. Recently, coupled inductors found popularity because they let converters with lower weight and cost. It seems that coupled inductances are a proper answer to the increasing voltage gain while keeping down the components number. This paper proposes a novel impedance network circuit based on three coupled inductors with a Δ connection. The proposed Δ-source converter offers smaller magnetizing current and winding losses compared to the successful Y-source circuit. Moreover, with the Δ-connected three coupled inductors, the adverse effect of leakage inductance on the converter performance is significantly reduced. The effectiveness of the proposed structure is analytically proved. The theoretical achievements over the conventional Y-source structure are confirmed through extensive simulations and experiments.**

***Index Terms*—Coupled inductors, dc–dc converter, leakage inductance, Z-source (ZS) network.**

I. Introduction

In THE last two decades, power electronic converters with enhanced voltage boosting ability to generate a much higher voltage from the available source have received extensive research attentions for many fields of applications, such as integrating the renewable energy sources to the grid. The introduction of Z-source (ZS) impedance networks in the early last decade [1] was a considerable advancement in voltage boosting ability of variety of converters, such as dc/dc, ac/dc, dc/ac, and ac/ac, especially for integrating the renewable energy sources to the grid [2]–[6]. Traditionally where the voltage generated by the renewable source must be boosted to the grid voltage level, an extra dc–dc converter is inevitable, which means complexity and increased cost and volume while adoption of the impedance network to these applications adds the simultaneous buck and boost ability to a single stage power converter. Many research works focused on alternative structures in order to improve the characteristics of the ZS-integrated converters [7], [8] while many papers investigated the possible modulation strategies and modeling and control algorithms [9], [10]. In addition, recent literature have focused on further applications of impedance networks in off grid inverters [11]–[13]. Also, the reliability of impedance networks is well investigated and explained in [14] and it is worthy to mention that the switching overlap is permissible for impedance network converters; thus, the immunity and reliability of converter to electromagnetic interference and wrong switching states increase significantly. Although ZS converter introduces many merits, some obstacles limit its applications. For example, to increase the output voltage, the duty cycle of the shoot-through (ST) state must be increased; as a result, the voltage stress on the switches of the converter increases. In addition, the output voltage waveforms deteriorate.

To address these problems, more advanced impedance networks, such as the SL impedance network [15] and the Switched Inductor Quasi Z-source (SL-QZS) impedance network [16] are recently introduced. These topologies can boost the voltage with a lower ST duty ratio; however, they need more components, so the efficiency reduces and the cost and volume increase. Use of coupled magnetics is an alternative solution to overcome the limited voltage gain of traditional impedance network converters, which offers very high voltage gains and high power densities with a reduced number of passive components. The most successful examples are T-source [17], trans ZS [18], Γ-source [19], flipped Γ-source [20], and Σ-source [21] impedance networks. Also the improved structures of some of these coupled inductor based networks have been proposed, which leads to some beneficial characteristics such as continuous input current at the price of more components [22], [23]. All these networks are based on two winding coupled inductors. A common advantage among all these converters is that high voltage gains are possible with higher modulation indexes, which means lower ST duty cycles. Thus, it is expected that the switches experience lower voltage stresses than the conventional impedance network converters. As a more advanced solution, the Y-source impedance network uses three coupled inductors in its structure [24], [25]. The main additional advantage of the Y-source network over other magnetically coupled topologies is the wide range of design choices for a specific voltage gain, which makes this network versatile by offering flexibility to meet different performance and design requirements.

Based on principles inspired from the successful Y-source structure, this paper proposes a more advanced impedance network with three coupled inductors in its structure, called Δ-source. With the same number of component, the proposed

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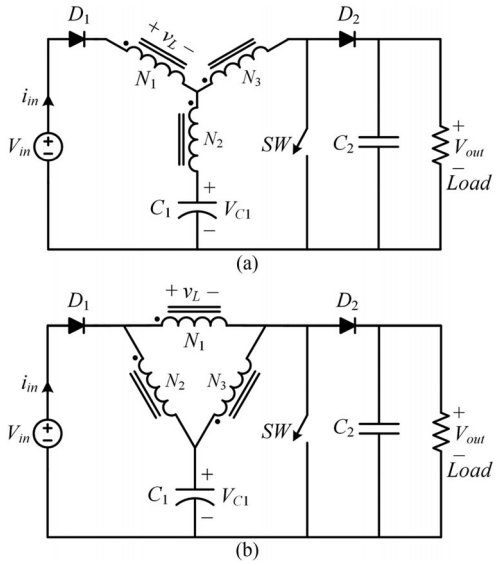

Fig. 1. Impedance networks with three coupled inductors: (a) Y-source and (b) Δ-source.

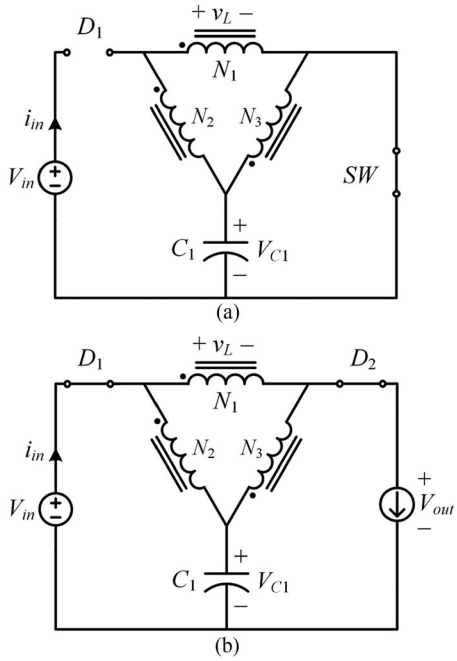

Fig. 2. Δ-source converter states (a) shoot-through and (b) nonshoot-through.

impedance network offers several advantages over the Y-source network, the main being a lower magnetizing current, which means more effective utilization of the core material and consequently smaller core size and volume. Also, as already demonstrated in [26], the Y-source output voltage is significantly sensitive to the leakage inductance, so the practical converter requires a precise closed loop control, which means extra cost and complexity, while this effect is minimized in the proposed Δ-source structure. Indeed, it will be shown that the voltage drop on the leakage inductance is highly reduced for the proposed Δ-source network compared to its Y-source counterpart. Furthermore, the winding losses of the Δ-source network are lower than those of the Y-source network, which decreases the reduction of the output voltage.

In this paper, the circuit analysis of the proposed impedance network is discussed and its characteristics are derived mathematically. After that the effect of leakage inductance is investigated and finally simulation and experimental comparative studies with the Y-source structure are presented.

II. Circuit Analysis

The proposed impedance network and the Y-source are shown in Fig. 1. The proposed topology has the same number of components as the Y-source. It is obvious that the only difference between two structures is the arrangement of coupled inductors. The main components of the proposed Δ-source are one capacitor (C_1), one diode (D_1), one switch (SW), and three coupled inductors, wound on the same core (N_1, N_2, N_3).

A. Operation Principle

This structure has the same operation states as other ZS converters, i.e., the ST and the non-ST states (NST), described as follows:

1) The ST state refers to the state that SW is conducting while D_1 is blocking, as shown in Fig. 2(a). In this state, the magnetizing inductance of the coupled inductors is charged through C_1. One can conclude from Fig. 2(a) that

$$v_L = \frac{N_1}{N_3} V_{C1}. \tag{1}$$

2) The NST state occurs when SW is OFF and D_1 conducts, as shown in Fig. 2(b), so the magnetizing inductance discharges to the load while the capacitor charges from the source and as a result the output voltage increases. It is obvious from Fig. 2(b) that

$$v_L = \frac{N_1}{N_2} \left(V_{\text{in}} - V_{C1} \right). \tag{2}$$

From (1) and (2), the capacitor voltage V_{C1} can be calculated by applying the volt-second balance over one switching period T, as

$$V_{C1} = V_{\text{in}} \frac{N_3 (1 - d_{\text{ST}})}{N_3 - N_1 d_{\text{ST}}} \tag{3}$$

where d_{ST} is the normalized ST time or the ST duty cycle. The converter voltage gain G can be readily determined by calculating the output voltage during the NST state, as

$$\hat{V}_{\text{out}} = V_{\text{in}} - v_L = V_{\text{in}} - \frac{N_1}{N_2} \left(V_{\text{in}} - V_{\text{in}} \frac{N_3 (1 - d_{\text{ST}})}{N_3 - N_1 d_{\text{ST}}} \right)$$
$$= V_{\text{in}} \left(\frac{N_3}{N_3 - N_1 d_{\text{ST}}} \right) \tag{4}$$

then

$$G = \frac{\hat{V}_{\text{out}}}{V_{\text{in}}} = \frac{1}{1 - \frac{N_1}{N_3} d_{\text{ST}}} = \frac{1}{1 - K_\Delta d_{\text{ST}}} \tag{5}$$

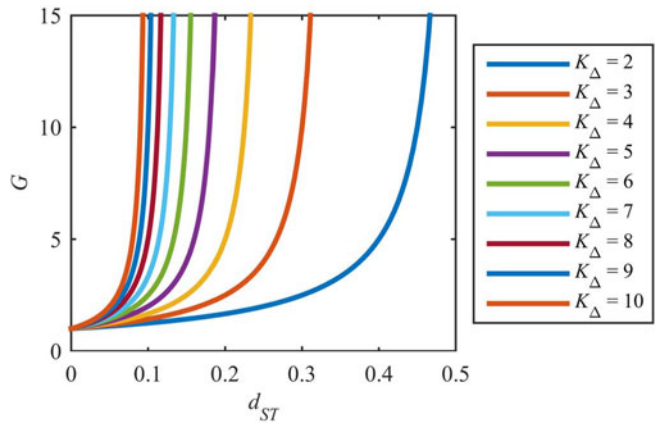

Fig. 3. Voltage gain (G) as a function of ST duty cycle for different turn ratios.

where $K_\Delta = N_1/N_3$ is the turn ratio of the transformer. The voltage gain of the Y-source converter is similar to this equation with K_Δ replaced by $K_Y = (N_3 + N_1)/(N_3 - N_2)$. Considering the volts/turn relation of the ideal three-winding transformer, i.e., $v_1/N_1 = v_2/N_2 = v_3/N_3$, where v_1, v_2, and v_3 are the voltages across the windings and the KVL relation among these voltages, i.e., $v_1 = v_2 + v_3$, one can simply conclude the following criteria to choose N_1, N_2, and N_3:

$$N_1 = N_2 + N_3. \tag{6}$$

Also, the upper limit of the ST duty cycle as a function of K_Δ is determined from (5), as

$$1 - K_\Delta d_{\rm ST} > 0 \Rightarrow d_{\rm ST} < \frac{1}{K_\Delta}. \tag{7}$$

To better illustrate the boosting performance, variations of voltage gain with the ST duty cycle for different turn ratios are depicted in Fig. 3. Obviously, high transfer gains can be achieved with small ST duty cycles by increasing the turn ratio K_Δ. It is a desirable feature in ac/ac and dc/ac converter applications, where increasing the ST duty cycle highly deteriorates the quality of the output voltage waveform. The shorter ST time is a common feature of all transformer-based ZS converters, specifically the Y-source of [24], at the price of requiring more precise adjustment of the ST duty cycle, especially for higher voltage gains. However, in practice, the values of $d_{\rm ST}$ and K_Δ must be chosen wisely. Although increasing K_Δ leads to a higher boost factor with a desired lower $d_{\rm ST}$, it produces more nonlinearity characteristics in the converter voltage gain and a small change in $d_{\rm ST}$ causes large variations in the voltage gain. So, depending on the application requirements some kind of compromise is necessary. For instance, in order to reach the voltage gain of $G = 3$, considering Fig. 3, $K_\Delta = 4$ is a proper choice. With the turn ratio $K_\Delta = N_1/N_3 = 4$, and considering (6), the coupled inductor turn ratio $N_1 : N_2 : N_3$ is finally calculated as 4:3:1.

Another issue with the transformer-based ZS converters is the effect of leakage inductances, which result in practical problems such as producing voltage spikes and decreasing the effective ST duty cycle. These effects are well investigated for the Y-source converter in [26]. In Section III, the effect of leakage inductances on the Δ-source converter performance is explored and the results are compared with the Y-source converter, which reveal that a considerable improvement is achieved.

B. Magnetizing Current and Core Size

The magnetic core size is mainly determined by the maximum stored energy during the ST time [27]. The maximum energy is related to the square of maximum magnetizing current, which can be calculated by

$$i_{m,\max} = I_m + \Delta i_m/2 \tag{8}$$

where I_m and Δi_m are the average and ripple value of the magnetizing current, respectively. The magnetizing current (i_m) is theoretically determined from the winding currents by the Ampere's law, as

$$N_1 i_m = N_1 i_1 + N_2 i_2 + N_3 i_3. \tag{9}$$

During the ST state, it is obvious from Fig. 2(a) and (9) that

$$\begin{aligned} i_m &= i_1 + \frac{N_2}{N_1} i_2 + \frac{N_3}{N_1} i_3 = i_2 \left[\frac{N_2 - N_1}{N_1}\right] + \frac{N_3}{N_1} i_3 \\ &= \frac{N_3}{N_1}\left[i_3 - i_2\right] \end{aligned} \tag{10}$$

so the capacitor current can be expressed as

$$i_{C1} = i_2 - i_3 = -\frac{N_1}{N_3} i_m. \tag{11}$$

Alternately, during the NST state, (9) becomes

$$\begin{aligned} N_1 i_m &= N_1 i_1 + N_2(i_{\rm in} - i_1) + N_3 i_3 \Rightarrow (i_1 + i_3) \\ &= \frac{N_1 i_m - N_2 i_{\rm in}}{N_3} \end{aligned} \tag{12}$$

and the capacitor current is found as

$$i_{C1} = i_{\rm in} - (i_1 + i_3) = i_{\rm in} - \frac{N_1 i_m - N_2 i_{\rm in}}{N_3}. \tag{13}$$

By substituting the average currents of each state in (11) and (13), the average capacitor currents in ST and NST states are calculated as

$$\begin{cases} I_{C1,\rm ST} = -\frac{N_1}{N_3} I_m \\ I_{C1,\rm NST} = I_{\rm in,NST} - \frac{N_1 I_m - N_2 I_{\rm in,NST}}{N_3} \end{cases} \tag{14}$$

where, as shown in Fig. 4, $I_{\rm in,NST}$ is the average input current during the NST state. Applying the ampere-second balance to the capacitor current during a switching period, the average magnetizing current is derived as

$$I_m = (1 - d_{\rm ST}) I_{\rm in,NST} = I_{\rm in}. \tag{15}$$

Also, the voltage equation of (16) is used to calculate the ripple component of the magnetizing current:

$$v_L = L_m \frac{\Delta i_m}{\Delta t}. \tag{16}$$

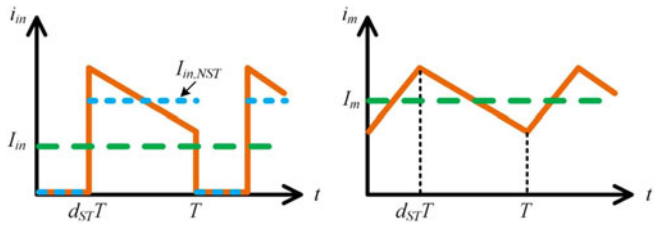

Fig. 4. Input and magnetizing currents waveforms during a switching period.

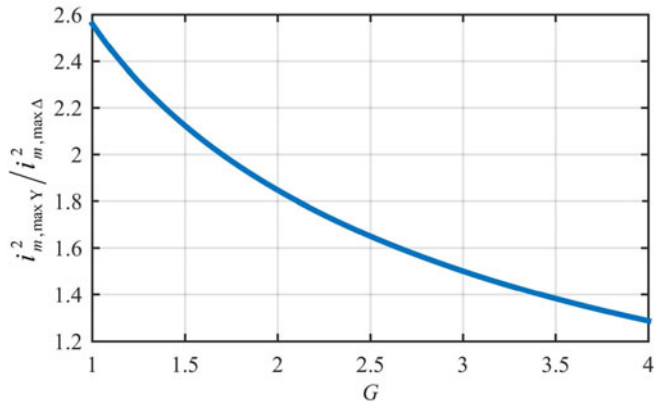

Fig. 5. Ratio of $i^2_{m,\max Y}/i^2_{m,\max \Delta}$ for Y- to Δ-source converter as a function of gain.

During the NST state the magnetizing current ripple can be expressed as

$$\Delta i_m = \frac{V_{\rm in}(G-1)}{L_m}(1-d_{\rm ST})T. \tag{17}$$

By following the same approach for the Y-source converter, the following results are attained for the average and ripple components of the magnetizing current:

$$I_m = \left(1+\frac{N_3}{N_1}\right) I_{\rm in} \tag{18}$$

$$\Delta i_m = \frac{N_1}{N_3-N_2}\frac{GV_{in}}{L_m}(1-d_{\rm ST})d_{\rm ST}T \tag{19}$$

In order to compare the maximum stored energy and the required core size for Y- and Δ-source converters, the ratio of $i^2_{m,\max Y}/i^2_{m,\max \Delta}$ as a function of voltage gain is plotted in Fig. 5. Evidently the Δ-source converter requires a very smaller magnetic core, especially at lower gains. For both converters, the input voltage and power are 60 V and 200 W, respectively. The magnetizing inductance is 1.2 mH and the turn ratios of the Y- and the Δ-source converters are (5:1:3) and (4:3:1), respectively, which result to $K_\Delta = K_Y = 4$. As it is clear from (17) and (19), the weakness of the proposed Δ-source against Y-source is its higher magnetizing current ripple, which produces more core losses. Using (17) and (19), the ratio of $\Delta i_{m,\Delta}/\Delta i_{m,Y}$ is obtained as $1 + N_{3,Y}/N_{1,Y}$, which for above-mentioned turns ratio is calculated as 1.6.

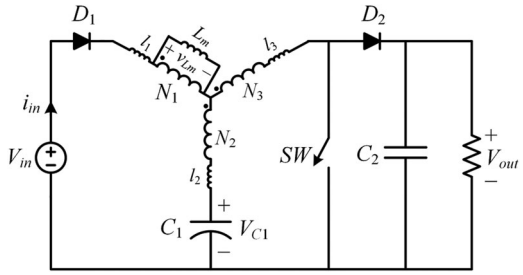

Fig. 6. Y-source converter in the presence of leakage inductances.

III. Effect of Parasitic Elements of Coupled Inductors

The parasitic parameters such as leakage inductances, equivalent series resistances (ESRs) of windings, diodes, and switch volt-drop can highly affect the converter performance. The main differences of parasitic parameters between Y- and Δ-source converters are in leakage inductances and windings ESRs. So, in the following the effect of these parameters is investigated. Regarding the Y-source, the leakage inductances reduce the effective $d_{\rm ST}$ and consequently the converter voltage gain [26]. Besides, the volt-drops on the ESRs cause more voltage gain reduction. In the following these effects are studied.

The voltage gain expression of (5) and the permissible ST duty cycle range, already defined by (7), are both derived with the assumption that the leakage inductances are substantially small to be safely ignored. In order to attenuate the voltage spikes in the magnetically coupled converters to a safe limit, the coupling among the inductors must be tight to ensure that the leakage inductances are as small as possible; however, in a practical case gaining a tight coupling is hard and expensive and some degree of compromise is unavoidable.

While during the ST and the NST states, the leakage inductances can be neglected due to their small values compared to the magnetizing inductance ($L_m \gg l_1, l_2, l_3$), but during the transition from the NST to the ST state, they resist against the rapid changes of the windings currents and affect the function of the converter. Therefore, with considering the leakage inductances, an extra state, called the intermediate (INT) state, must also be taken into account to examine the effect of leakage inductances [26]. The circuit model that is used to demonstrate the effect of leakage inductance on the Y-source converter is shown in Fig. 6 [26]. In the same manner, the equivalent circuits of the Δ-source converter during the three states are depicted in Fig. 7. The INT state, which is shown at the bottom of Fig. 7, occurs right after the NST and before the ST states when SW is turned ON but D_1 still conducts due to the existence of the leakage inductances. During this state, the currents i_1 and i_2 change rapidly and finally become equal ($|i_1| = |i_2|$) at the end of the INT state. It should be noted that the duration of the INT state is part of the desired ST time (i.e., $d_{\rm ST}T$), while as already shown in [26], the voltage across the magnetizing inductance in this state is almost equal to its value during the NST state, which means that the converter behaves mostly similar to the NST state; therefore, the effective ST duty cycle is calculated

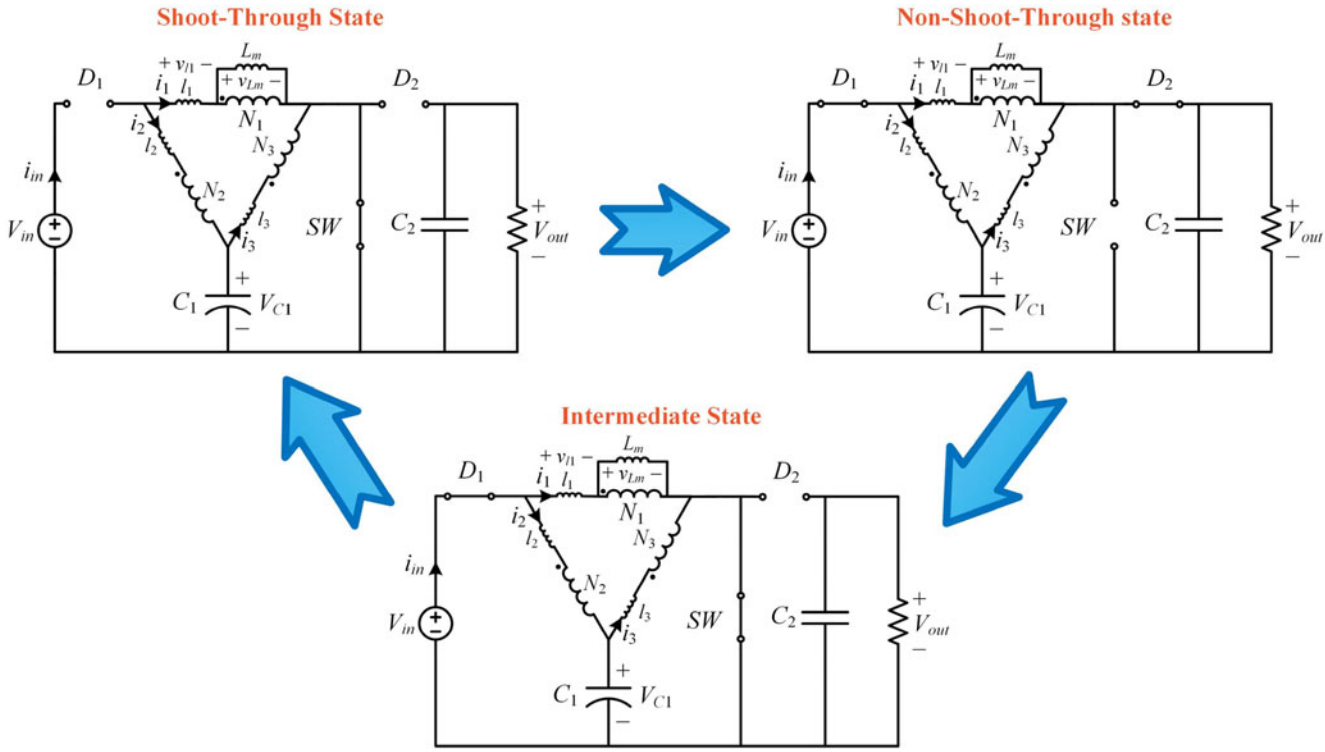

Fig. 7. Illustration of intermediate state of Δ-source in the presence of leakage inductances.

as

$$d_{\mathrm{ST,effective}} = d_{\mathrm{ST}} - \Delta d_{\mathrm{ST}} \tag{20}$$

where Δd_{ST} is the normalized time of the INT state and can be calculated using the voltage across the leakage inductance as

$$\Delta d_{\mathrm{ST}} = \frac{L_{l1}\Delta I_1}{TV_{l1}} \tag{21}$$

where V_{l1} is the voltage across the first winding leakage inductance during the INT state and ΔI_1 is the change of i_1 during the INT state. Equations (20) and (21) are both valid for Δ- and Y-networks. However, their expected values are significantly different because of the difference between ΔI_1 and V_{l1} for two structures. Although finding the exact value of Δd_{ST} is not simple, comparisons between Δd_{ST} values for two structures are presented by simulations and experiments. It will be shown with simulations and experiments that Δd_{ST} is much smaller for the proposed Δ-source compared to the Y-source network.

The effect of other parasitic parameter (i.e., the ESR volt-drop) on the voltage gain depends on the winding currents of the Y- and Δ-source converters. However, with respect to the winding configurations of Y and Δ, it is obvious that the existence of parallel paths for current in different states of the Δ configuration leads to less ESR volt-drop than the Y-connected windings, which means less gain reduction. The total gain reductions resulted from the effect of parasitic parameters are evaluated with both simulation and experimental tests.

Table I shows a brief comparison of different parameters among impedance networks with coupled inductors. As it is clear, the proposed structure offers several advantages simultaneously, such as high voltage gain with low d_{ST} while keeping down the magnetizing current in order to reduce core size, which is not possible to achieve in other structures. Also the voltage stress on the capacitor and diode is the same as other structures at the same d_{ST} and input voltage.

IV. Performance Confirmation

In order to confirm the theoretical achievements, the proposed circuit as well as the Y-source circuit is simulated in PLECS software and results are compared with experimental results from a prototype, which was built in the laboratory.

The prototype parameters for both simulations and experiments are listed in Table II. For Δ- and Y-networks, the winding turn ratios are chosen as 4:3:1 and 5:1:3, respectively. Same magnetizing inductance is achieved by choosing equal N_1. Therefore, K is equal to 4 and d_{ST} is limited between 0 and 0.25. In Section II, it was mentioned that by increasing the duty cycle, the outputs become sensitive to small variations. To show the performance of converter with a reasonable values, it is decided that $d_{\mathrm{ST}} = 0.167$, which means $G = 3$.

The value of $i_{m,\max}$ for both converters can be calculated by (8) and considering $L_m = 1.2\,\mathrm{mH}$, $L_m i_{m,\max}^2$, which is directly related to the core size, can be obtained as 52.8 and 35.2 mH·A^2 for Y and Δ inductors, respectively. It was also expected from Fig. 5 that the required core size of Y is 1.5 times

TABLE I
COMPARISON BETWEEN Δ- AND Y-SOURCE CONVERTERS

Converter	K	G	V_{C1}	V_{D1}	I_m	Δi_m
Δ-source	$\frac{N_1}{N_3}$	$\frac{1}{1-K_\Delta d_{ST}}$	$(1-d_{ST})GV_{in}$	$(K_\Delta-1)GV_{in}$	$\frac{P}{V_{in}}$	$\frac{(G-1)V_{in}}{L_m}(1-d_{ST})T$
Y-source [24], [25]	$\frac{N_3+N_1}{N_3-N_2}$	$\frac{1}{1-K_Y d_{ST}}$	$(1-d_{ST})GV_{in}$	$(K_Y-1)GV_{in}$	$(1+\frac{N_3}{N_1})\frac{P}{V_{in}}$	$\frac{N_1}{N_3-N_2}\frac{GV_{in}}{L_m}d_{ST}(1-d_{ST})T$
T-source or Trans-Z-source [18]	N	$\frac{1}{1-(1+K_T)d_{ST}}$	$(1-d_{ST})GV_{in}$	$K_T GV_{in}$	$(1+\frac{1}{N})\frac{P}{V_{in}}$	$N\frac{GV_{in}}{L_m}d_{ST}(1-d_{ST})T$
Γ-Z-source [19]	$\frac{N}{N-1}$	$\frac{1}{1-K_{\Gamma-Z}d_{ST}}$	$(1-d_{ST})GV_{in}$	$\frac{1}{N-1}GV_{in}$	$\frac{P}{V_{in}}$	$\frac{N}{1-N}\frac{GV_{in}}{L_m}d_{ST}(1-d_{ST})T$
Flipped Γ-Z-source [20]	N	$\frac{1}{1-K_{f\Gamma-Z}d_{ST}}$	$(1-d_{ST})GV_{in}$	$(K_{f\Gamma-Z}-1)GV_{in}$	$\frac{P}{V_{in}}$	$\frac{1}{N(N+1)}\frac{GV_{in}}{L_m}(1-d_{ST})^2T$
Σ-Z-source [21]	$2+\frac{1}{N_{\Gamma1}-1}+\frac{1}{N_{\Gamma2}-1}$	$\frac{1}{1-K_{\Sigma-Z}d_{ST}}$	$(1-d_{ST})GV_{in}$	$\frac{-(N_{\Gamma1}N_{\Gamma2}-1)}{(N_{\Gamma1}-1)(N_{\Gamma1}-1)}G$	$\frac{P}{V_{in}}$	$\frac{N_{\Gamma1}}{1-N_{\Gamma1}}\frac{GV_{in}}{L_m}d_{ST}(1-d_{ST})T$

Magnetizing currents are referred to high turn number windings.

TABLE II
SYSTEM PARAMETERS

Parameter	Value
Load resistance	162 Ω (200 W @ 180 V)
Output voltage	180 V
Input voltage	60 V
Switching frequency (1/T)	20 kHz
C_1/C_2	470 μF /470 μF
Inductor turns	Δ:120:90:30/Y:120:24:72
Core	0077615A7
Switch	C3M0065090D
Diode 1	C4D10120D
Diode 2	FEP30JP

TABLE III
MEASURED VALUES OF LEAKAGE INDUCTANCES

Inductor	l_1 (N_1)	l_2 (N_2)	l_3 (N_3)
Y	13.6 μH (120)	1.23 μH (24)	0.60 μH (72)
Δ	5.00 μH (120)	1.67 μH (90)	2.47 μH (30)

of Δ. Finally, the core can be chosen using these values from the core manufacturer catalog [27]. However, in order to better comprise the converter performance, same core is used in the experiments.

In the simulations, all parasitic parameters are considered based on experimental prototype; the leakage inductances are measured as Table III using the procedure of [28], the calculated dc resistances are regarded as windings ESRs and also a typical value is chosen from datasheets for the diodes voltdrops and MOSFET ON resistance. Fig. 8 shows the comparative simulation results. Clearly both structures boost the input voltage from 60 to 180 V (not exactly). The output voltage of the Δ-source experiences less reduction. Fig. 8(b) shows the windings currents. Windings losses can be roughly approximated as $P_{loss} = R\,i_{rms}^2$. It is acceptable to assume that the winding resistance is proportional to the wire length and therefore the winding turn number. So, one can deduce that $P_{loss} \propto N i_{rms}^2$. Table IV compares both converters from the winding losses point of view based on above-defined criteria. The winding losses of Δ-source converter are less than half of the Y-source. As it is clear, although the Δ inductor has higher turn number, the rms values of winding currents are significantly smaller, which is the main reason of smaller winding losses. It must be considered that the values in Table IV are not losses in W and are just proportional to the losses. As it is shown in Fig. 5, the core size and weight of Δ inductor are smaller than those of Y. On the other hand, the winding volume and weight are related to its turn number and wire bare area (A_w) or rms value of currents as $V_{winding} \propto (NA_w$ or $Ni_{rms})$. The relative weight or volume of both inductors windings is calculated in Table IV. The total winding weight of Δ is less than that of Y by the factor of 0.69. Consequently, both core and windings weight and therefore the total weight of Δ inductor is less than that of Y.

As mentioned in Section III, the presence of leakage inductances results in the INT state, which reduces the effective d_{ST} and the output voltage. The INT state is zoomed in Fig. 8(c). Obviously, Δd_{ST} is much lower for the Δ-source compared to the Y-source and as it can be seen in Fig. 8(a), the direct result is less output voltage reduction.

Other practical problems due to the leakage inductances are the ringing and spikes in the voltage of semiconductor devices, which is produced due to the presence of parasitic capacitance (c_p) in parallel and inductance (l_p) in series with the semiconductor devices. In order to protect semiconductor devices, D_1 in the studied circuits, against this high voltage spikes, snubber circuits are usually used. The required snubber capacitor value is related to the parasitic inductance or inversely related to the square of ringing frequency ($f_{ring}^2 = 1/(4\pi^2 l_p c_p)$). So a lower ringing frequency required a higher snubber capacitor value and consequently increased snubber dissipation [29]. The parasitic capacitance of D_1 is measured from experiments using the procedure presented in [29] equal to 700 pF. The main source of l_p is the leakage inductances of the coupled inductors. Considering these parameters in the simulations, Fig. 9 shows the difference between ringing frequencies of both converters. This figure clearly shows that the ringing voltage frequency for the Δ-source is around 1.35 MHz while this value for the Y-source is about 0.962 MHz approximately. Considering equal parasitic capacitances, it means that the parasitic inductance in series with the diode for the proposed structure is smaller in comparison with the Y-source, which results in less snubber requirements and dissipation.

In order to show the performance of the Δ-source network in practice, a 200 W prototype, which is shown in Fig. 10, was

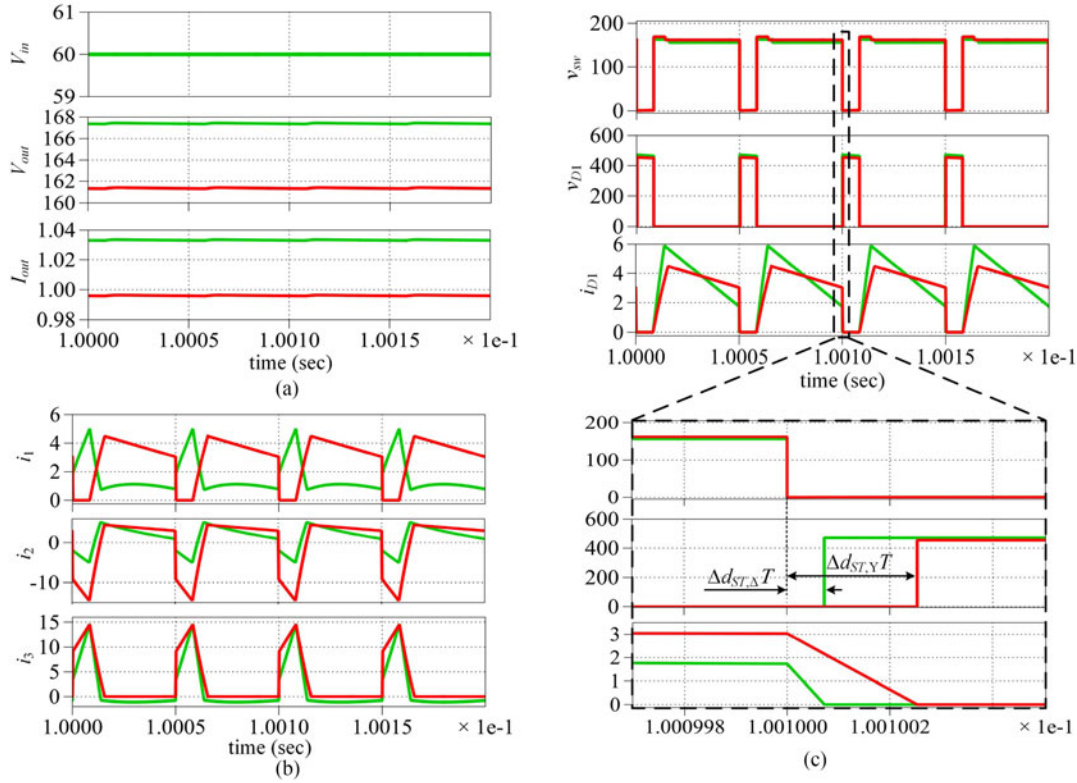

Fig. 8. Simulation results for Δ-source (green) and Y-source (red).

TABLE IV
WINDING LOSSES COMPARISON

Converter	$i_{1,\mathrm{rms}}(N_1)$	$i_{2,\mathrm{rms}}(N_2)$	$i_{3,\mathrm{rms}}(N_3)$	$\sum N_j i_{j,\mathrm{rms}}^2$	$\sum N_j i_{j,\mathrm{rms}}$
Y-source	3.31 A (120)	6.31 A (24)	5.66 A (72)	4580	957
Δ-source	1.95 A (120)	3.13 A (90)	4.77 A (30)	2024	660

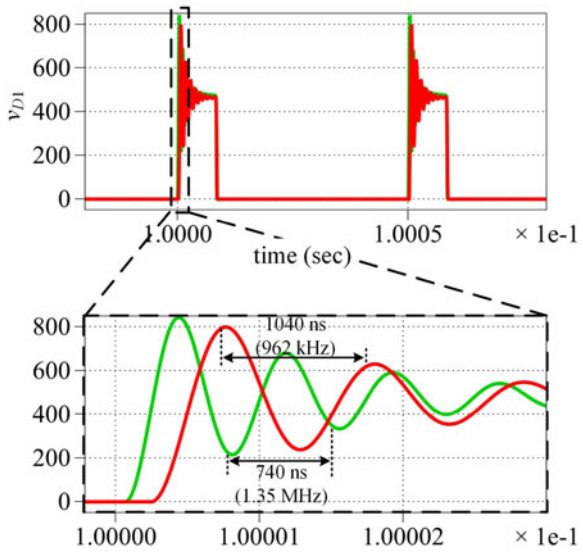

Fig. 9. D_1 voltage for Δ-source (green) and Y-source (red).

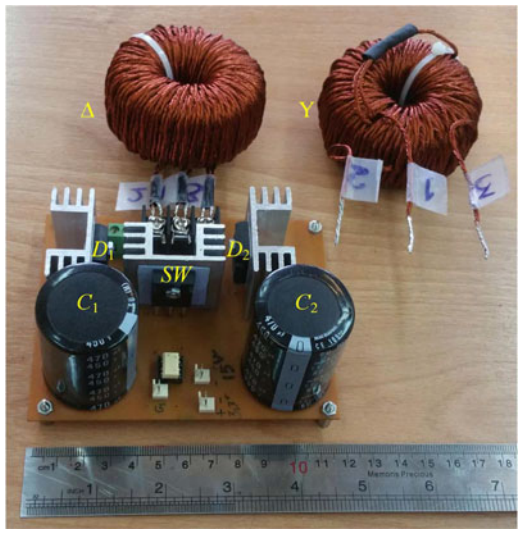

Fig. 10. Image of experimental setup.

built. To facilitate the comparison between two structures, both impedance networks were implemented on the same board, so it is acceptable to claim that both circuit structures operate under the same circumstances, such as the same parasitic parameters. The converter parameters are listed in Table II. To highlight the differences between Y- and Δ-networks, snubber circuits were not implemented for the diodes or the switch, so the effect of parasitic parameters can be seen clearly.

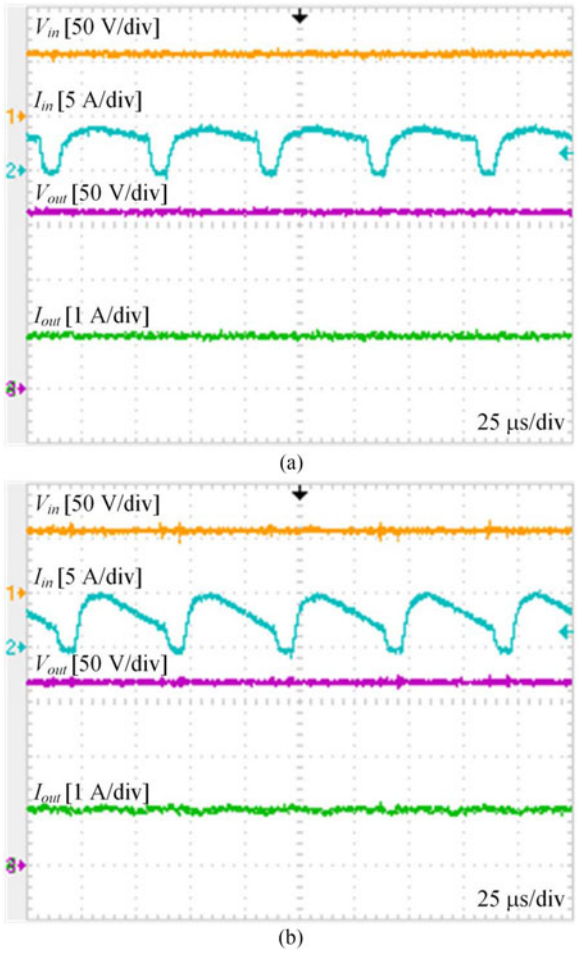

Fig. 11. Experimental waveforms: (a) Y-source and (b) Δ-source.

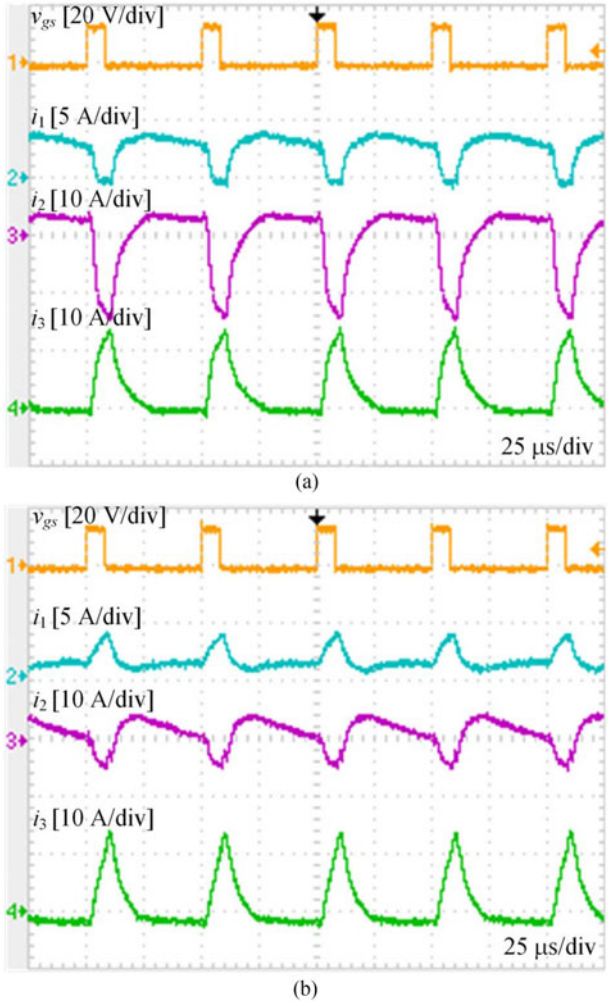

Fig. 12. Experimental waveforms: (a) Y-source and (b) Δ-source.

Fig. 11 shows input and output waveforms for both structures. Experimental measurements show that the output voltages for the Y- and Δ-source circuits reach to 157.65 and 163.5 V, respectively. Output voltage drop for the Δ-source is around 17 V while this value for the Y-source is around 23 V. As mentioned before, both structures are implemented on the same circuit, so the main difference between output results is caused by different leakage inductances and the ESRs. Fig. 12 shows windings currents, which are in good agreement with the simulation results and give valuable information about the current variations during the NST and the ST states.

Finally, Fig. 13 clearly compares the effect of leakage inductances on the effective ST duty cycle and the voltage ringing frequency. This figure also confirms the simulation results of Fig. 9 and measured values of leakage inductances, mentioned in Table III. As it mentioned before, in the experiments, d_{ST} is set to 0.167; however, the presence of leakage inductances reduces this value to 0.1634 (output voltage reduced to 173.2 V) and 0.1656 (output voltage reduced to 177.7 V) for the Y- and the Δ-source converters, respectively. The more gain reduction in practice can be attributed to the volt-drops on the ESRs and the conducting semiconductors; however, as can be seen this effect is much lower for the Δ-source converter. Fig. 13 shows valuable information for designing the snubber circuit which is in good agreement with the simulation results of Fig. 9. As it was discussed before, the frequency of voltage ringing is a dominant factor for snubber design. As expected, the frequency of ringing for the Δ-source is higher than that for the Y-source.

The measured efficiencies of both converters are shown in Fig. 14 . In a practical application, the output voltage of converter is usually fixed by using a closed loop control system. Therefore, for the efficiency measurements, the output voltages of both converters are fixed to the nominal voltage (i.e., 180 V) by adjusting d_{ST}. As it is mentiond, the winding loss for the proposed Δ-source converter is lower than that for the Y-source, which results in higher efficency of the Δ-source converter, especially at higher loading conditions. In order to better compare the distribution of losses among key components of the two converters, the losses on each component are estimated by using the analytical method presented in [22]. The comparative results at the nominal loading condition (200 W) are shown in Fig. 15. As expected, the winding loss of the Y-source

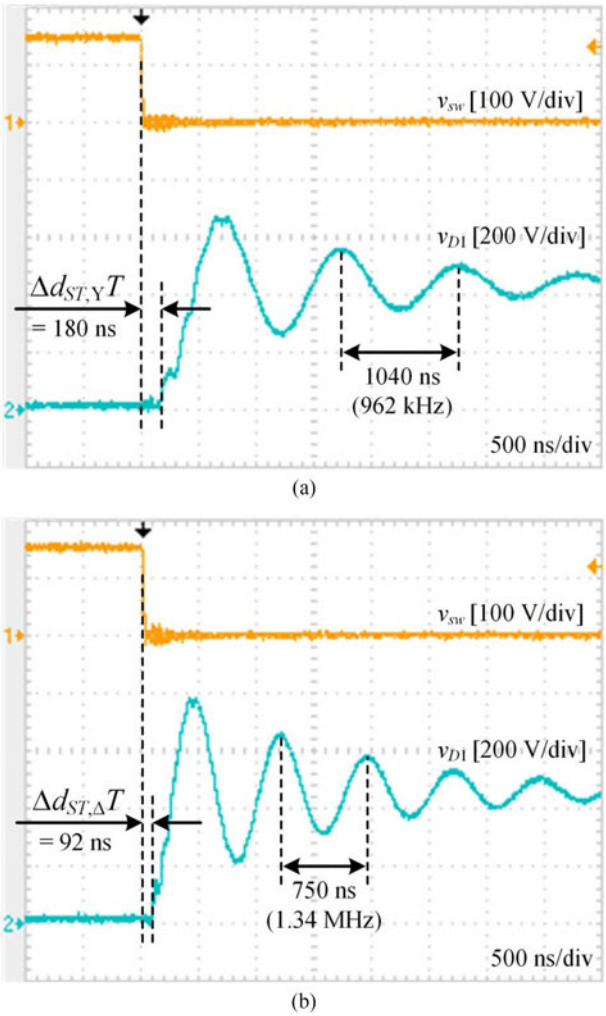

Fig. 13. Experimental waveforms: (a) Y-source and (b) Δ-source.

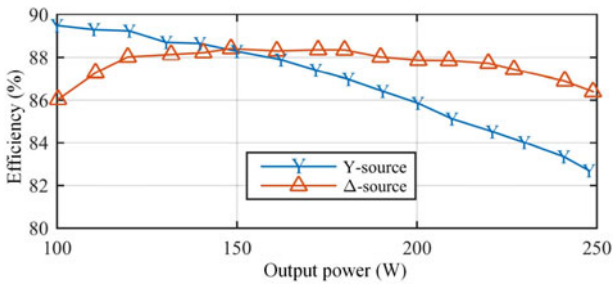

Fig. 14. Measured efficiency at different output powers.

converter is almost two times the Δ-source converter, while other losses are approximately equal. It is worth mentioning that the core loss of the Δ-source converter is higher; however, its share in the total converter losses is not considerable. Therefore, the main source of efficiency difference between the two converters is the winding loss.

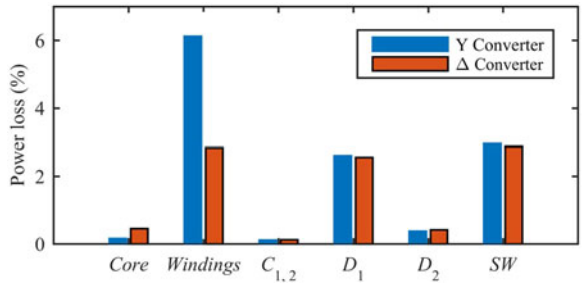

Fig. 15. Comparative loss analysis between Y- and Δ-source converters.

V. Conclusion

A novel ZS converter with three coupled inductors connected in Δ was presented in this paper. In comparison with the conventional Y-source network, the proposed Δ-source network took benefit of a smaller leakage inductance, which led to less reduction of the effective ST duty cycle and required smaller snubber than the Y-source. Furthermore, winding losses of Δ-source network were smaller, which resulted in higher efficiency, especially at higher output power and smaller volt-drops, which made the Δ-source converter gain reduction less than the Y-source structure. Another advantage of proposed structure was its smaller magnetizing current, which resulted in a smaller core size. The weakness of the proposed structure was its higher core loss due to the larger magnetizing current ripple. The effectiveness of the proposed structure and above-mentioned advantages were proved by simulations and experiments.

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