A Multilevel AC/AC Converter With Reduced Number of Switches

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***Abstract*—In this paper, a single-phase multilevel ac/ac converter with reduced number of power semiconductor devices is proposed. For the simple case of a three-level converter, only three bidirectional switches and two capacitors are required. The proposed converter provides a highly sinusoidal and regulated output voltage with a simple topology. The efficiency is high because in each state of operation only one semiconductor conducts. The converter can be easily extended to any desired levels in the output voltage to even more reduce the output total harmonics distortion. Another advantage of the proposed converter is that by increasing the voltage levels, the stress on the switches will decrease. The proper performance of the proposed converter is confirmed through extensive simulation and experimental tests.**

***Index Terms*—AC/AC converter, efficiency, *n*-level voltage, stress voltage, total harmonics distortion (THD).**

I. INTRODUCTION

FOLLOWING the recent advances in power electronics, such as the availability of high-power/voltage transistor switches and development of efficient modulation and control algorithms, new topologies for conventional converters are under serious investigations by researchers. In this way, the phase-controlled ac voltage regulators are recently replaced by pulse width modulated (PWM) ac to ac converters, which can generate the high-quality input and output waveforms with minimum harmonic distortions [1]–[12]. A serious problem with these converters is the lower voltage rating of available transistor switches compared to the thyristors, which are used in the structure of conventional phase-controlled converters. A recent solution to this problem is the adoption of multilevel conversion concepts to the ac/ac converter circuits [13].

The multilevel power conversion technique was first proposed for the dc/ac converters [14]–[20] and was then successfully adopted to the dc/dc converters [21], [22]. Most recently, multilevel ac choppers are proposed for high-power and medium-voltage applications [23]–[29], where the availability of semiconductor devices is a major challenge. Besides, the multilevel

technique offers many other practical advantages, such as reduced total harmonics distortion (THD) of the output voltage, less voltage stress on the power semiconductors, less distortion of the input current and filtering requirements, etc.

The main idea of multilevel ac/ac power conversion is to use a combination of capacitors and bidirectional semiconductor switches to divide the switched voltages to some lower levels.

The result is a staircase voltage waveform in the output while the voltage stress on each semiconductor switch is much lower than the main voltages. Available multilevel ac choppers are basically derived from the conventional two-level ones by replacing the bidirectional switches with the capacitor clamped base cells and/or by series or parallel connection of floating capacitors [23]. While all these conventional multilevel ac choppers offer the advantages of lower voltage stresses, bidirectional power flow, high input power factor and high quality and regulated output waveforms, but all suffer from requiring a large number of switches, especially when the number of output levels increases. For example, all topologies proposed yet require at least four bidirectional switches to generate a three-level output.

Consequently, in this paper, a novel three-level ac/ac converter is proposed that can generate the output levels of V_i, $V_i/2$, and 0, with a reduced number of power switches (three bidirectional switches). However, the proposed converter circuit has the flexibility to easily increase the number of voltage levels. In addition to the reduced number of switches, which translates to a lower cost and volume, the proposed converter presents very low conduction losses, since in all operating states only one switch conducts.

The paper is arranged as follows. Section II describes the proposed ac/ac converter. In Section III, the operation states of the ac/ac converter are investigated. Section IV presents the steps to calculate the output voltage equation. Section V discusses the design of the converter parameters. In Section VI, the proposed converter is compared with other competitors. In Section VII, a procedure based on genetic algorithms is proposed to determine the optimum duty ratios in order to minimize the output voltage THD. Simulation and experimental results illustrating the performance of the converter are presented in Section VIII. Section IX concludes the paper.

II. PROPOSED CONVERTER TOPOLOGY

Fig. 1 shows the proposed multilevel ac/ac converter. In this structure, the number of switches depends on the number of levels. The ac-link capacitors $C_1 - C_n$ are large enough to be
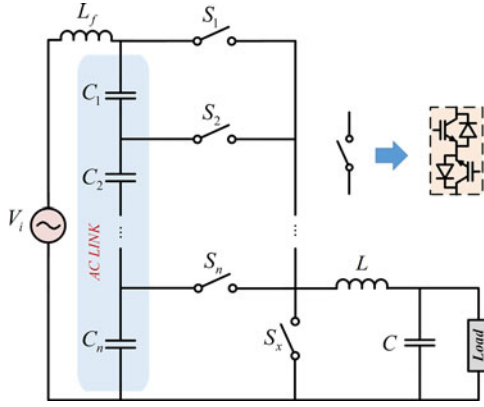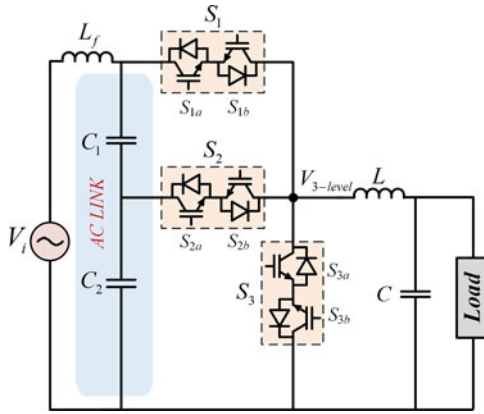
Fig. 1. Proposed multilevel ac/ac converter.

Fig. 2. Proposed three-level ac/ac converter.

TABLE I
POSSIBLE SWITCHING STATES AND THE GENERATED VOLTAGES

Output	State	S_1	S_2	S_3
V_i	I	1	0	0
$V_i/2$	II&IV	0	1	0
0	III	0	0	1

considered as a constant voltage source during a short switching period. As will be demonstrated, the switch directly connected between the power supply and the load (S_1) and the free-wheeling switch (S_x) work at half of the switching frequency and switches S_2-S_n work at the switching frequency. The switch S_x provides the free-wheeling path for the load current during the commutation of main switches and also generates the zero-level output. Unlike most conventional circuits, in the circuit of Fig. 1, only one switch conducts at any time that substantially reduces the conduction losses. As already stated and it is obvious in Fig. 1, the proposed converter can theoretically generate any desired number of levels by connecting the same number of voltage dividing capacitors in series. However, for the sake of simplicity, the rest of paper focuses on the simplest case of a three-level converter, shown in Fig. 2. Table I illustrates all possible switching states and associated output voltage levels.

Evidently, the proposed three-level buck ac/ac converter can generate the output voltages equal to V_i, $V_i/2$ and 0, assumed that the input capacitors C_1 and C_2 are equal.

III. OPERATION PRINCIPLE AND OUTPUT VOLTAGE ANALYSIS

To simplify the steady-state analysis, the following assumptions are made: the switching and conduction losses of the components are neglected, the input and output voltages are considered constant during a switching period T_s, the ac-link capacitors C_1 and C_2 are large enough to be considered as constant ac voltage sources with the instantaneous value of $V_i/2$. The converter in Fig. 2 has four distinct operating states, which are explained in the following.

A. Operation State I

In state I, [t1 $\sim$ t2] [refer to Figs. 4 and 3(a)], the switch S_1 conducts. The switching period is T and the switch-on ratio (or S_1 duty ratio) is D_1. The switch is open for the rest of the switching period, i.e., $(1 - D_1)T$. The current through inductance changes during state I as given by the following, in which V_c is the output voltage:

$$I_{\max 1} - I_{\min 1} = \left(\frac{V_i - V_c}{L} \right) D_1 T. \tag{1}$$

B. Operation States II and IV

In both states II [t2 $\sim$ t3] and IV [t4 $\sim$ t5] [refer to Figs. 4 and 3(b)], the switch S_2 conducts. The switch-on ratio is D_2. The current through inductance increases almost linearly and the total changes during states II and IV can be written as

$$I_{\max 2} - I_{\max 1} = \left(\frac{\frac{V_i}{2} - V_c}{L} \right) D_2 T \tag{2}$$

$$I_{\min 1} - I_{\min 2} = \left(\frac{\frac{V_i}{2} - V_c}{L} \right) D_2 T. \tag{3}$$

C. Operation State III

In state III, [t3 $\sim$ t4] [refer to Figs. 4 and 3(c)], the switch S_3 conducts. The voltage across the inductance is $V_L = -V_c$, so the current through inductance decreases almost linearly as given by

$$I_{\min 2} - I_{\max 2} = \left(\frac{-V_c}{L} \right) (1 - D_1 - 2D_2) T. \tag{4}$$

In the steady-state condition, the average inductor voltage over one switching period has to be zero, which lets calculate the converter gain. The result is given in the following, in which $D = D_1 + D_2$:

$$V_c = DV_i. \tag{5}$$

Equation (5) is similar to the steady-state voltage gain of the conventional buck chopper, with the extra flexibility that the
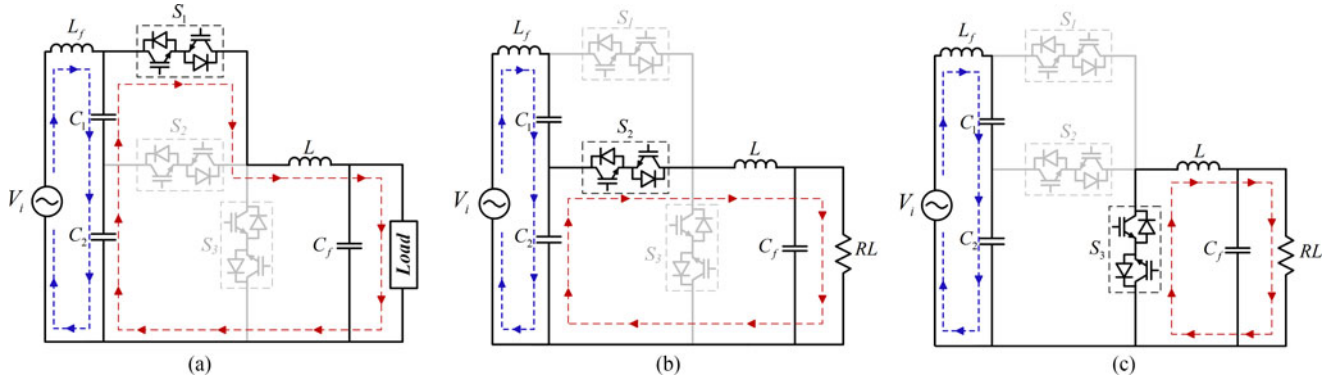
Fig. 3.   Operation states (a) I, (b) II and IV, and (c) III.

voltage gain can be adjusted with two parameters D_1 and D_2, provided that the inductor current is continuous.

IV. ANALYSIS OF THE OUTPUT VOLTAGE WAVEFORM

The input voltage is defined as an ideal sinusoid, presented in the following, where ω is the angular frequency and V_{p-p} in the peak voltage:

$$V_i = V_{p-p} \sin(\omega t). \tag{6}$$

The Fourier series of the three-level voltage of Fig. 4 with the assumption that $V_i = 110$ is given by [11] (7), shown at the bottom of this page, where D_1, D_2, and ω_s are the duty ratios of switches 1 and 2 and the angular switching frequency, respectively. With a sinusoidal envelop as (6), the generated voltage by the converter yields (8), shown at the bottom of this page.

The THD is defined as

$$\text{THD}_v = \frac{100}{V_{\text{of}}} \sqrt{\sum_{k=1}^{\infty} V_{\text{ok}}} \tag{9}$$

where V_{ok} and V_{of} are the amplitudes of the harmonic and fundamental components of the output voltage, respectively.

Assuming an ideal smoothing filter and a resistive load at the output, the relation between the fundamental components of the

output and the converter voltages is

$$V_{\text{of}} = \left| \frac{-jX_c R}{(X_L X_c) + jR(X_c - X_L)} \right| V_{\text{rf}} \tag{10}$$

where

$$X_c >> R >> X_L$$

$$X_c = \frac{1}{\omega C} \tag{11}$$

$$X_L = \omega L \tag{12}$$

$$V_{\text{rf}} = (D_1 + D_2)V_{p-p} \tag{13}$$

then

$$V_{\text{of}} = \left(\frac{RX_c}{\sqrt{(X_L X_c)^2 + (RX_c - RX_L)^2}} \right) V_{\text{rf}} \approx V_{\text{rf}}. \tag{14}$$

Also the similar approach can be followed for the harmonic components as

$$V_{\text{ok}} = \left| \frac{-jRX_{\text{cfs}}}{(X_{\text{Lfs}}X_{\text{cfs}} - j(X_{\text{cfs}} - X_{\text{Lfs}})R)} \right| V_{\text{rk}} \tag{15}$$

$$V_{\text{3 - level}} = (D_1 + D_2) + \sum_{n=1}^{\infty} \left(\left(\frac{[\sin(2\pi n(D_1 + D_2)) - \sin(2\pi nD_2) + \sin(2\pi n(D_1 + 2D_2))]^2}{2\pi n} \right) \times \cos(n\omega_s t) \right.$$

$$\left. + \left(\frac{[\cos(2\pi nD_2) - \cos(2\pi n(D_1 + D_2)) - \cos(2\pi n(D_1 + 2D_2)) + 1]^2}{2\pi n} \right) \times \sin(n\omega_s t) \right) \tag{7}$$

$$V_r = (D_1 + D_2)(V_{p-p} \sin(\omega t))$$

$$+ \sum_{n=1}^{\infty} \left(\left(\frac{\sin(2\pi n(D_1 + D_2)) - \sin(2\pi nD_2) + \sin(2\pi n(D_1 + 2D_2))}{4n\pi} \right) ((\sin(n\omega_s \pm \omega)t)(V_{p-p})) \right.$$

$$\left. + \left(\frac{\cos(2\pi nD_2) - \cos(2\pi n(D_1 + D_2)) - \cos(2\pi n(D_1 + 2D_2)) + 1}{4n\pi} \right) \times (\cos(n\omega_s \pm \omega)t)(V_{p-p})) \right) \tag{8}$$
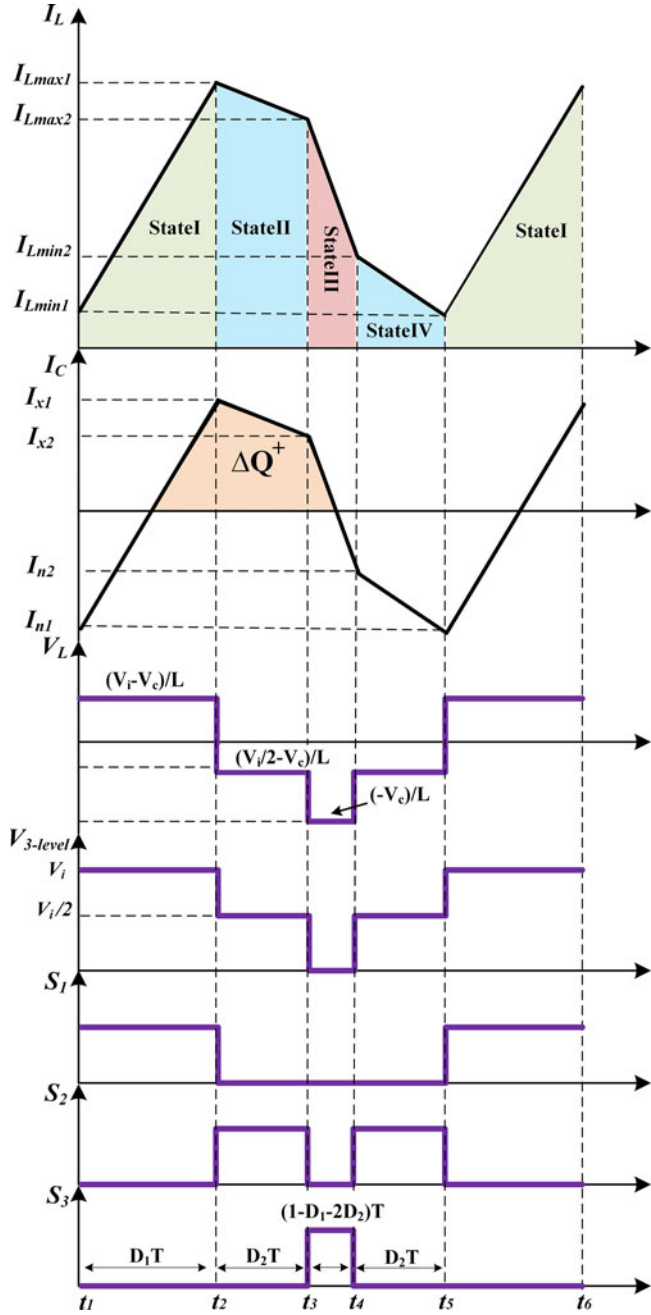
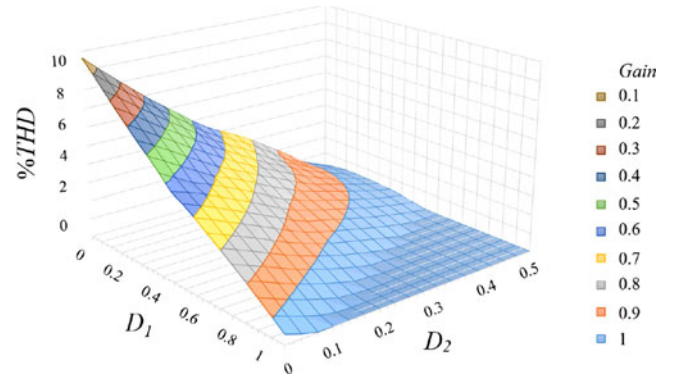Fig. 4. Inductor current, inductor voltage, and the output voltage waveforms during two consequent switching cycles of S_2.

Fig. 5. THD variations as a function of duty ratios.

$$V_{rk} = \frac{V_{p-p}}{4n\pi} \left([\sin(2\pi n(D_1 + D_2)) - \sin(2\pi nD_2) \right.$$
$$+ \sin(2\pi n(D_1 + 2D_2))]^2 + [\cos(2\pi nD_2)$$
$$- \cos(2\pi n(D_1 + D_2))$$
$$\left. - \cos(2\pi n(D_1 + 2D_2)) + 1]^2 \right)^{1/2}. \quad (18)$$

Since $\omega_s \gg \omega$, then, (16) and (17) are approximated as

$$X_{\text{cfs}} \approx \frac{1}{k\omega_s C} \quad (19)$$

$$X_{\text{Lfs}} \approx k\omega_s L \quad (20)$$

also

$$X_{\text{Lfs}} \gg R \gg X_{\text{cfs}}$$

then

$$I_s = \frac{V_o I_o}{V_i \eta} V_{\text{ok}} \approx \left(\frac{X_{\text{cfs}}}{X_{\text{Lfs}}} \right) V_{\text{rk}} \quad (21)$$

and, finally, one has

$$V_{\text{ok}} \approx \left(\frac{X_{\text{cfs}} V_{p-p}}{X_{\text{Lfs}} 4n\pi} \right) \left([\sin(2\pi n(D_1 + D_2)) - \sin(2\pi nD_2) \right.$$
$$+ \sin(2\pi n(D_1 + 2D_2))]^2 + [\cos(2\pi nD_2)$$
$$- \cos(2\pi n(D_1 + D_2))$$
$$\left. - \cos(2\pi n(D_1 + 2D_2)) + 1]^2 \right)^{1/2}. \quad (22)$$

Now, it is possible to calculate the THD, which is reported in (23), shown at the bottom of this page.

According to (23), the THD of the output voltage is related to D_1, D_2, L, and C. The load does not appear in the THD equation. Fig. 5 shows the THD variations as a function of duty cycles of switches for specific values of filter parameters.

where

$$X_{\text{cfs}} = \frac{1}{(k\omega_s \pm \omega)C} \quad (16)$$

$$X_{\text{Lfs}} = (k\omega_s \pm \omega)L \quad (17)$$

$$\%\text{THD}_v = \left(\frac{100}{(D_1 + D_2)4\pi} \right) \left(\sum_{n=1}^{\infty} \left(\frac{X_{\text{cfs}}}{X_{\text{Lfs}}} \right)^2 \times \left(\frac{[\sin(2\pi n(D_1 + D_2)) - \sin(2\pi nD_2) + \sin(2\pi n(D_1 + 2D_2))]^2}{n^2} \right) \right.$$
$$\left. + \left(\frac{[\cos(2\pi nD_2) - \cos(2\pi n(D_1 + D_2)) - \cos(2\pi n(D_1 + 2D_2)) + 1]^2}{n^2} \right) \right)^{1/2} \quad (23)$$

TABLE II
POSSIBLE VARIATION RANGES OF DUTY RATIOS

GAIN < 0.5	GAIN > 0.5
$0 < D_2 < 0.5$	$0 < D_2 < 0.5$
$0 < D_1 < 0.5$	$D_{1\min} < D_1 < D_{1\max}$ $D_{1\min} = \text{Gain} - D_{2\max}$ $D_{1\max} = \text{Gain} - D_{2\min}$

V. PARAMETER DESIGN

Design specifications of the three-level ac/ac converter are defined as following: the input voltage V_i is 110 V, the power supply frequency is 60 Hz, the output voltage V_o is 80 V, and the switching frequency is 10 kHz.

A. Duty Cycles

The fundamental relations for the proposed converter are

$$D_1 + D_2 = \text{Gain} \tag{24}$$

$$D_1 + 2D_2 < 1. \tag{25}$$

An exact evaluation of (24) and (25) reveals the possible variation ranges of duty ratios as summarized in Table II.

B. AC-Link Voltage Dividing Capacitors and Input Inductive Filter

In this paper, the main goal is to optimize the output voltage quality by minimizing its THD. To achieve this aim, the capacitors in the ac link should be large enough to provide required energy during each state to let neglect the voltage variations during each switching period. This is a fundamental assumption in deriving the THD formulation, which is then used to obtain the optimized switch-on times (duty ratios). If the values of capacitors are selected small, then the result of optimization problem is not accurate and the THD of the output voltage increases. Therefore, with the comparatively large capacitors in the ac link, the power factor with a resistive load may be low leading. In our application, the value of input filter inductor is determined from the required switching noise attenuation. If a higher power factor is intended, one can increase the input filter inductance, at the price of increased volume and losses. However, if the load is highly inductive, such as an induction motor, then the power factor at the input side is much higher.

C. Power Switch

Two important points to choose a power switch are the nominal current through the switch and the voltage across the switch when it is open. In this structure, the maximum voltage across each switch is equal to the input peak voltage. The switch current is given by the following equation:

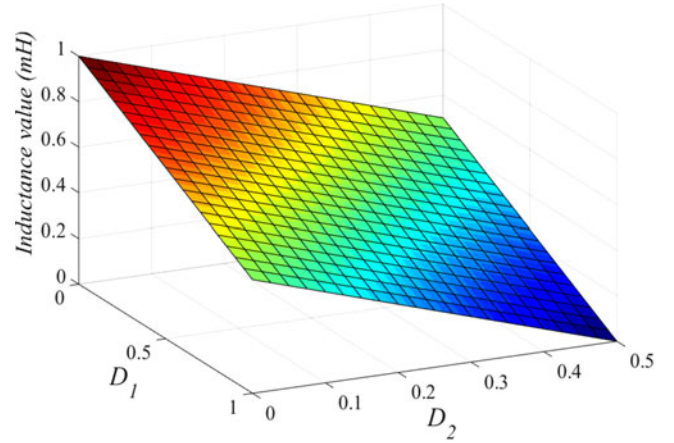$$I_s = \frac{V_o I_o}{V_i \eta}. \tag{26}$$

Fig. 6. Minimum required inductance as a function of duty ratios.

D. Inductor L for Energy Storage

By solving (1)–(3), the inductor currents of Fig. 4 are calculated as

$$I_{\min 1} = V_c \left[\frac{1}{RT(D_1 + D_2)(D_1 + 2D_2)} + \frac{D_1 T}{L} \right] - \frac{V_i D_1 T}{L} \tag{27}$$

$$I_{\min 2} = V_c \left[\frac{1}{RT(D_1 + D_2)(D_1 + 2D_2)} + \frac{(D_1 + 2D_2) T}{2L} \right] - \frac{V_i (D_1 + D_2) T}{2L} \tag{28}$$

$$I_{\max 1} = V_c \left[\frac{1}{RT(D_1 + D_2)(D_1 + 2D_2)} - \frac{D_1 T}{L} \right] + \frac{V_i D_1 T}{L} \tag{29}$$

$$I_{\max 2} = V_c \left[\frac{1}{RT(D_1 + D_2)(D_1 + 2D_2)} - \frac{(D_1 + 2D_2) T}{2L} \right] + \frac{V_i (D_1 + D_2) T}{2L}. \tag{30}$$

To ensure continuous-conduction mode (CCM) operation $I_{\min 1} > 0$, which leads to a minimum inductance value as

$$L = \frac{RT^2}{2} \left[(1 - D_1 - 2D_2)(D_1 + D_2)(D_1 + 2D_2) \right]. \tag{31}$$

Fig. 6 shows the inductance variations as a function of duty ratios. Accordingly, L is selected to be 1 mH. According to Section III, the proposed converter has four operation states that the inductance current variations during these states are shown in Fig. 4.

D. Capacitor C for Output Filtering

According to Fig. 4, the capacitor current is the ac part of the inductor current where

$$\begin{cases} I_{x1} = I_{L\max 1} - I_{\text{load}} \\ I_{x2} = I_{L\max 2} - I_{\text{load}} \\ I_{n1} = I_{L\min 1} - I_{\text{load}} \\ I_{n2} = I_{L\min 2} - I_{\text{load}} \end{cases} \tag{32}$$

TABLE III
COMPARISON AMONG THREE-LEVEL AC/AC CONVERTERS

Description	Proposed converter	Cell-based three level converter [23]	Cascaded multilevel converter [30]	Multilevel direct converter [31]
Number of switches	3	4	6	4
Number of diodes	0	0	12	0
Number of inductors (excluding the filters)	1	1	6	1
Number of capacitors (excluding the filters)	2 (100 μF)	1 (4.7 μF)	6 (2.2 μF)	1 (260 μF)
RC snubber	required	required	–	required
Voltage gain	$D_1 + D_2$	D	$3D$	D
Number of semiconductors conducting simultaneously	1	2	2	2
Isolation transformer	–	–	required	–
Extendibility to any n-levels	easy	impossible	hard	easy
Total blocking voltage	$5V_i/2$	$7V_i/2$	$6V_i$	$4V_i$
Total energy of capacitors (CV^2)	$50V_i^2$	$4.7\,V_i^2$	$3.3V_i^2$	$260\,V_i^2$
Applications	Regulated sinusoidal power supply, induction motor drive, dynamic voltage restorer	Regulated sinusoidal power supply, electronic transformer	Line conditioner reactive power compensator	STATCOM

and the capacitor voltage ripple depends on the area under the capacitor current waveform, which is defined as ΔQ and calculated as

$$\Delta Q = \left(\frac{T}{2}\right)\left(I_{L\max1}\left(\frac{D_1}{2} + D_2\right)\right.$$
$$\left. + I_{L\max2}\left(\frac{1-D_1}{2}\right) - I_{\text{Load}}\left(\frac{1+D_2}{2}\right)\right). \quad (33)$$

Consequently, the output voltage ripple can be concluded as follows, which lets decide the required capacitor to ensure the ripple is less than the desired value:

$$\Delta V = \frac{\Delta Q}{C}. \quad (34)$$

VI. COMPARATIVE ANALYSIS OF THE PROPOSED CONVERTER

Table III compares the proposed three-level converter with already available competitors from different aspects. According to Table III, the number of bidirectional switches is minimum for the proposed converter and no extra diode is also required that means the lowest total number of semiconductors compared to other topologies, which reduces the losses. The conduction loss of the proposed converter is lower because the number of semiconductors in each current path is only one device. The number of reactive elements is also less than two other converters and only the converter of [31] needs one less capacitor. The gain equation of the proposed converter has two degrees of freedom, in other words by proper determination of D_1 and D_2 not only the desired voltage gain is attained, but also some kind of optimization can be achieved. In this paper, the output voltage THD is minimized. Another considerable advantage of the proposed converter in comparison with other three-level ac choppers is the lower total blocking voltage. Finally, the proposed topology can be readily extended to any desired levels by readily adding one switch and one capacitor for each extra output voltage level.

One of the most important features for any topology is a reliable operation. The proposed converter has the minimum number of semiconductors to produce the same levels compared to other available topologies, which translates to lower total semiconductor failures. On the other hand, with the lowest number of semiconductors, what will happen if any semiconductor fails? If S_1 or S_2 fails, then the converter can still operate but the number of levels in the output voltage decreases from three to two. If S_3 fails then the worst possible case happens because if S_1 or S_2 are turned ON, then the input source will become short circuit. Compared to modular topologies, the proposed converter does not have the capability of fault-tolerant operation.

VII. OPTIMIZATION

In this paper, and to find the best values for the duty ratios in order to minimize the THD value of the output voltage, a genetics algorithms optimization is employed, where the THD equation of (23) is chosen as the fitness function, which is minimized subject to the following constraints:

$$\begin{cases} 0 < D_1 < 1 \\ 0 < D_2 < 0.5 \\ D_1 + 2D_2 < 1 \end{cases} \quad (35)$$

$$D_1 + D_2 = \text{Gain}. \quad (36)$$

The gain in (36) is defined as the output to the input voltage ratio. Fig. 7 shows that the proper selection of the duty ratios leads to a very small THD.

VIII. PERFORMANCE EVALUATION

The simulations are done in MATLAB/Simulink. The converter parameters are listed in Table IV. The THD values analytically derived from (23) are compared with the simulation results in Fig. 8, which are in good agreement.

To confirm the analytical and simulated achievements, experimental tests on a three-level ac/ac converter are also reported. Fig. 9 shows the prototype, which has the same parameters as
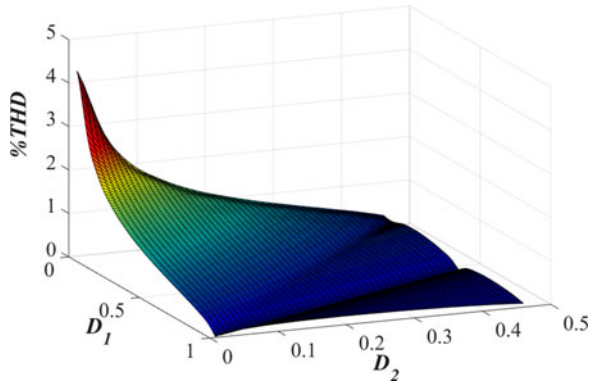
Fig. 7.   Total harmonics distortion as a function of duty ratios.

TABLE IV
SYSTEM PARAMETERS

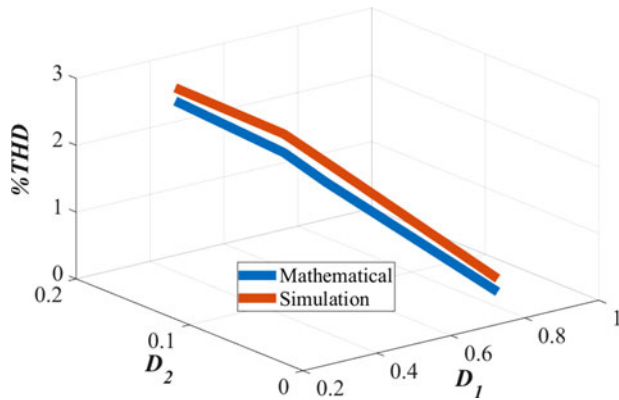| Parameter	Value
Input voltage (V_i)	110 V
Output voltage (V_o)	80 V
Supply frequency (f)	60 Hz
Switching frequency (f_s)	10 kHz
Converter inductance (L)	1 mH
Input filter inductance (L_f)	1.2 mH
Output capacitance filter (C)	5 μF

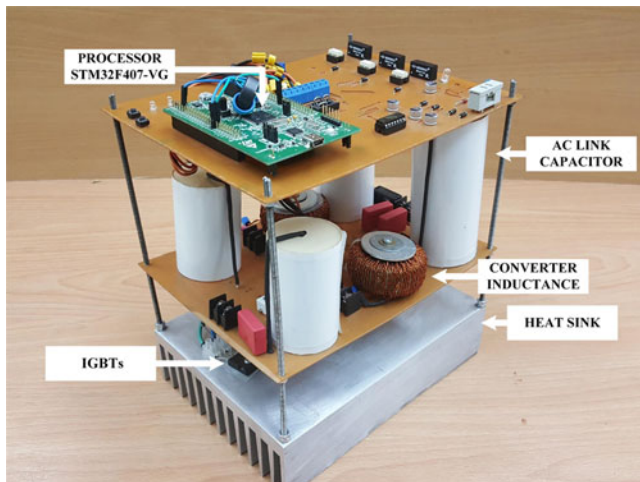

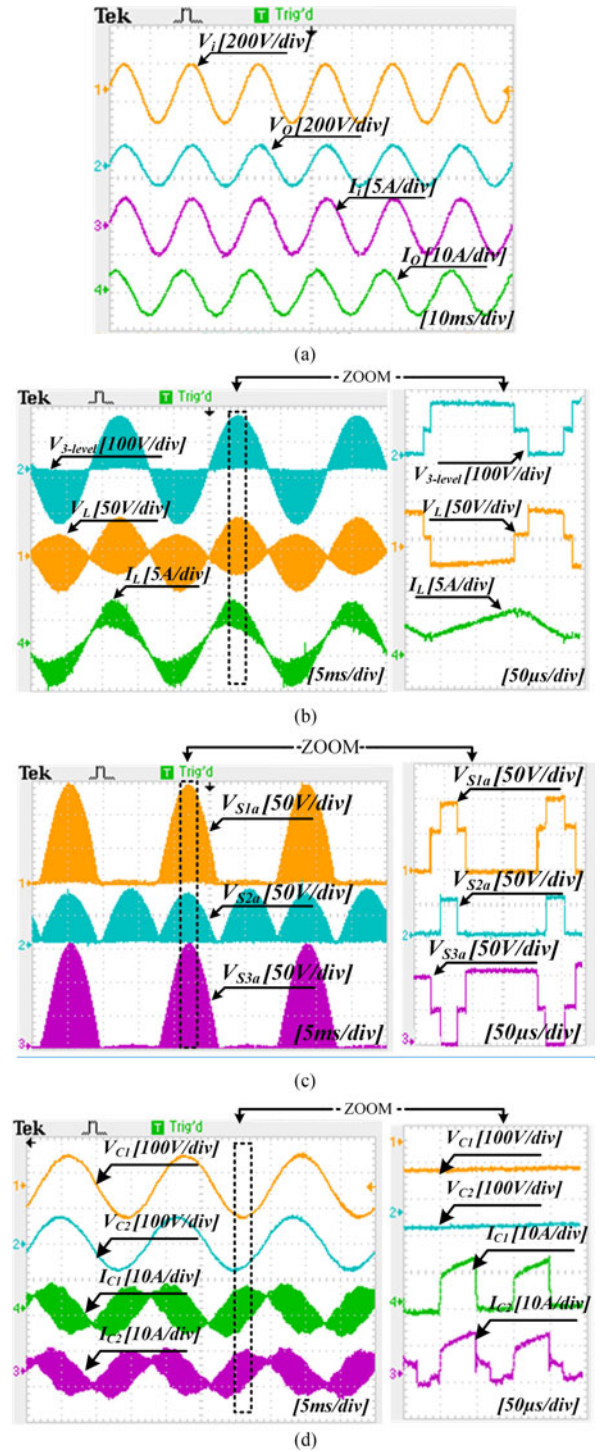Fig. 8.   Simulation and analytical results of THD.

Fig. 9.   Prototype picture.

Fig. 10.   Experimental results under resistive load (10 Ω): (a) input and output waveforms, (b) inductor waveforms and three-level voltage, (c) blocked voltages by S_{1a}, S_{2a}, and S_{3a}, and (d) voltages and currents of ac-link capacitors.

the simulations. The experimental waveforms under the same test conditions as simulations are reported in Fig. 10. The simulated waveforms are summarized in Fig. 11. The output voltage waveform is highly sinusoidal, with THD $= 1.45\%$. In this test, $D_1 = 0.6$ and $D_2 = 0.2$.
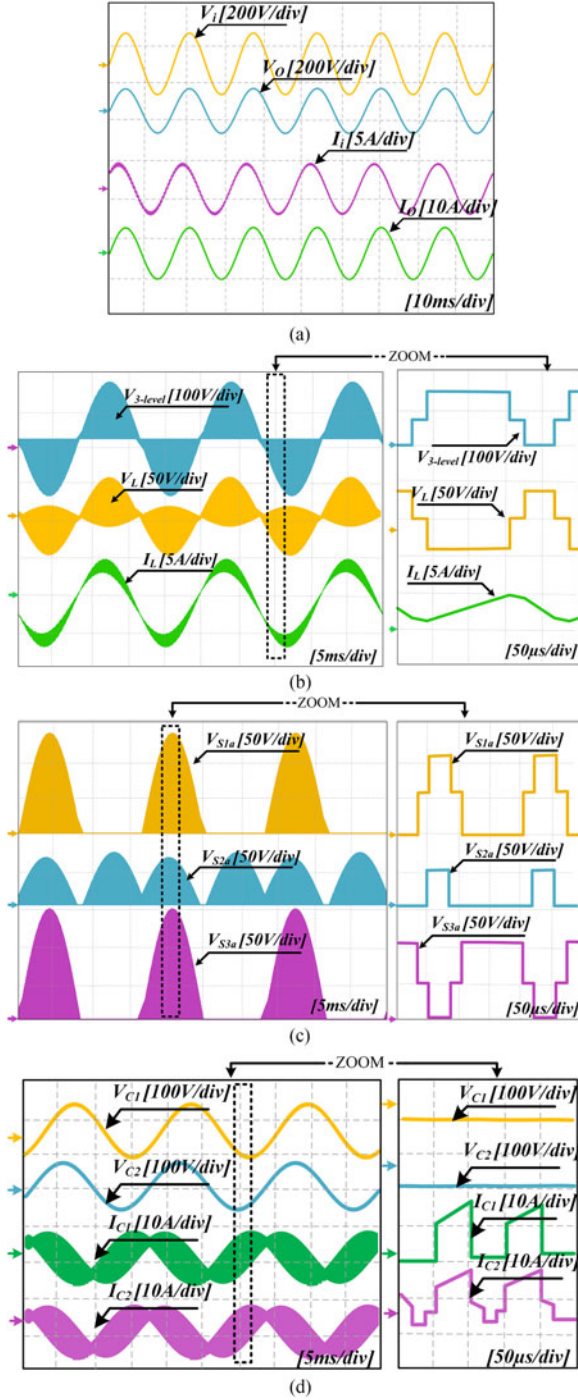
(a)

Fig. 12. Experimental output waveforms under (a) capacitive load ($R = 20\,\Omega$ and $C = 50\,\mu$F) and (b) inductive load ($R = 6.5\,\Omega$ and $L = 20$ mH).

current (I_i), and the output current (I_o), are all highly sinusoidal waveforms, as the THD of the input and the output currents are 4.5% and 1.7%, respectively, in the experiments.

Figs. 10(b) and 11(b) show the current and voltage waveforms of the inductor and the three-level output voltage of the converter, with a zoomed view at the peak of sinusoid. Accordingly, the minimum inductor current is higher than zero, which means that the CCM operation is achieved ($I_{\min2} > 0$). Also, the three-level voltage waveforms at the output of the converter and across the filter inductor are in accordance to the expected waveforms, already defined in Fig. 4. The output voltage waveform has three levels as V_i, $V_i/2$, and 0.

The blocked voltages by the switches S_{1a}, S_{2a}, and S_{3a} (see Fig. 2) are plotted in Figs. 10(c) and 11(c). It can be seen that the peak reverse voltages on S_{1a} and S_{3a} are equal to the source peak voltage, while S_{2a} just blocks half of the source peak voltage. Fig. 12 shows the waveforms of the output voltage and current under capacitive ($R = 20\,\Omega, C = 50\,\mu$F) and inductive ($R = 6.5\,\Omega$, $L = 20$ mH) loading conditions, respectively.

The output power factor for the capacitive and inductive loads are PF $= 0.35$ (lead) and PF $= 0.46$ (lag), respectively. The THD values of the output voltage and current are $\text{THD}_{Io} = 4.25\%$, $\text{THD}_{Vo} = 2.97\%$ and $\text{THD}_{Io} = 4.48\%$, $\text{THD}_{Vo} = 2.36\%$, respectively.

As already mentioned and is clear in Fig. 12, with a highly inductive load, the input power factor is close to unity.

The transient performance of the converter in response to step changes of input voltage, reference voltage, and load is examined and the experimental results are shown in Fig. 13. The proposed converter system presents a smooth and fast response in all cases, as the transients diminish in less than a quarter of cycle without experiencing considerable over or undershoots.

Finally, the conversion efficiency versus the output load has been shown in Fig. 14 for the fixed output voltage of 80 V and the input voltages equal to its nominal as well as 0.9 and 1.1 of the nominal. Clearly, the efficiency in a wide range of output powers is more than 91%, which is a result of low conduction losses, because in each state only one switch conducts.

Fig. 11. Simulation results under resistive load (10 Ω): (a) input and output waveforms, (b) inductor waveforms and three-level voltage, (c) blocked voltages by S_{1a}, S_{2a}, and S_{3a}, and (d) voltages and currents of ac-link capacitors.

Figs. 10 and 11 show the good operation of the converter in the steady state and also indicate the agreement between simulation and experimental results. Figs. 10(a) and 11(a) show the input voltage (V_i) with 60-Hz frequency, which is fed to the ac/ac converter. Clearly, the output voltage (V_o), the input
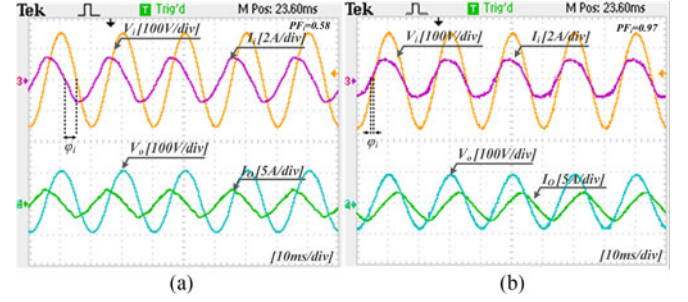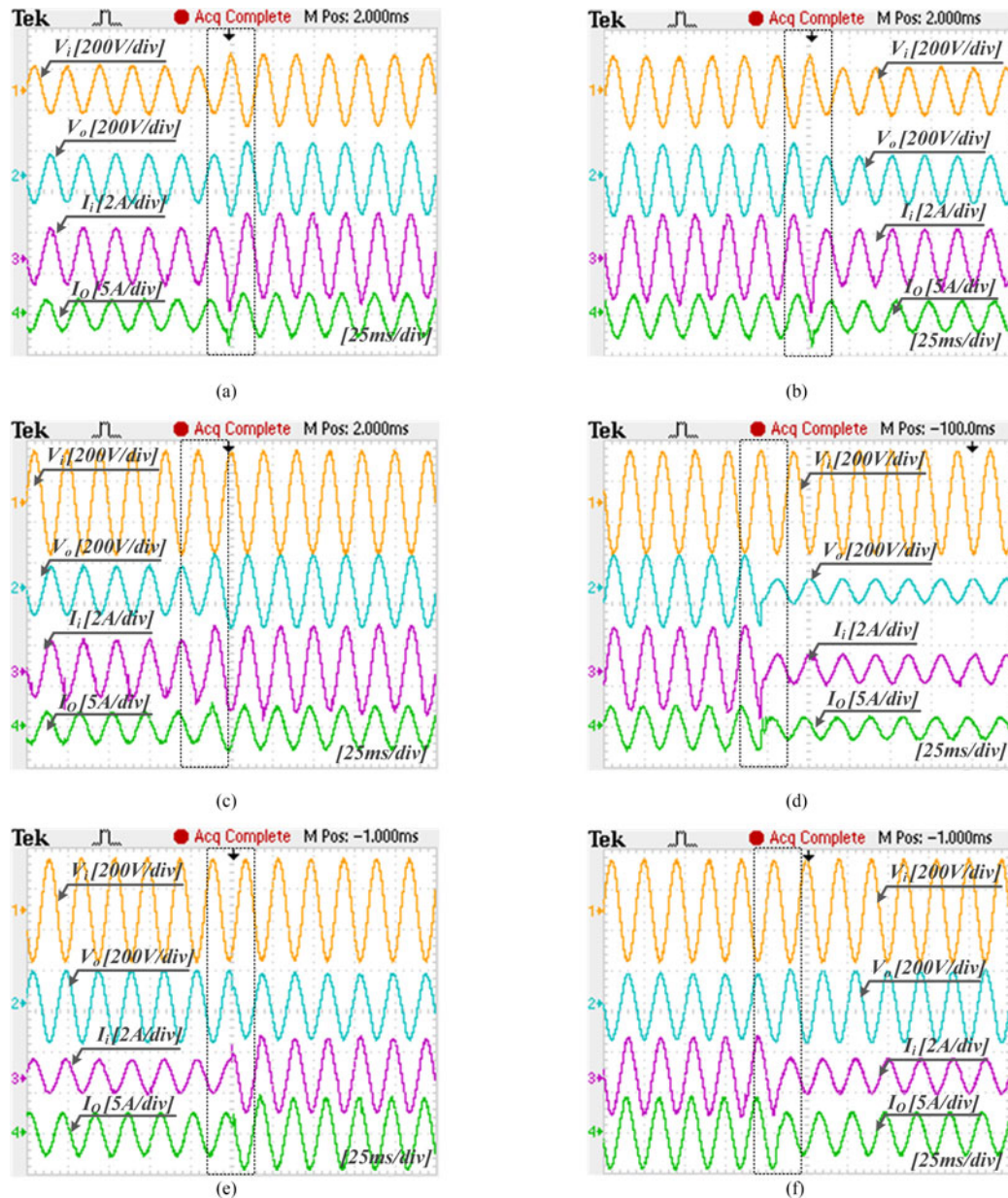
Fig. 13. Experimental transient waveforms in response to step-up and -down of (a), (b) input voltage amplitude, (c), (d) reference voltage amplitude, and (e), (f) load.
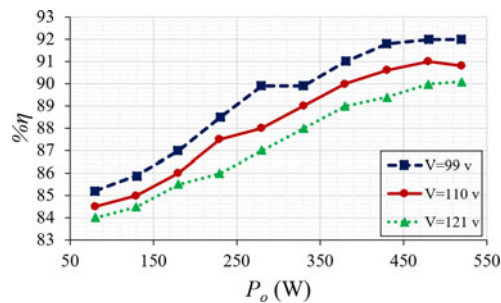

Fig. 14. Efficiency versus the resistive load power at three different input voltages and a fixed output voltage.

IX. CONCLUSION

A novel single-phase PWM controlled ac to ac converter is proposed in this paper that takes benefit of a reduced number of switches compared to other competitors. The output voltage equation is derived and is used to optimize the output voltage THD by proper selection of duty ratios. Briefly, the proposed converter along with the proposed control scheme offers the following advantages:

1) the ability to be readily extended to any desired level by just adding a capacitor and a switch for one-step level increase;
2) simple topology and control algorithm;
3) minimum conduction losses, because in each state only one semiconductor conducts;
4) low-voltage stress on the middle switches.

This paper also describes the converter design and the controller tuning of a prototype of 460 W, 110 V, 60 Hz to 80 V. Experimental results provided confirm the proper operation of the multilevel ac/ac converter under different loading conditions.

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