Series and Tapped Switched-Coupled-Inductors Impedance Networks

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***Abstract*—A new class of impedance networks is proposed in this paper. The proposed coupled-inductors-based impedance cells, called the series and the tapped switched-coupled-inductors, are employed within the (quasi) switched boost networks. The achieved impedance networks based on the proposed cells offer very high conversion gains with less-than-unity turn ratios ($n < 1$), which simplifies the realization of the magnetic element and at the same time reduces the number and size of passive components. The high boosting capability is achieved with small shoot-through durations that bring some additional advantages, such as low ratings of switching devices. The circuit analysis and operation concepts as well as a design procedure for the components of the proposed impedance networks are presented. Theoretical achievements are confirmed through experiments on a 220 W dc–dc converter laboratory setup.**

***Index Terms*—Coupled-inductors, high-gain, impedance network, shoot-through (ST).**

I. Introduction

THE pulsewidth modulated voltage/current-source converters (VSCs/CSCs), are widely used in many applications, such as adjustable speed drives, renewable energy systems and electric vehicles. Both VSCs and CSCs can suffer from reliability problems, known as possible input voltage short circuit (in VSCs) or input current open circuit (in CSCs) caused by electromagnetic interference noises or mismatches of gating pulses. Besides, in applications where the simultaneous buck–boost operation is required, multistage power conversion with the traditional CSC or VSC is unavoidable, which results in a higher system cost, volume, weight, and lower efficiency [1]. To overcome these drawbacks, a new type of converter called the Z-source converter (ZSC) has been already proposed that is formed of an X-shaped network of two inductors and two capacitors preceding the main switching stage [2]. In a voltage-fed X-shaped Z-source inverter (ZSI), short circuiting the bridge arms, which is called the shoot-through (ST) is not anymore a concern. With proper selection of the ST duration, the output voltage of the ZSI can be increased to a desired magnitude, with respect to the input. Also, without the ST state in a ZSI, the voltage buck operation of the inverter is possible as conventional. Thus, a wide range of the buck-boost output voltage gains is achieved for a ZSI. Therefore, the single-stage buck–boost voltage inversion with higher reliability and improved output voltage quality due to the elimination of the dead-times is obtained. Recently, several ac–dc, dc–ac, dc–dc, and ac–ac converters along with the proper control and modulation techniques are proposed, which utilize different topologies of Z-source impedance networks (ZSNs) in their circuits [3]–[14].

The traditional ZSN has some limitations, mainly known as high component stresses, high inrush currents, several passive elements, and lack of a common ground between the input source and the switching stage [2]. In order to alleviate these problems, various ZSNs have been recently introduced. For instance, by effectively employing a diode and a controlled switch instead of a capacitor and an inductor of the traditional X-shaped ZSN, the (quasi) switched boost networks, (q)SBNs, can produce the same voltage gain with the reduced number of passive components and better efficiency [15]–[17]. The qSBN topology is even more improved by utilizing the switched-inductors (SL) network leading to the actively switched capacitor/switched inductor quasi Z-source network (ASC/SL-qZSN) [18], [19]. However, the maximum voltage gain of these impedance networks is practically limited due to a high ST duty cycle requirement, which is a major restriction in many applications requiring high-voltage conversion gains. Lately, the coupled-inductors-based impedance networks are proposed, which offer higher gains with shorter ST durations and reduce the number as well as the size of passive components. Some of successful implementations are the trans Z-source [20], the TZ-source [21], and the improved trans Z-source [22], which utilize the turn ratio of transformer windings to increase the voltage gain, while offering continuous input current and lower voltage stresses. The magnetically coupled impedance networks such as the Γ-source [5], the A-source [12], the Y-source [10], and the Δ-source [23] are also well-known impedance networks that employ coupled-inductors with lower number of components and the same voltage boosting capabilities compared to their transformer-based counterparts. Recently, the SCL-qZSN was introduced in [24], which offers high gains with the turn ratios as low as unity at the price of increased number of circuit components through combining the switched-coupled-inductors (SCL) and the switched-capacitors. The lower turn ra-

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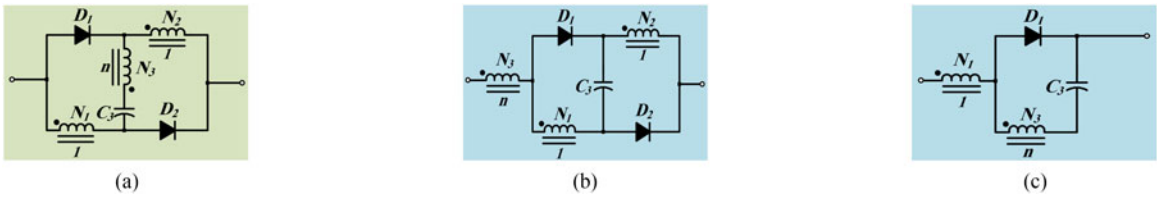

Fig. 1. (a) Conventional switched-coupled-inductors (SCL) [24]. (b) Proposed series switched-coupled-inductors (SSCL). (c) Proposed tapped switched-coupled-inductors (TSCL) impedance cell.

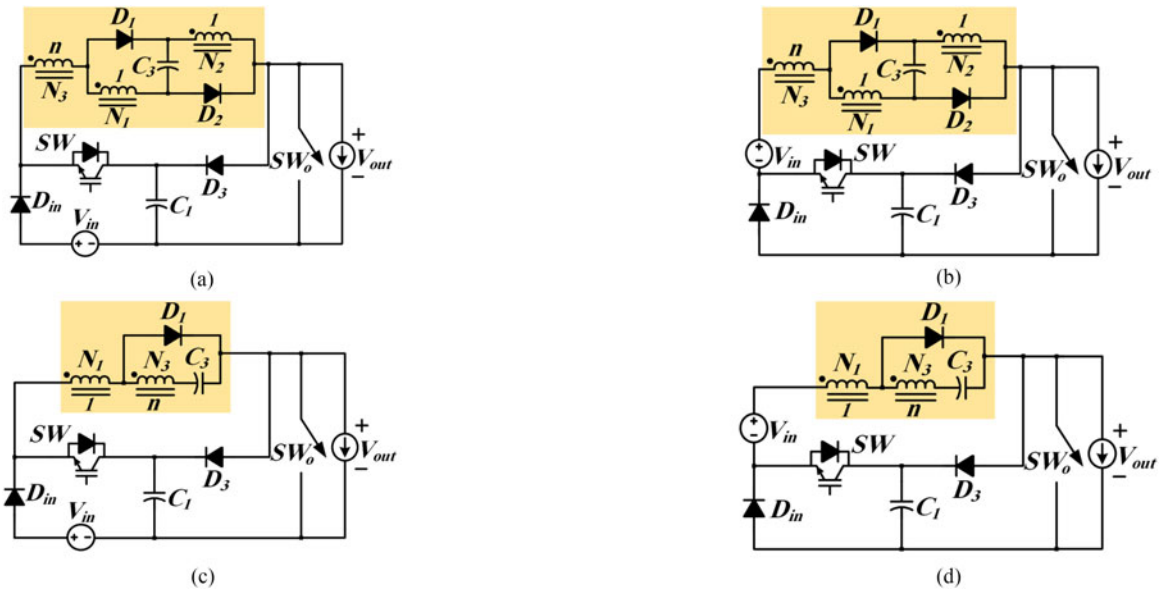

Fig. 2. Proposed impedance networks. (a) SSCL-SBN. (b) SSCL-qSBN. (c) TSCL-SBN. (d) TSCL-qSBN.

tio of the coupled-inductors translates to ease of magnetic circuit realization.

In this paper, a class of very high step-up gain impedance networks is proposed, which employs the coupled-inductors within the (q)SBN topologies. All proposed impedance networks can highly increase the output voltage with less-than-unity turn ratios ($n < 1$), while requiring very short ST durations. Consequently, the ST stresses are reduced. Despite offering a high gain performance, the number and size of energy storage elements are minimum for the proposed class of ZSNs. The operation principles of the proposed impedance networks are theoretically derived and experimentally confirmed in a dc–dc prototype converter. However, for the dc–dc conversion, there are other schemes like high boosting gain dc–dc converters already proposed in [25]–[27]. It should be noted that these topologies are suggested only for dc–dc conversion, while the proposed class of impedance networks in this paper can be readily employed for all types of conversion.

II. Proposed Impedance Networks

A. Topology Derivation

Fig. 1(a) shows the successful SCL impedance cell [24]. Due to employing the capacitor voltage boosting ability within the coupled-inductors structure, this impedance cell offers high step-up gains with winding turn ratios as low as unity ($n = 1$). Obtaining the same high step-up performance with a coupled-inductors-based impedance cell with turn ratios less-than-unity is of interest in order to reduce the size of the magnetic circuit and simplify its implementation. Considering this purpose, two modified impedance cells, shown in Fig. 1(b) and (c), are proposed. As observed from Fig. 1(b), the winding N_3 is moved and placed in series with the main cell compared to the SCL, thus named series switched-coupled-inductors (SSCL). Also, as shown in Fig. 1(c), the winding N_1 is in series with the simplified cell, where the winding N_2 and the diode D_2 are removed from the original circuit of Fig. 1(a). It is called tapped switched-coupled-inductors (TSCL). The proposed impedance cells are utilized within the SBN and the qSBN, the main switching circuits of [15] and [16], resulting to the impedance networks shown in Fig. 2(a)–(d). As these figures show, the SBN and the qSBN realizations only differ in the position of the input voltage source. A common ground between the input and the output can be recognized as an advantage of the SBN-based topologies compared to the qSBN-based ones. The principle of performance and detailed comparison of features are thoroughly investigated in the following of the paper.

B. Performance Analysis

Similar to all of the ZSCs, the proposed topologies have two states of operations, i.e., ST and non-shoot-through (non-ST).

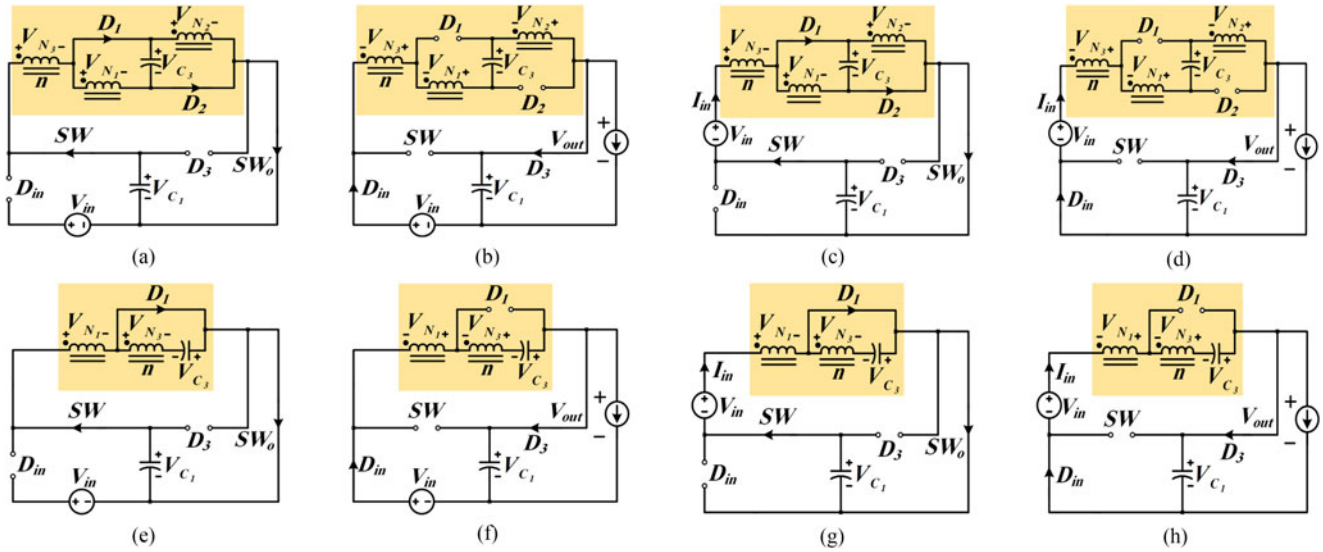

Fig. 3. Operating states. (a) ST and (b) non-ST of SSCL-SBN. (c) ST and (d) non-ST of SSCL-qSBN. (e) ST and (f) non-ST of TSCL-SBN. (g) ST and (h) non-ST of TSCL-qSBN.

The equivalent circuits of the proposed topologies in the ST and non-ST states are shown in Fig. 3 and analyzed in the following.

1) SSCL-SBN: The first proposed impedance network is depicted in Fig. 2(a) and the operation states are explained hereafter.

a) ST state: In this state, the switches SW and SW_o conduct simultaneously, as shown in Fig. 3(a). Moreover, diodes D_1 and D_2 are forward biased and thus conduct, while diodes D_{in} and D_3 are blocked. Therefore, the capacitor C_1 discharges its energy into the coupled-inductors and the capacitor C_3. The voltage equations are

$$\begin{cases} V_{N_1} + V_{N_3} = V_{C_1} \\ V_{N_3} = nV_{N_1} = nV_{N_2} \\ V_{N_1} = V_{C_3} \end{cases}. \tag{1}$$

b) Non-ST state: Both switches SW and SW_o are turned OFF and the diodes D_{in} and D_3 are conducting, while diodes D_1 and D_2 are blocked, as shown in Fig. 3(b). In addition, the diode D_3 provides a path for charging current of the capacitor C_1. The voltage equations are

$$\begin{cases} V_{N_1} + V_{N_2} + V_{N_3} = V_{C_1} - V_{C_3} - V_{\text{in}} \\ V_{N_3} = nV_{N_1} = nV_{N_2} \\ V_{C_1} = V_{\text{out}} \end{cases}. \tag{2}$$

By applying the volt-second balance on winding N_1, the steady-state output voltage equation of the SSCL-SBN is obtained from (1) and (2) as follows, in which, D is the ST duty-cycle:

$$V_{\text{out}} = \frac{\left(1+\frac{1}{n}\right)(1-D)}{1-\left(2\left(1+\frac{1}{n}\right)\right)D} V_{\text{in}}. \tag{3}$$

2) SSCL-qSBN: This converter is shown in Fig. 2(b) and its performance is similar to the SSCL-SBN with the only difference in the configuration that the voltage source is connected in series with the capacitor C_1 in the ST state.

a) ST state: This state is shown in Fig. 3(c). Readily one can write

$$\begin{cases} V_{N_1} + V_{N_3} = V_{C_1} + V_{\text{in}} \\ V_{N_3} = nV_{N_1} = nV_{N_2} \\ V_{N_1} = V_{C_3} \end{cases}. \tag{4}$$

b) Non-ST state: The voltage equations are exactly the same as (2) for this state shown in Fig. 3(d), and thus the volt-second balance results in

$$V_{\text{out}} = \frac{\left(1+\frac{2}{n}\right)}{1-\left(2\left(1+\frac{1}{n}\right)\right)D} V_{\text{in}}. \tag{5}$$

3) TSCL-SBN: The third proposed converter is shown in Fig. 2(c) and its operation is analyzed during the ST and non-ST states.

a) ST state: This state is shown in Fig. 3(e). The diode D_{in} disconnects the voltage source, while D_3 is blocked and D_1 is forward biased. The charging current of the TSCL cell flows through the conducting switches SW and SW_o. Under this condition, the voltage equations are

$$\begin{cases} V_{N_1} = V_{C_1} \\ V_{N_3} = nV_{N_1} = V_{C_3} \end{cases}. \tag{6}$$

b) Non-ST state: As indicated in Fig. 3(f), the input current flows through the series-connected TSCL cell windings N_1 and N_3 and the capacitor C_3. This current supplies the load and at the same time charges the capacitor C_1. The voltage equations are

$$\begin{cases} V_{N_1} + V_{N_3} = V_{C_1} - V_{C_3} - V_{\text{in}} \\ V_{N_3} = nV_{N_1} \\ V_{C_1} = V_{\text{out}} \end{cases}. \tag{7}$$

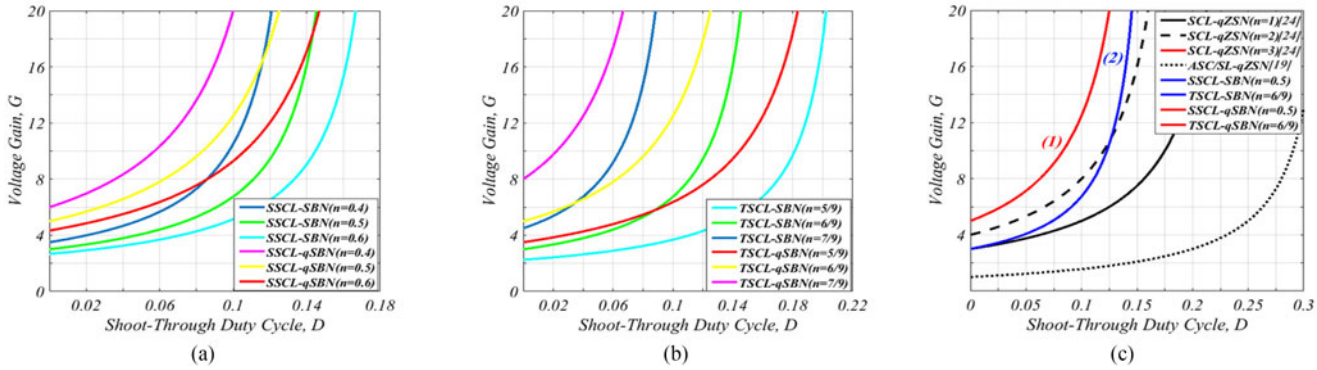

Fig. 4. Voltage gains of the proposed (a) SSCL- and (b) TSCL-based impedance networks versus the ST duty cycle (*D*). (c) Comparative gain plot.

With the volt-second balance, the output voltage equation of the TSCL-SBN is obtained as

$$V_{\text{out}} = \frac{(1-D)}{(1-n)-2D} V_{\text{in}}. \tag{8}$$

4) TSCL-qSBN: The impedance network configuration is plotted in Fig. 2(d), and the equivalent circuits during the ST and non-ST states are presented in Fig. 3(g) and (h), respectively. Following a similar procedure, the converter output voltage can be simply calculated as

$$V_{\text{out}} = \frac{(1+n)}{(1-n)-2D} V_{\text{in}}. \tag{9}$$

Fig. 4(a) and (b) are plotted based on the steady-state gain equations already derived in (3), (5), (8), and (9), in which *G* is the amplitude ratio of the output to the input voltage. As shown in these figures, with the turn ratios less-than-unity, very high step-up gains are achieved. Besides, the more the turn ratio (*n*) decreases from one, the higher the voltage gain becomes for the SSCL-(q)SBN, which can be characterized as a positive feature for these converters. On contrary, for the TSCL-(q)SBN, closer turn ratios to unity result in higher voltage gains. As a comparative gain analysis, Fig. 4(c) represents the voltage gain curves of the SCL-qZSN [24], the ASC/SL-qZSN [19], and the proposed impedance networks. Obviously, the proposed qSBN-based topologies can achieve the same very high gains as the SCL-qZSN [24] with the turn ratio being much lower ($n < 1$) and both aforementioned topologies offer much higher gains than the ASC/SL-qZSN [19]. As shown in this figure, to plot the voltage gain curve labeled as (1), $n = 3$ is needed for the SCL-qZSN [24] and also $n = 0.5$ and 6/9 are required for the SSCL-qSBN and the TSCL-qSBN, respectively. On the other hand, by properly selecting the turn ratio (*n*) for the proposed SBN-based topologies, a much smaller change in the ST duty cycle value can considerably change the voltage gain of these converters in comparison with the SCL-qZSN [24], which is clear from the curve labeled as (2) in Fig. 4(c).

III. Component Parameters Design and Comparison

This section is considered to design the passive component parameters of the proposed impedance networks and compare the results with some competitors.

A. Passive Components Design

1) Magnetizing Inductance: In order to achieve the tolerable magnetizing current ripple, the required magnetizing inductance is calculated based on the following equation, which has been used as a design constraint:

$$\Delta i_m = \frac{V_{N1} DT}{L_m}. \tag{10}$$

In (10), V_{N1}, *T*, and L_m are the voltage across winding N_1 during the ST state, the switching period, and the magnetizing inductance, respectively. Accordingly, by introducing $\alpha\%$ as the percent of magnetizing current regarded as its ripple magnitude, the value of L_m can be obtained as

$$L_m = \frac{V_{N1} DT}{\alpha\% I_m}. \tag{11}$$

In the following equations, the value of magnetizing inductance is calculated for the proposed converters:

$$L_m^{\text{SSCL-SBN}} = \frac{G^2((G-1)n-1)}{(1+n)^3(2G-1)^2} \times L_m^B \tag{12}$$

$$L_m^{\text{SSCL-qSBN}} = \frac{(G+1)(Gn-2-n)}{2G(1+n)^3} \times L_m^B \tag{13}$$

$$L_m^{\text{TSCL-SBN}} = \frac{G^2(G(1-n)-1)}{(2G-1)^2} \times L_m^B \tag{14}$$

$$L_m^{\text{TSCL-qSBN}} = \frac{(G+1)(G(1-n)-1-n)}{2G} \times L_m^B. \tag{15}$$

In the above-mentioned equations, *G* is the voltage gain from (3), (5), (8), and (9), *n* is the turn ratio and

$$L_m^B = \frac{V_{\text{in}}^2 T}{\alpha\% P_o} \tag{16}$$

where P_o and V_{in} are the rated output power and the input voltage, respectively.

2) Capacitors: The voltage ripple of the capacitors C_1 and C_3 are imposed by the duration and the amplitude of the current flowing through them, characterized by the following equation, in which I_C is the ST current through the capacitor:

$$\Delta V_C = \frac{I_C DT}{C}. \tag{17}$$

TABLE I
NUMBER OF PASSIVE AND ACTIVE COMPONENTS COMPARISON

Component Type		Number of Components in the Networks				
		SCL-qZSN [24]	ASC/SL-qZSN [19]	DC-DC Converter in [25]	Proposed SSCL-(q)SBN	Proposed TSCL-(q)SBN
Number of passive components	Inductors	1 inductor and 3 coupled-inductors (2 magnetic elements)	2 inductors (2 magnetic elements)	2 coupled-inductors (1 magnetic element)	3 coupled-inductors (1 magnetic element)	2 coupled-inductors (1 magnetic element)
	Capacitors	3	1	4	2	2
Number of active components	Switches	0	1	2	1	1
	Diodes	3	5	1	4	3

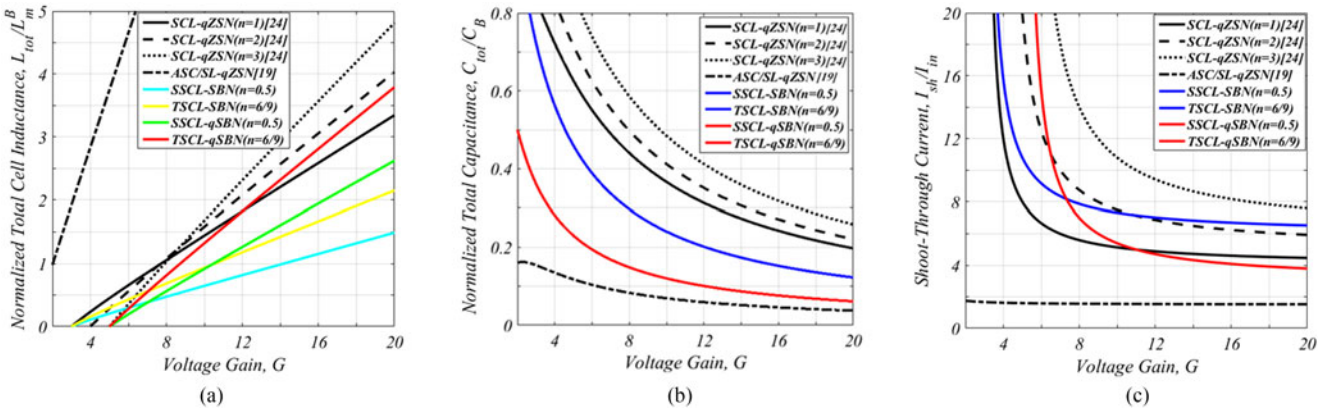

Fig. 5. Requirements comparison. (a) Normalized total cell inductance. (b) Total capacitance. (c) Normalized shoot-through current.

By supposing $\beta\%$ as the acceptable capacitor voltage ripple, the following equations define the required capacitances for the proposed impedance networks:

$$C_1^{\text{(S/T)SCL - SBN}} = 2 \times C_1^{\text{(S/T)SCL-qSBN}} = \frac{G-1}{G^2} \times C_B \tag{18}$$

$$C_3^{\text{SSCL-SBN}} = 2 \times C_3^{\text{SSCL-qSBN}} = \frac{(1+n)}{G} \times C_B \tag{19}$$

$$C_3^{\text{TSCL-SBN}} = 2 \times C_3^{\text{TSCL-qSBN}} = \frac{1}{nG} \times C_B \tag{20}$$

where

$$C_B = \frac{P_o T}{\beta\% V_{\text{in}}^2}. \tag{21}$$

B. Components Requirements Comparison

The inductors and the capacitors are important parts of any impedance network circuit that mainly determine the converter volume and cost. In order to make a quantitative comparison among the proposed impedance networks, the SCL-qZSN, the ASC/SL-qZSN, the number of circuit elements only in impedance networks and the normalized required total cell inductance (L_{tot}) and capacitance (C_{tot}) for each impedance network are calculated and the results are summarized in Table I and Fig. 5, respectively. Also, the high boosting dc–dc converter of [25], as a successful traditional solution, is considered for comparison in Table I. According to Table I, the number of energy storage components, including magnetic elements and capacitors, is minimum for the proposed class of converters. For the sake of a fair comparison, the results of Fig. 5 are obtained and analyzed considering the gain curves shown in Fig. 4(c), also the output power, the input voltage, and the voltage gain are the same for all cases.

1) Total Inductance: By using the magnetizing inductance equations (12)–(15) and normalizing the results based on (16), the normalized required total cell inductances (L_{tot}) is calculated for the proposed impedance networks. The results are plotted in Fig. 5(a). The same procedure has been done for the other topologies. It should be noted that L_{tot} is calculated by considering only the cell inductors of all topologies. The normalized required total cell inductances (L_{tot}) are derived assuming the same current ripple. As observed from Fig. 5(a), all four proposed impedance networks need much lower total cell inductances compared to the ASC/SL-qZSN. Also, due to the same voltage gain of the proposed qSBN-based topologies and the SCL-qZSN with $n = 3$ [see Fig. 4(c)], they are compared in Fig. 5(a). Obviously, from this figure, the required total cell inductances of the proposed qSBN-based topologies are much lower than those of the SCL-qZSN with $n = 3$. In addition, the L_{tot} parameter is significantly lower for the proposed SBN-based topologies compared to the SCL-qZSN with $n = 1$, as shown in Fig. 5(a). Thus, according to Fig. 4(c), the proposed SBN-based topologies advantageously offer higher voltage gains with $n < 1$ than SCL-qZSN with $n = 1$ while requiring much lower total cell inductance (L_{tot}).

2) Total Capacitance: To calculate the required total capacitances, the voltage ripple percent of capacitors is considered to be the same. The sum of required capacitance for each

TABLE II
COMPARISON OF THE PROPOSED IMPEDANCE NETWORKS

Converter	Pros & Cons	Duty cycle (D)	Switch/Diode blocking voltage (V_B)	Shoot-through current** (I_{sh})	Magnetizing current (I_m)
SSCL-SBN	+ simple and small magnetic element ($n<1$) + low total capacitance value + low shoot-through current + input and output common grounded − discontinuous input current − need for one active switch	$\frac{(G-1)n-1}{(1+n)(2G-1)}$	$V_{D1,2}=\frac{(2G-1)}{(2+n)}V_{in}$ $V_{SW}=V_{Din}=(G-1)V_{in}$ $V_{SWo}=V_D=GV_{in}$	$\frac{(1+D(1+n))}{D(1-D)(1+n)}I_{in}$	$I_m=\frac{(2+n)}{(1-D)}I_{in}$
SSCL-qSBN	+ simple and small magnetic element ($n<1$) + very low total capacitance value + very low shoot-through current + quasi-continuous input current − need for one active switch − lack of a common ground	$\frac{Gn-(2+n)}{2(1+n)G}$	$V_{D1,2}=\frac{(G+1)(2G-1)}{G(2+\mathrm{n})}V_{in}$ $V_{SWo/SW}=V_{Din}=V_D=GV_{in}$	$\frac{(1+D(1+n))}{D(2+n)}I_{in}$	$I_m=(1+n)I_{in}$
TSCL-SBN	+ simple and small magnetic element ($n<1$) + low total capacitance value + low shoot-through current + input and output common grounded − discontinuous input current − need for one active switch	$\frac{G(1-n)-1}{(2G-1)}$	$V_{D1}=\frac{(1+n^2)G-1}{(1+n)}V_{in}$ $V_{SW}=V_{Din}=(G-1)V_{in}$ $V_{SWo}=V_D=GV_{in}$	$\frac{(n+D)}{D(1-D)}I_{in}$	$I_m=\frac{(1+n)}{(1-D)}I_{in}$
TSCL-qSBN	+ simple and small magnetic element ($n<1$) + very low total capacitance value + very low shoot-through current + quasi-continuous input current − need for one active switch − lack of a common ground	$\frac{G(1-n)-(1+n)}{2G}$	$V_{D1}=\frac{(1+n^2)G-(1-n^2)}{(1+n)}V_{in}$ $V_{SWo/SW}=V_{Din}=V_D=GV_{in}$	$\frac{(n+D)}{D(1+n)}I_{in}$	$I_m=I_{in}$
SCL-qZSN [24]	+ continuous input current + input and output common grounded − massive coupled-inductors, even with $n=1$ − high total capacitance value − high shoot-through current	$\frac{G-(2+n)}{(3+n)G}$	$V_{D1,2}=\frac{(1+n)G}{(2+n)}V_{in}$ $V_{SWo}=V_{Din}=GV_{in}$	$\frac{(1+n)+(3+n)D}{(2+\mathrm{n})D}I_{in}$	$I_m=I_{in}$
ASC/SL-qZSN [19]	+ quasi-continuous input current + very low shoot-through current − very low gain − very high total inductance value − lack of a common ground	$\frac{G-1}{3G+1}$	$V_{D3}=\frac{(1-D)}{D}V_{D1,2}=(1+G)V_{in}$ $V_{S7/SWo}=V_{Db}=V_{Di}=GV_{in}$	$\frac{2}{(1+D)}I_{in}$	NA*
DC-DC Converter in [25]	+ quasi-continuous input current + very low switch current stress + soft-switching (ZVS) capability − very high turn ratios requirement − high total inductance requirement	$\frac{G-1}{G+n}$	$V_{S1,2}=\frac{(n+G)}{n+1}V_{in}$ $V_{Do}=(n+G)V_{in}$	I_{in}	I_{in}

* NA- NOT APPLICABLE
** IS ALSO SWITCH CURRENT STRESS

impedance network is then normalized based on C_B of (21). The comparative results are shown in Fig. 5(b). According to this analysis, the total capacitance demand of all proposed impedance networks is significantly lower than the SCL-qZSN. However, the proposed impedance networks require more total capacitance than the ASC/SL-qZSN.

3) Shoot-Through Current: One of the most restricting parameters of the ZSCs is the current that flows through the output switches, which is referred to as the ST current. The high ST current often makes the semiconductor selection very critical. In order to validate the low ST current operation of the proposed impedance networks, Fig. 5(c) is plotted with the I_{sh} equations given in Table II. The normalized ST currents of the proposed impedance networks, the SCL-qZSN and the ASC/SL-qZSN as a function of voltage gain, are plotted in this figure. As a common feature among all proposed and SCL-qZSN impedance networks, the ST current highly increases at low voltage gains that define a practical lower limit for the voltage gain. On the other hand, the proposed qSBN-based topologies produce twice less ST currents than the SCL-qZSN with $n=3$ at the same voltage gain. Besides, the current stress is fairly comparable among the proposed SBN-based topologies, the SCL-qZSN, and the ASC/SL-qZSN. Finally, the ASC/SL-qZSN offers the minimum ST current requirement among all competitors. Meanwhile, all proposed impedance networks can offer much higher voltage gains compared to the ASC/SL-qZSN. In addition to the ST state currents (I_{sh}), the switches and diodes blocking voltages (V_B), the duty cycles (D), and the magnetizing currents (I_m) of all proposed impedance networks, the SCL-qZSN, the ASC/SL-qZSN, and the dc–dc converter of [25] with pros and cons are given and compared in Table II. The switch SW_o is considered as the dc-link switch of the SCL-qZSN and the ASC/SL-qZSN in this table.

4) Voltage Stress: The total blocking voltage of all switching devices of the proposed impedance networks is calculated from the voltage equations given in Table II and the results are

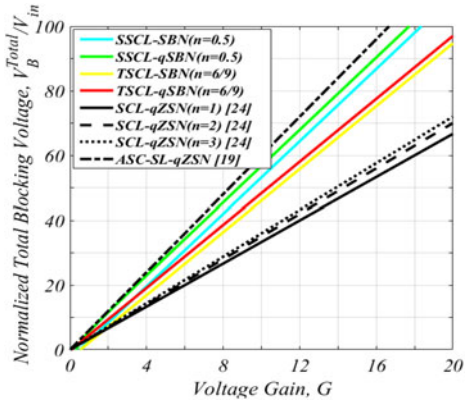

Fig. 6. Normalized total blocking voltage versus voltage gain.

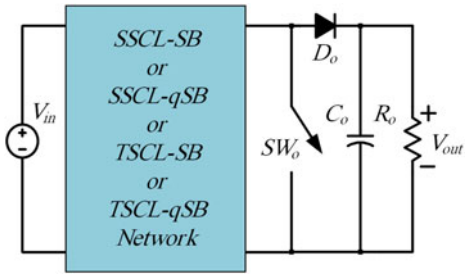

Fig. 7. Implementation of the proposed impedance networks within a dc–dc converter.

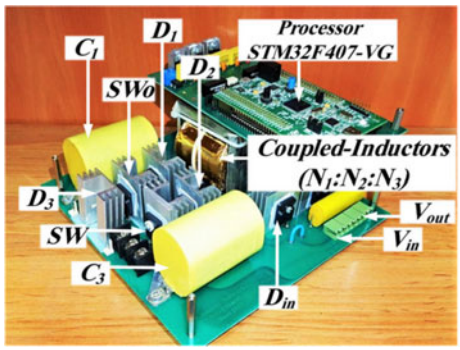

Fig. 8. Prototype picture.

compared with other competitors. The normalized total blocking voltages versus the voltage gain (G) are plotted in Fig. 6. As seen in this figure, the normalized total blocking voltages of the proposed impedance networks are lower than those of the ASC/SL-qZSN and higher than compared to the SCL-qZSN. According to Table II, it is worth mentioning that the SCL-qZSN has the minimum number and the ASC/SL-qZSN has the maximum number of active components among all topologies under study.

IV. Experimental Results

For the sake of simplicity, a dc–dc converter, shown in Fig. 7, is considered as the test bench of the proposed impedance networks. The picture of laboratory test rig is shown in Fig. 8. The parameters of the experimental system are summarized in Table III. The gate signals are generated by an ARM microcontroller, STM32F407VG from STMicroelectronics. As shown in Fig. 9, a simple pulse width modulation (PWM) signal is generated for both SW and SW_o by comparing the duty cycle signal with a triangular carrier waveform. The magnetic elements of the proposed Z-source cells are wound on the center leg of an EE ferrite core with trifilar copper foils to reduce the leakage inductances. The core material is equivalent to R from Magnetics®. It is important to note that the input voltage for the SBN-based topologies is set to 55 V_{dc} and for the qSBN-based ones to 30.5 V_{dc}. In addition, the duty cycle (D) was assumed constant and the same for all proposed topologies, as given in Table III. This ensures the output voltage gain of $G = 5$ and 9 for the SBN and the qSBN-based topologies, respectively. With the voltage equations already derived in Section II and the parameters of Table III, one can calculate $V_{out} = V_{C1} = 275\,V_{dc}$ for all topologies and $V_{C3} = 183.3\,V_{dc}$ and $203.6\,V_{dc}$ for the SBN-based and the qSBN-based topologies, respectively. Besides, the measured and calculated average values of the output

TABLE III
Experimental Parameters

Description	Values
Rated power	220 W
Input voltage	30.5 V_{dc} , 55 V_{dc}
Output voltage	275 V_{dc}
Frequency, f_{sw} & duty cycle, D	10 kHz, 0.075
Capacitors: C_1, C_3 and C_o	28 µF, 68 µF and 20 µF
Magnetic core	EE70/33/32 Ferrite
Magnetizing inductances (L_m):	
SSCL-cell (N_1:N_2:N_3→n)	230 µH (12:12:6→n=0.5)
TSCL-cell (N_1:N_3→n)	500 µH (18:12→n=6/9)
IGBT switches, SW and SW_o	FGH60N60SFD
Diodes, D_1-D_3, D_{in} and D_o	VS-60EPU04

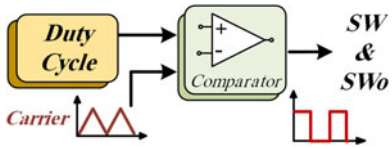

Fig. 9. PWM generation of gating signals.

TABLE IV
Measured and Calculated Parameters Values

Parameter		SSCL-SBN	SSCL-qSBN	TSCL-SBN	TSCL-qSBN
V_{out}	*Meas.*	266 V	265 V	262 V	263 V
	Calc.	275 V	275 V	275 V	275 V
	Err.%	3.27%	3.63%	4.72%	4.36%
V_{C3}	*Meas.*	168 V	187 V	160 V	180 V
	Calc.	183.3 V	203.6 V	183.3 V	203.6 V
	Err.%	8.36%	8.18%	12.7%	11.6%
I_{in}	*Meas.*	4.46 A	8.12 A	4.6 A	8.22 A
	Calc.	4 A	7.21 A	4 A	7.21 A
	Err.%	11.5%	12.6%	15%	14%
I_m	*Meas.*	12.3 A	12.2 A	8.25 A	8.1 A
	Calc.	10.8 A	10.8 A	7.2 A	7.21 A
	Err.%	13.8%	12.9%	14.5%	12.3%
$\frac{I_m}{I_{in}}$	*Meas.*	2.75	1.5024	1.79	0.985
	Calc.	2.7	1.5	1.8	1
	Err.%	1.85%	0.1%	0.5%	1.46%

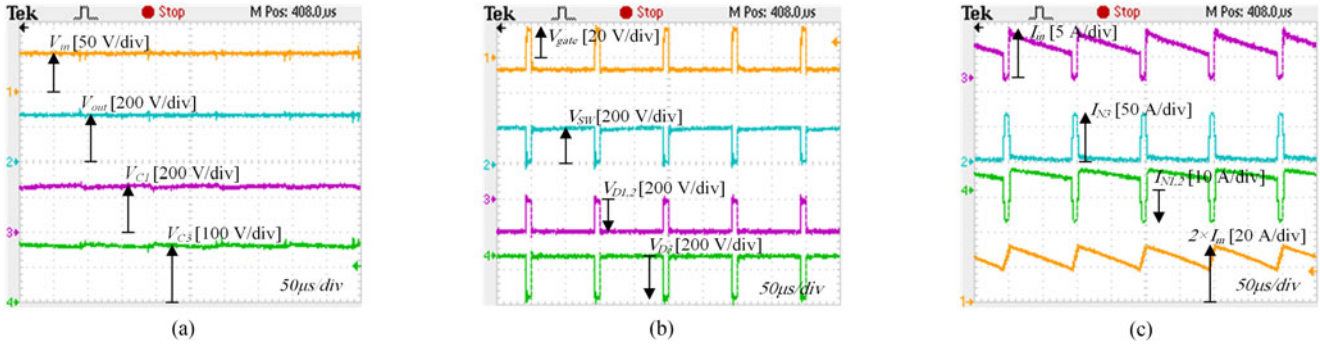

Fig. 10. SSCL-SBN experimental waveforms. (a) Input voltage, output voltage, C_1 voltage, and C_3 voltage. (b) Gate pulse of switches *SW* and *SW*$_o$, voltage across switch *SW*, diodes $D_{1,2}$ and D_3. (c) Input current, winding N_3, winding $N_{1,2}$, and magnetizing currents from top to bottom.

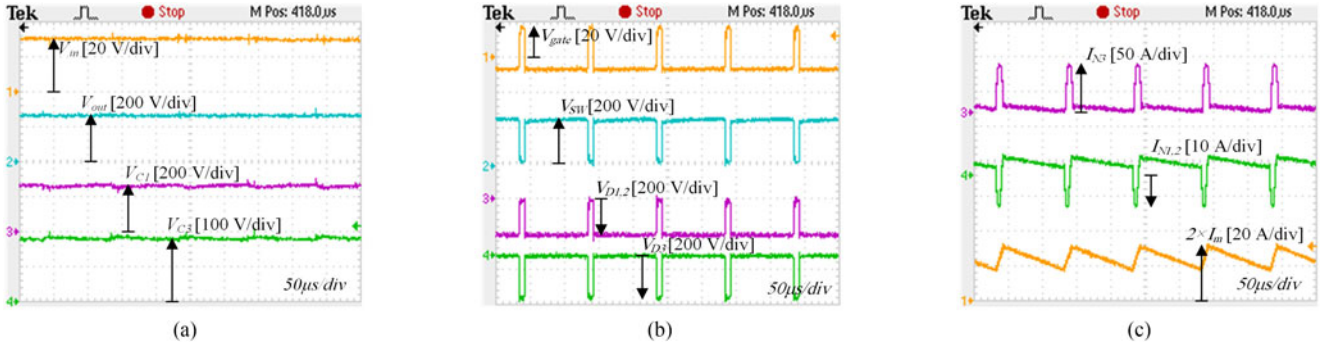

Fig. 11. SSCL-qSBN experimental waveforms. (a) Input voltage, output voltage, C_1 voltage, and C_3 voltage. (b) Gate pulse of switches *SW* and *SW*$_o$, voltage across switch *SW*, diodes $D_{1,2}$ and D_3. (c) Winding N_3, winding $N_{1,2}$, and magnetizing currents from top to bottom.

and the cell capacitor voltages and the input and the magnetizing currents are summarized in Table IV. Evidently, the measured currents are slightly higher than the calculated ones, since the efficiency of the converter in the calculations is assumed to be unity.

Figures 10 and 11 show the waveforms of the SSCL-based converters. The input and output voltages V_{C1} and V_{C3} for the SSCL-SBN and for the SSCL-qSBN are shown in Figs. 10 and 11(a), respectively. As can be seen from Fig. 10(a), the ripple of the output voltage is much lower than the voltage ripple across C_1. This is due to the increase of the output capacitance during the non-ST state and at the same time the very short ST duration. The voltages across the active switch *SW* and the diodes $D_{1,2}$ and D_3 are shown in Fig. 10(b) for the SSCL-SBN and Fig. 11(b) for the SSCL-qSBN, where channel 1 is the gating signal of *SW* and *SW*$_o$ that is active during the ST state. As already expected, *SW* and $D_{1,2}$ conduct during the ST state, while diode D_3 blocks the voltage of C_1. The very short period of conduction (<10 μs) results in much lower ST current stresses, and at the same time, allowing to derate the switches to a lower rated current. Figs. 10 and 11(c) represent the waveforms of the input, the windings, and the magnetizing currents. As observed from these two figures, input current of the SSCL-SBN is discontinuous, while it is quasi-continuous for the SSCL-qSBN. It should be noted that the currents of the diode D_{in} and the input current of the SSCL-SBN, and the winding N_3 and the input current of the SSCL-qSBN are the same, respectively [see Fig. 3(a)–(d)]. Also, the windings N_1 and N_2 currents of the SSCL cell are the same, as depicted in Figs. 10 and 11(c). The winding N_3 currents are also shown in these figures, which have always positive values unlike the windings N_1 and N_2 currents. It is worth mentioning that an *LC* circuit constituting leakage inductances of the SSCL or the TSCL cells and the capacitors C_1 and C_3 causes a sinusoidal positive half-cycle resonance appear in the cell windings and capacitors currents during the ST state. With the proper selection of the capacitances C_1 and C_3 such that this sinusoidal positive half-cycle completes before the end of the ST state, a significant reduction in voltage spikes across the switching semiconductors is achieved. The same tests procedure has been considered for the TSCL-based proposed converters, as observed from Figs. 12 and 13, where Fig. 12 shows the TSCL-SBN and Fig. 13 shows the TSCL-qSBN experimental results. Also, the obtained parameter values from the TSCL-based converter operation are all given in Table IV. A close agreement between the measured and calculated values is clear that support the analytical achievements. As obviously can be seen from Figs. 12 and 13, the same principles of operations are held for the TSCL-based proposed converters as those for their SSCL-based counterparts. Although, unlike the SSCL cell, the winding N_1 in the TSCL cell has always positive values in its current during a switching cycle [see Fig. 3(e)–(h)].

As can be concluded from Table III and the experimental waveforms, the ST duration of 7.5 μs is enough to ensure that the ST current can reach zero before the end of the ST state; there-

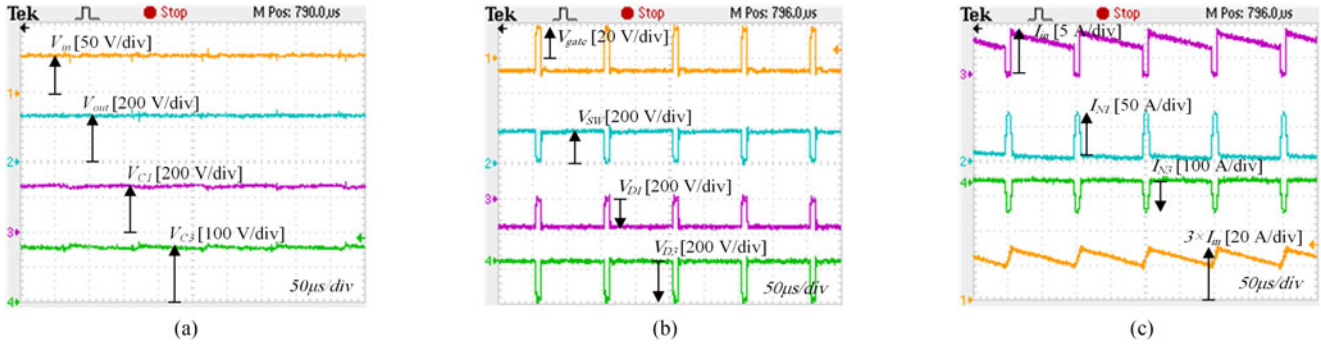

Fig. 12. TSCL-SBN experimental waveforms. (a) Input voltage, output voltage, C_1 voltage, and C_3 voltage. (b) Gate pulse of switches *SW* and *SW*$_o$, voltage across switch *SW*, diodes D_1 and D_3. (c) Input current, winding N_1, winding N_3, and magnetizing currents from top to bottom.

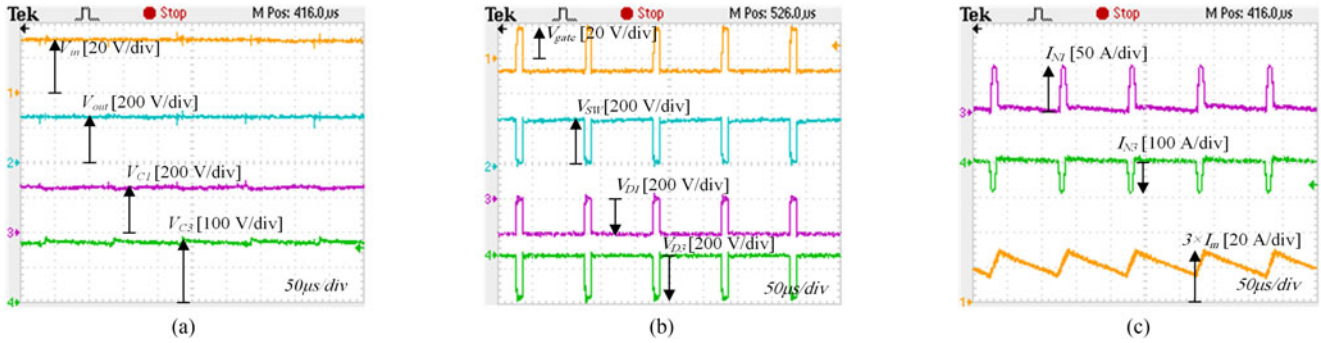

Fig. 13. TSCL-qSBN experimental waveforms. (a) Input voltage, output voltage, C_1 voltage, and C_3 voltage. (b) Gate pulse of switches *SW* and *SW*$_o$, voltage across switch *SW*, diodes D_1 and D_3. (c) Winding N_1, winding N_3, and magnetizing currents from top to bottom.

fore, a zero current turn-OFF of semiconductor devices is possible, resulting in reduced switching losses and smooth switching transients. However, lower duty cycles than $D = 0.075$ are also possible with the risk of interrupting a high ST current for this paper's converters design.

In order to verify magnetizing current equations of the SSCL and the TSCL cells given in Table II, these waveforms are also reported in Figs. 10–12 and 13(c).

It must be clarified that the magnetizing current is measured from the winding currents multiplied by the turn numbers, i.e., $N_1 I_m = N_1 I_{N1} + N_2 I_{N2} + N_3 I_{N3}$. According to the turn numbers, it is more convenient to calculate $2I_m = 2I_{N1} + 2I_{N2} + I_{N3}$ for the SSCL cell and $3I_m = 3I_{N1} + 3I_{N2} + 2I_{N3}$ for the TSCL cell.

According to Table II, the ratio of magnetizing current to the input current (I_m/I_{in}) is 2.7, 1.5, 1.8, and 1, for the SSCL-SBN, SSCL-qSBN, TSCL-SBN, and TSCL-qSBN, respectively. Again, the measured average values of I_m and I_m/I_{in} ratios, concluded from Table IV, are in a good agreement with their theoretically calculated values. As a comparative analysis of performance differences among the proposed topologies, the ripples of the voltage across the capacitors and the magnetizing currents are obtained from Figs. 10 to 13. The ripple of I_m is 55.2%, 61.4%, 48.4%, and 65.8% for the SSCL-SBN, SSCL-qSBN, TSCL-SBN, and TSCL-qSBN, respectively. According to these results, the qSBN-based topologies produce higher current ripples than the SBN-based ones, which can be contributed to the higher voltage across the winding N_1 of the SSCL and TSCL cells during the ST state. In addition, the voltage ripple is 5.4% for C_1 and 4.3% for C_3 for all topologies. These results show that the voltage ripple of the capacitor C_3 is slightly lower than that of C_1, because of its lower voltage level and about 2.5-times higher capacitance. Finally, the efficiency is compared based on the experimental results obtained for the proposed topologies and the competitors in the same dc–dc circuit. The results for four different voltage gains of 4, 5, 7, and 9 are plotted in Fig. 14(a)–(d), respectively. The output voltage is fixed to 275 V_{dc} by manually adjusting the duty cycle in all tests. Fig. 14 depicts that all proposed impedance converters offer a higher efficiency than the ASC/SL-qZSN at different gains and powers. On the other hand, the efficiency of the proposed SBN-based topologies is lower than that of the SCL-qZSN ($n = 1$), as shown in Fig. 14(a) and (b). According to Fig. 14(c) and (d), the proposed SSCL-qSBN offers a higher efficiency than the proposed TSCL-qSBN, the SCL-qZSN ($n = 1$), and the ASC/SL-qZSN. Also, the efficiency of the proposed TSCL-qSBN is lower than the SCL-qZSN ($n = 1$) for $G = 7$ and higher than that for $G = 9$. Obviously, the SCL-qZSN ($n = 1$) efficiency at high voltage gains decreases, while with the proposed qSBN-based topologies, the efficiency is even slightly increased. Certainly, a more optimized design and components selection improve the efficiency of the proposed impedance converters. It should be noted that the ASC/SL-qZSN cannot achieve $G = 9$ in experimental tests due to very high losses. As shown in Fig. 14, the efficiency

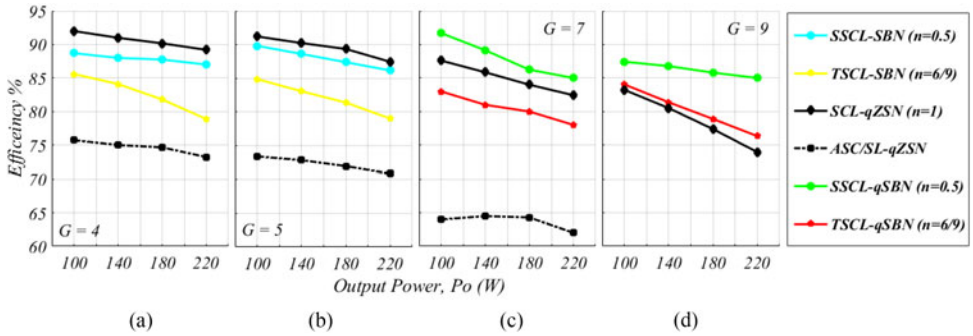

Fig. 14. Efficiency comparison among the proposed SBN-based topologies for (a) $G = 4$ and (b) $G = 5$, and qSBN-based topologies for (c) $G = 7$ and (d) $G = 9$ with the SCL-qZSN and the ASC/SL-qZSN.

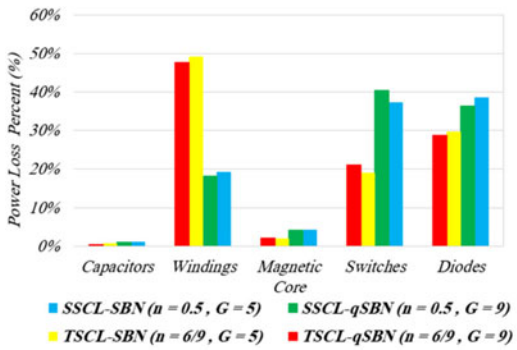

Fig. 15. Power loss distribution in percent.

of the ASC/SL-qZSN is drastically lower than the SCL-qZSN ($n = 1$) and the proposed impedance converters. Therefore, it can be readily concluded that the ASC/SL-qZSN is not a proper solution for high-gain and low-power applications.

The loss distribution among the components of the proposed impedance converters is obtained using the analytical method in [22], shown in Fig. 15. For the test conditions presented in Table III, the results are obtained and summarized in Fig. 15, which shows the percentage of each component loss share for the proposed impedance converters. Evidently, the winding losses are dominant for the TSCL-based topologies, while the switching losses have the main share for the SSCL-based ones. The capacitor loss is negligible, because low equivalent series resistance (ESR) plastic-film capacitors are utilized. Also, the core loss is very low, which can be attributed to the almost low switching frequency, the low loss ferrite material, and the small variations of the magnetizing current and consequently the magnetic flux in the core.

V. Conclusion

This paper introduced a new class of coupled-inductors-based impedance networks in the dc–dc application. The main advantages can be summarized as a very high voltage gain ability with less-than-unity ($n < 1$) turn ratio, lower inductance and capacitance requirement, and reduced ST state duration and stresses. The improvements were achieved at the price of need for one active switch in all proposed impedance networks and lack of a common ground between the input and the output in the qSBN-based ones. The theoretical steady-state operation analysis was presented and successfully confirmed with experimental tests.

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