Energy-Efficient Wide-Range Voltage Level Shifters Reaching 4.2 fJ/Transition

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***Abstract*— This letter proposes a new level-shifting structure that can convert extremely low levels of input voltages to high output voltages while maintaining excellent delay and power dissipation. In order to reduce contention and voltage swing in the internal nodes, the proposed circuit uses a diode-connected level shifter between gate terminals of the output inverter. Using a control circuit, only during the high-to-low transitions of the output, a current is forced into the diode-connected device. Measurement results demonstrate that the proposed circuit can consume as small energy as 4.2 fJ/transition with V_{DDL} and V_{DDH} of 0.35 V and 1.1 V, respectively when implemented in a 40-nm CMOS technology. Furthermore, when fabricated in a 180-nm technology, the level-shifting circuit can convert V_{DDL} s as small as 80 mV to 1.8 V without using low-threshold devices.**

***Index Terms*—Level converter, level shifter, low power, nanometer-scale CMOS, wide range, sub-threshold.**

I. Introduction

In the relentless push towards an ultra-low-power circuit design of digital [1] and mixed-signal [2] system-on-chip (SoC), the most proven way is to reduce the supply voltage. This method is especially effective if the value of the supply voltage is chosen below the threshold level of CMOS devices (so-called sub-threshold design) [3], [4]. This technique results in dual- or multi-supply systems whereby time-critical parts are powered at a higher supply voltage (i.e., V_{DDH}) whereas other noncritical parts operate at a lower supply voltage (i.e., V_{DDL}). This allows to conveniently trade off performance versus power consumption of low and high supply voltages. Furthermore, even if the whole core of a chip could work in the sub-threshold domain, an above-threshold supply voltage would still be needed for the digital input/output (I/O) pad cells. Hence, level-shifting or level-converting circuits with short delay and low power dissipation are needed to interface the sub-threshold circuit parts with the above-threshold modules. In other words, the required level shifters must convert the low logic levels of (0, V_{DDL}) to the high logic levels of (0, V_{DDH}). One of the most common implementations of a voltage level-shifting circuit is shown in Fig. 1.

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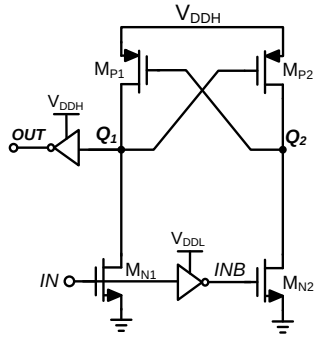

Fig. 1. Schematic of the conventional voltage level shifter.

Its operation is as follows. When the input signal (i.e., *IN*) goes from "V_{SS}" (i.e., ground) to "V_{DDL}" (L→H transition), the input transistors M_{N1} and M_{N2} are turned on and off, respectively. As M_{N1} is trying to pull node Q_1 down to V_{SS}, M_{P2} is gradually turned on to pull node Q_2 up to V_{DDH} and to turn M_{P1} off. It can be observed that there is a contention between the pull-up transistor (i.e., M_{P1}) driven to V_{DDH} and the pull-down transistor (i.e., M_{N1}) driven by V_{DDL} during the transition times in which the output is not yet corresponding to the logic level of the input. This leads to an increase of the propagation delay and, therefore, power dissipation. It also increases the minimum acceptable value of V_{DDL} (i.e. $V_{DDL,min}$) for a given value of V_{DDH}. In [5]-[20], several efforts have been reported to improve the performance of level shifters; specifically to reduce the power consumption (or energy-per-transition), to increase the speed, and to reduce the value of $V_{DDL,min}$. In this letter, a high-performance voltage level shifter using a diode-connected transistor with dynamic current switching [21] is proposed. Not only this makes a considerable reduction in the delay and the power consumption, but also enables the circuit to operate correctly for a wide range of V_{DDL} values.

II. Proposed Voltage Level Shifter

The schematic of the proposed voltage level shifter is shown in Fig. 2. It consists of an input and an output branch. The input branch comprises a controllable current source, a diode-connected transistor, M_{P3}, serving as an internal level shifter (ILS), and an nMOS switch transistor, M_{N3}. The output branch is a CMOS inverter consisting of M_{N4}/M_{P4}. Fig. 2(a) shows the conceptual schematics of the basic structure of the proposed level shifter where the gate terminals of the output stage (i.e., $V_{G,N}$ and $V_{G,P}$ where $V_{G,P}=V_{G,N}+|V_{GS,P3}|$) are separated by the ILS (i.e., M_{P3}). Fig. 2(b) shows the detailed circuit where the switched current source is implemented using M_{N1}, M_{N2}, M_{P1} and M_{P2}. The operation of the circuit in both H→L and L→H transitions of the input signal will be explained here.

A. High-to-Low Transition

During pull down (i.e. at the H→L transition of the input), M_{N3} is

turned off while a current is injected into M_{P3} (only during the transition). Therefore, the voltages of both G_P and G_N nodes rise and the pull-up pMOS device is weakened. Therefore, the existing contention between the pull-up and pull-down devices will be reduced leading to decrease the propagation delay and the power consumption of the circuit. The current I_2 is injected during the H→L transition since INB has become "H" and OUT is still "H" and thus the current in M_{N1} and M_{N2} is mirrored through M_{P1} and M_{P2}. As soon as the output node falls below $V_{th,N2}$, where $V_{th,N2}$ is the threshold voltage of M_{N2}, the current spike flowing through M_{N2}, M_{N1} and M_{P1} drops to zero. It should be noted that the current-mirror ratio, i.e., $(W/L)_{MP1}/(W/L)_{MP2}$ directly affects the circuit delay (i.e., $t_{p,H\to L}$) as will be discussed in Section III.

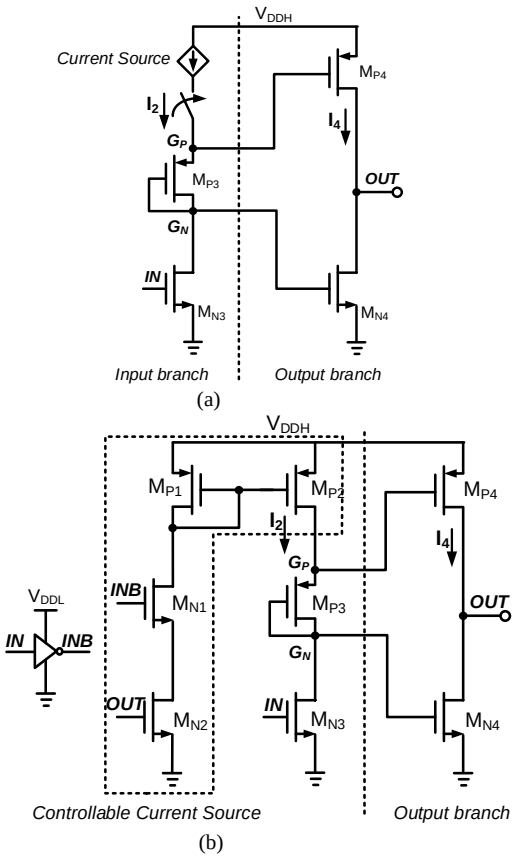

Fig. 2. Schematic of the basic structure of the proposed level shifter: (a) conceptual schematics (b) detailed circuit.

B. Low-to-High Transition

During pull up, since M_{N3} is on and since no current is injected into M_{P3}, the drain terminal of M_{N3} (i.e., the gate terminal of M_{N4}) is pulled down to ground; thus turning M_{N4} off. The voltage of node GP, in this case, becomes low enough to turn M_{P4} on.

It should be emphasized that there is no static power consumption in the circuit since the current source is only on during the H→L transitions of the signal.

III. Design Considerations

In this section, the impact of sizing for different devices on important merits of the circuit will be studied. Furthermore, for special requirements for the circuit, i.e. larger V_{DDL} range (smaller $V_{DDL,min}$) at the output, a modified structure will be proposed.

A. Circuit Speed

Considering the H→L transition, the propagation delay, i.e. $t_{pH\to L}$ is strongly affected by the strength of the pull-down network and the contention at the output node. As explained in Section II, during the H→L transition, there is a contention between the pull-down M_{N4} gradually turning on and the pull-up M_{P4} gradually turning off. In order to reduce the delay time, both the gate terminals of M_{N4} and M_{P4} must be raised quicker. Therefore, a larger current being injected to M_{P2}, increases the speed with which the voltages of the gate terminals rise. Furthermore, the smaller the parasitic capacitance at G_N node, the higher the rising speed of the node becomes. Besides, the larger the voltage drop across M_{P3}, the higher the G_P node voltage and thus the weaker the pull-up strength. By increasing the mirroring ratio, the current injected to M_{P3} is increased and thus the delay is decreased. In order to reduce the power consumed in the current mirror, and to have a suitable mirroring ratio of M_{P1} and M_{P2}, M_{P1} was made much longer than the minimum gate length of the other transistors. Furthermore, by increasing the size of M_{P3}, since the voltage drop across it is decreased and since the parasitic capacitances are also larger, the H→L propagation delay also increases.

Similarly, the L→H transition delay mainly depends on the strength of the pull-up network, i.e. M_{P4} and the contention at the output. It can be observed that by increasing the mirroring ratio, the delay becomes worsened due to the fact that the parasitic capacitances are larger. Also, the larger the size of M_{P3}, the smaller the voltage drop and the larger the parasitic capacitance; increasing the delay. Based on the above, the designer can decide about the sizing of the devices. For minimum propagation delay that includes both the H→L and L→H delays, the designer can decide about the optimum value of the sizes.

B. Power Consumption

In order to reduce the power consumption, not only the contention at the output node in both H→L and L→H transitions but also the parasitic capacitances, including those associated with the internal nodes, must be minimized. Therefore, increasing the mirroring ratio, slightly increases the power consumption; however, by increasing the size of M_{P3}, the power is reduced. In this work, the size of all nMOS devices are chosen as minimum and the corresponding pMOS devices are sized proportionally (to have equal pull-up and pull-down strengths). Just the length (i.e., L) of M_{P1} is chosen much larger than that of M_{P2} to have a suitable mirroring ratio between M_{P1} and M_{P2}.

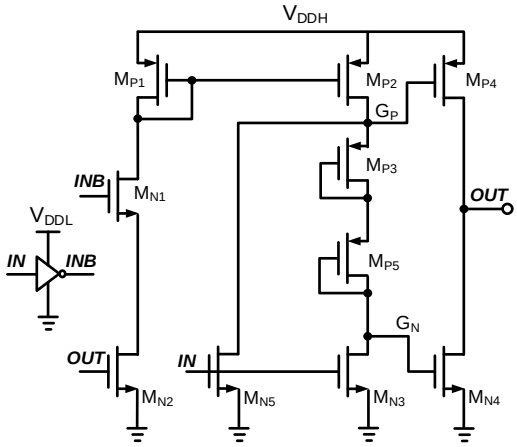

Fig. 3. Schematic of the wide-voltage range level shifter

C. V_{DDL} Range

Another important parameter of level shifters is the value of $V_{DDL,min}$ (for a given value of V_{DDH}). In order to increase the convertible V_{DDL}

range, i.e., reducing the value of $V_{DDL,min}$, the structure depicted in Fig. 3 with two modifications compared to Fig. 2 is proposed. First, another level-shifting diode-connected device, i.e., M_{P5}, is put in series with MP3. Second, in order to increase the pull-up strength at the L→H transition, the gate terminal of M_{P4} has to be pulled hard to V_{SS}, thus motivating the addition of M_{N5}. By increasing the number of internal diode-connected devices, the voltage drop between $V_{G,P}$ and $V_{G,N}$ increases; further reducing the voltage swing of $V_{G,N}$. Therefore during the L→H transition of the sub-threshold input signal, $V_{G,N}$ is pulled down faster by M_{N3} thus lowering both the $t_{pL\rightarrow H}$ and the power consumption.

IV. Measurement Results

In order to study the effect of the technology, the proposed circuit has been fabricated in both 40-nm and 180-nm standard CMOS technologies. Fig. 4 shows the chip micrograph of the one fabricated in 40-nm CMOS. The area of the circuit is 8 μm^2 and 135 μm^2 in the 40-nm and 180-nm technologies, respectively. In the fabricated circuits in 40-nm CMOS, the W/L size of almost all devices is set to 120nm/40nm (i.e., the minimum allowed) to reduce the parasitic capacitances. Furthermore, all devices, except for M_{P3} (which is a nominal-V_T device with a $|V_{T0}|$ of 416mV) are low-V_T devices with threshold voltages of 311mV and -337mV for nMOS and pMOS, respectively. Note that in order to reduce the size and, therefore, the parasitic capacitance of M_{P3}, it has not been put in a separate n-well and the body terminals of M_{P1}-M_{P4} are all tied to V_{DDH}. . In order to measure the delay of the circuit, both input and output buffers are replicated in another "test" path, as shown in Fig. 5. Therefore, the delay between the "OUT_SIG" and "OUT_TEST" is an estimation of the delay between "IN" and "OUT" nodes. Of course, it is a pessimistic estimation of the delay since V_{DDL} is always smaller than the supply voltage of the buffers, i.e., V_{DD_BUFF} and thus the corresponding inverter is slower in the main path compared to the "test" path. Furthermore, the input signal, *IN*, experiences the skewness practically happening for such a "low-swing" signal.

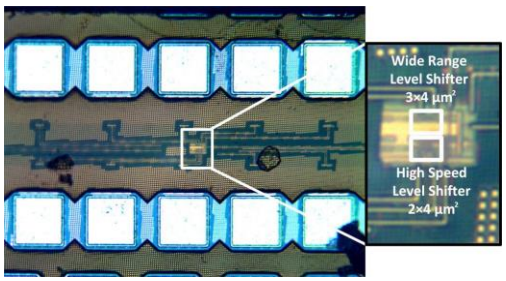

Fig. 4. Microphotographs of the chips fabricated in 40-nm CMOS.

A. 40-nm Implementation Results

Fig. 6 shows the measured waveforms of both OUT_SIG and OUT_TEST at the input pulse frequency of 1MHz. The value of $V_{DDL,\ min}$ is 120mV (that can be shifted to 1.1 V for a maximum operating frequency, f_{max}, of 140 kHz). For the circuit shown in Fig. 3, the value of $V_{DDL,min}$ is reduced down to 50 mV for f_{max}= 10 kHz. The level shifter consumes only 4.2 fJ/Transition for a 0.35-V → 1.1-V conversion. As for the value of the delay, to exclude the effect of the technology, it should be expressed as a function of fanout-4 (FO4). For a 0.4-V→0.9-V conversion, the value of delay is 1.17 FO4 (using a simulated value for FO4). Furthermore, it should be mentioned that for smaller values of V_{DDH}, the power consumption and thus the energy-per-transition are reduced. At a frequency of 100 kHz, the energy-per-transition of the circuit is only 1.8 fJ for a 0.25-V→ 0.6-V conversion.

B. 0.18-μm Implementation Results

In order to demonstrate the effect of the technology on the performance of the level shifter and the effectiveness of the proposed structure in older CMOS processes, both the circuit of Fig. 2-b and the one depicted in Fig. 3 have been fabricated in a standard 0.18-μm CMOS technology. In this section, the value of V_{DDH} is assumed to be 1.8 V unless explicitly stated otherwise. Measurements confirm that the circuit can convert V_{DDL} levels of 180mV and 400mV for operating frequencies of 10 kHz and 5 MHz, respectively. The energy-per-transition of the level converter for the 0.4 V→1.8 V conversion at a frequency of 5 MHz is 46 fJ/transition. The measured value of $V_{DDL,min}$ for the circuit shown in Fig. 3 capable to be converted to V_{DDH} of 1.8V is 80 mV at the frequency of 10 kHz. Finally, the performance of the circuits are compared to the state-of-the-art reports in Table I. It can be observed that not only the minimum convertible value of V_{DDL} but also the energy-per-transition have considerably been improved in the proposed circuits.

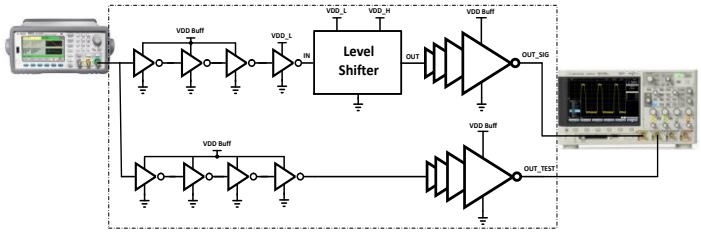

Fig. 5. Test setup for the delay measurement.

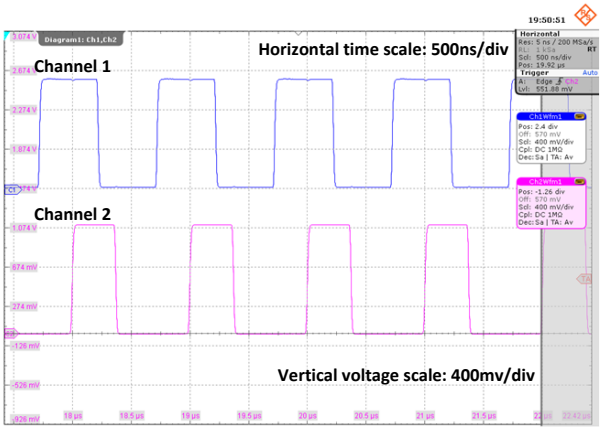

Fig. 6. Oscilloscope screenshot of OUT_TEST (Ch.1) and OUT_SIG (Ch.2) for a 1-MHz signal.

V. Conclusion

We have proposed a highly power-efficient level shifter covering a wide range of frequencies and voltages, which is capable of converting extremely low input voltages. The key enabling idea is to reduce contention between the output devices through a dynamically engaged diode-connected internal level-shifting transistor inserted between their gate terminals. Measurement results in both 40-nm and 180-nm CMOS technologies confirm the power efficiency of the proposed level shifter. Compared to the state-of-the art, the proposed circuits exhibit superior performance, especially from the power consumption viewpoint. For the case where a wider range for V_{DDL} is required, i.e. if a smaller $V_{DDL,min}$ is desired, an additional internal level shifter has been inserted. The designer can therefore decide

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

	Technology	V_{DDH}	$V_{DDL,min}$	Delay (ns) (V_{DDL}→ V_{DDH})	Static Power (nW) @ V_{DDL}	Energy per Transition (fJ)@ V_{DDL}	Area (μm^2)
Y. Osaki, JSSC '12 [9]	0.35 µm	3 V	230 mV	10000 ns (0.4V→3V)	0.23@ 0.4V	5800 @0.4V	1880
S.-C. Luo, TCAS-I'14 [13]	65 nm	1.2 V	100 mV	N.A.	4.05@0.2V	667 @0.2V	16
J. Zhou, TCAS-I'15 [15]	180 nm	3.3 V 1.8 V	210 mV	243 ns (0.3→3.3) 167 ns (0.3→1.8)	0.97@0.3V 0.16@0.3V	954 (0.3V → 3.3V) 39 (0.3V →1.8V)	153
Y. Kim, VLSIC'11 [16]	130 nm	2.5 V	300 mV	41.5 ns (0.3V→2.5V)	0.475@0.3V	229 @0.3V	102
W. Zhao, TCAS-II,'15 [17]	65nm	1.2 V	140 mV	25 ns (0.3V→1.2V)	2.5	30.7 (0.3V→1.2V)	17.6
Y. Ho, TCAS-II'16 [18]	65 nm	1 V	200 mV	12.9 ns (0.2V→1V)	N.A.	204(0.2V → 1V)	1931
L. Wen, TCAS-II '16 [19]	65 nm	1.2 V	100 mV	13.7 ns (0.2V→1.2V)	1.24@0.2V	90.9 (0.2V → 1.2V)	31.3
M. Lanuzza, TCAS-II '17 [20]	180 nm	1.8 V	100 mV	31.7 ns (0.4V→1.8V)	0.055@0.4V	173 (0.4V →1.8V)	108.8
This work	180 nm (Fig. 2)	1.8 V	180 mV	180 ns (0.4V→1.8V)	1.5@0.1V	46 (0.4V →1.8V)	135
	180 nm (Fig. 3)	1.8 V	80 mV	95 ns (0.4V→1.8V)	1.8@0.1V	118 (0.4V →1.8V)	160
	40 nm (Fig.2)	1.1 V	120 mV	15.5 ns (0.4V→1.1V)	0.55@0.2V	4.2 (0.35V → 1.1V)	8
	40 nm (Fig.3)	1.1 V	50 mV	80 ns (0.3V→1.1V)	0.6@0.2V	18 (0.35V → 1.1V)	12

between the circuit configurations based on the application whether a higher speed or a larger V_{DDL} range is required.

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