An Integrated Interleaved Dual-Mode Time-Sharing Inverter for Single Phase Grid Tied Applications

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***Abstract*—A novel integrated interleaved dual-mode time-sharing inverter (IIDMI) is proposed for the grid-tied transformer-less photovoltaic (PV) applications. While, the dual-mode time-sharing conversion technique ensures minimum losses, the IIDMI also retains the advantages of interleaved topologies, such as low total harmonic distortion of the AC current with reduced filtering requirements, increased power density and reduced current and thermal stresses of power devices. Besides, the leakage current problem, which is a main concern with the transformer-less PV inverters, is solved by increasing the frequency of the main side band of the common mode voltage above the resonance frequency of the common mode impedance, while avoiding high switching losses. The current control, especially at transitions between the buck and the boost modes of operation is highly improved by utilizing a fast response dead-beat control (DBC) scheme. The working principles of IIDMI are explained in details and a 2.2-kW experimental prototype is implemented to confirm the theoretical achievements.**

***Index Terms*—Dual-mode time-sharing, grid-tied inverter, interleaved, leakage current, transformer-less.**

I. INTRODUCTION

EVER increasing share of residential-based photovoltaic (PV) power generation systems calls for new topologies of interface power electronic converters offering higher efficiencies and lower costs. The common solution is the transformer-less two-stage single-phase converter, which includes a high switching frequency boost chopper to track the maximum power point of the PV panels followed by a full-bridge voltage source inverter (VSI) to generate sinusoidal currents to be injected to the grid. Due to the high number of switching devices operating at high frequencies, the efficiency improvement is a serious challenge with the conventional topology. Besides the efficiency, the size, cost and definitely the quality of the power injected to the grid, as well as the leakage current are major design concerns with a transformer-less PV converter.

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As the most recent advancement to reduce the losses, the dual-mode time-sharing conversion techniques are proposed, which use a time combination of the boost converter and the grid tied inverter to avoid unnecessary high-frequency switching operations [1]–[12]. In these methods, the boost converter is only active when the DC voltage level is lower than the instantaneous value of the grid voltage, while the full bridge inverter stage operates at the grid frequency as a simple unfolding circuit. When the DC voltage level is higher than the instantaneous value of the grid voltage, then the boost stage is inactive and only the step-down inverter operates at a high-frequency to generate the desired output waveform.

A significant improved efficiency than the conventional two stage converters was notified with the basic configuration of these techniques [1]–[3]. However, further efficiency improvement by avoiding any unnecessary switching and conduction losses, maximum utilization of the magnetic circuit and lower leakage current are still matters of interest. Consequently, to tackle some of these issues, several methods are proposed, the main being the zero voltage switching (ZVS) of the boost stage [4], interleaved configuration of the boost stage followed by the H5 and the dual buck inverters [5], dual cascaded boost stage followed by a dual cascaded buck inverter [6] and the quasi-two stage converter [7]. The two stage topology is even more improved by changing the position of the boost and the buck stages, known as the Aalborg inverter [8]–[11]. This lets share the same inductance between the input-buck and the output-boost stages at the price of a discontinuous current at the input and need for larger input power decoupling capacitors. The Aalborg converter suffers from some drawbacks, such as the requirement for two DC sources and an increased number of semiconductor devices. To improve the efficiency and avoid the unbalance of two input DC voltage sources of the Alborg inverter, lately a coupled inductor is used to regulate both input DC sources [12].

To overcome the aforementioned limitations of the transformer-less grid-connected inverter topologies, a new dual-mode time-sharing converter scheme is proposed in this paper, which integrates an interleaved step-down DC-chopper with another interleaved dual-step-up chopper with two polarity selection switches. The proposed converter circuit has the intrinsic ability to be controlled based on a time-sharing

switching technique that highly reduces the conversion losses by avoiding any unnecessary switching and conduction losses in all operation modes. The time-sharing operation principle and the circuit analysis with the equivalent circuits in different operating modes are presented. The common mode voltage and the leakage current are then investigated. The interleaved topology offers increased equivalent switching frequency and improved operation characteristics while reducing the losses and the leakage current. For the three-phase interleaved circuit of this work, the equivalent switching frequency is three-times the PWM frequency and the passing currents through the high frequency semiconductor devices are one-third the output current. Finally, a dead-beat controller (DBC) is developed to calculate the optimal duty cycles in all modes of operation, which ensures a fast and accurate response with a constant switching frequency. More specifically, the operation transitions between the buck and the boost modes, which occur twice a half-cycle with the time-sharing technique, are smooth and seamless with the developed DBC. Finally, various experimental results on a 2.2 kW prototype are presented that confirm the theoretical achievements.

II. Proposed Converter Operation and Design

A. Operation Principles

The circuit diagram of the proposed converter and the basic operation principles of the dual-mode time-sharing control technique are shown in Fig. 1 and Fig. 2, respectively. At the source side, three MOSFETs (S_k), three clamping diodes (D_k) and three inductors (L_k) k∈1,2,3 constitute an interleaved buck converter. The buck stage shares its inductors with the grid-side interleaved dual-boost converter. Apparently, each boost converter consists of interleaved connection of three unidirectional IGBTs ($S_{k,p}$ and $S_{k,n}$). Considering the AC nature of the grid waveform, two polarity selection IGBTs (S_+ and S_-), operating at the line frequency, decide the output voltage polarity according to the grid voltage half-cycle polarity. The boost capacitor (C_C), the grid-side filter inductor (L_g) and the DC link capacitor (C_{DC}) are other required passive components of the proposed converter circuit. The basic idea behind the proposed circuit is to integrate an interleaved step-down DC-chopper with another interleaved dual-step-up chopper. The connection polarity of the output stage to the grid is then determined by the two polarity selection switches. As shown in Fig. 2, whenever the instantaneous absolute value of the grid voltage is lower than the generated DC voltage (V_{PV}) then the buck stage is active and the boost stage in conjunction with the polarity selection switches unfolds the generated voltage by the buck. On the other hand, as long as the DC voltage is lower than the instantaneous absolute value of the grid voltage the buck-switches remain ON and the dual-boost converter is PWM controlled. During the positive half AC line period of the grid voltage, the positive cell works to regulate the injected waveform of the grid current, while the negative one operates in the boost PWM mode. In the next half period, the two cells exchange their operation modes.

According to the previous explanations, the proposed converter circuit is named as the integrated interleaved dual-mode inverter (IIDMI). As already shown in Fig. 1, the interleaving technique is used in both buck and boost stages by connecting three converters in parallel and 120° phase-shifting the switching pulses of parallel converters. Therefore the power capacity is increased and the ripple frequency is tripled that reduces the size of the grid filter inductor, the total output current ripple and increases the main sideband frequency of the common mode voltage, which itself highly reduces the current through the PV parasitic capacitor (C_{PV}).

The equivalent circuits during the operation states of Fig. 2 are illustrated in Fig. 3. Clearly four different topological modes during an AC cycle can be recognized, which are briefly described below:

Mode I, $V_{PV} \geq |+v_g|$ (t_0-t_1 and t_2-t_3): when the PV input DC voltage (V_{PV}) is higher than the grid voltage (v_g) in the positive half cycle, as shown in Figs. 3(a) and (b), then the buck stage is PWM controlled while the positive cell and the positive polarity selection switch, are all continuously ON.

Mode II, $V_{PV} \leq |+v_g|$ (t_1-t_2): when the DC input voltage is lower than the grid voltage in the positive half cycle, as shown in Figs. 3(c) and (d), then the buck switches and the positive polarity selection switch are always on, while the dual-step up stage is PWM controlled.

Mode III, $V_{PV} \geq |-v_g|$ (t_3-t_4 and t_5-t_6): the DC input voltage is higher than the absolute grid voltage in the negative half cycle and as shown in Figs. 3(e) and (f) the operation is similar to Mode I with the only difference that the negative cell and the negative polarity selection switch are ON.

Mode IV, $V_{PV} \leq |-v_g|$ (t_4-t_5): the DC input voltage is lower than the absolute grid voltage in the negative half cycle and as shown in Figs. 3(g) and (h) the operation is similar to Mode II.

Figure 4 illustrates the PWM scheme for the proposed converter. In step-down operation mode, where the control signal $v_{buck\text{-}control}$ is higher than zero, the MOSFETs S_k are PWM controlled and $S_{k,p}$ and S_+ are kept on during the positive half cycle. Similarly, during the negative half cycle the switches $S_{k,n}$ and S_- are on. In step-up operation mode and during the positive half cycle, when the control signal $v_{boost\text{-}control}$ is higher than zero, the IGBTs $S_{k,n}$ are PWM controlled while the switches S_k, $S_{k,p}$ and S_+ are kept on. Similarly, during the negative half cycle

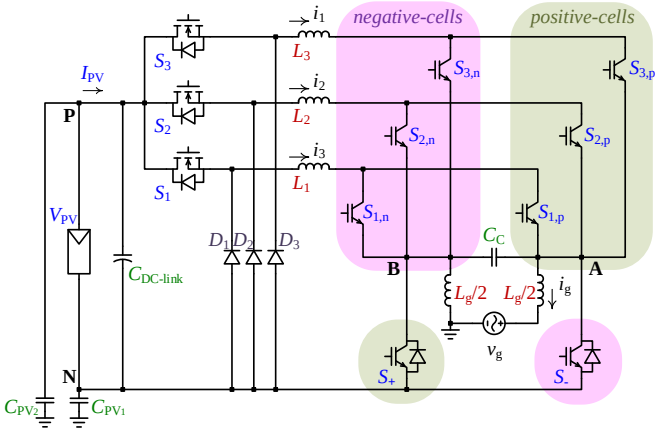

Fig. 1. Circuit diagram of the proposed converter.

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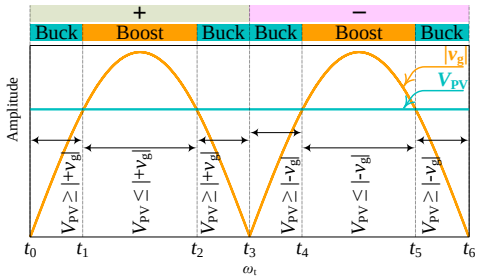

Fig. 2. Operation principle.

the IGBTs $S_{k,p}$ are PWM controlled with S_k, $S_{k,n}$ and S_- being on. Evidently, the three carrier signals have a similar pattern except that they are mutually phase shifted by 120°.

B. Components Design

The C_{DC} performs as a buffer for the instantaneous power difference between the grid and the PV. Thus, to maintain the ripple of the DC-link voltage (ΔV_{DC}) below a specific value, C_{DC} must satisfy the following equation [13].

$$C_{DC} \geq \frac{P_0}{\omega_0 V_{PV} \Delta V_{DC}} \tag{1}$$

where P_0 is the average power, ω_0 is the grid angular frequency and V_{PV} is the PV side DC voltage.

Inductors L_k perform as either buck or boost inductors according to the operation mode. For both operation modes, L_k can be decided with respect to the tolerable current ripple Δi_{Lk}.

The Δi_{Lk} in the buck and the boost operation modes can be calculated as (2) and (3), respectively.

$$\Delta i_{(Lk)}\big|_{buck} = \left[v_g\left(V_{PV} - v_g\right) - I_{Lk}^2\left(r_k + r_g\right)^2\right]\frac{T_s}{L_k V_{PV}} \tag{2}$$

$$\Delta i_{(Lk)}\big|_{boost} = \left(1 - \frac{V_{PV}}{I_g r_g + v_g}\right)\left(V_{PV} - I_{Lk} r_k\right)\frac{T_s}{L_k} \tag{3}$$

where I_{Lk} and r_k are the average inductor current and the equivalent resistance of L_k, I_g and r_g are the average injected grid current and the equivalent resistance of L_g and T_s is the sampling period, which is also the period of carrier waveforms. Thus, after deciding the permissible Δi_{Lk} one can calculate the values of L_k from (4) and (5).

$$L_k\big|_{buck} \geq \left[v_g\left(V_{PV} - v_g\right) - I_{Lk}^2\left(r_k + r_g\right)^2\right]\frac{T_s}{\Delta i_{Lk} V_{PV}} \tag{4}$$

$$L_k\big|_{boost} \geq \left(1 - \frac{V_{PV}}{I_g r_g + v_g}\right)\left(V_{PV} - I_{Lk} r_k\right)\frac{T_s}{\Delta i_{Lk}} \tag{5}$$

To keep the output voltage ripple (Δv_C) below a certain value, the capacitor C_C must satisfy

$$C_C \geq \Delta Q_C / \Delta v_C \tag{6}$$

where ΔQ_C is the total capacitor charge change and can be calculated as [14]

$$\Delta Q_C\big|_{buck} = \Delta i_{Lk} T_s / 8 \tag{7}$$

$$\Delta Q_C\big|_{boost} = I_{Lk} D_{boost}\left(1 - D_{boost}\right) T_s . \tag{8}$$

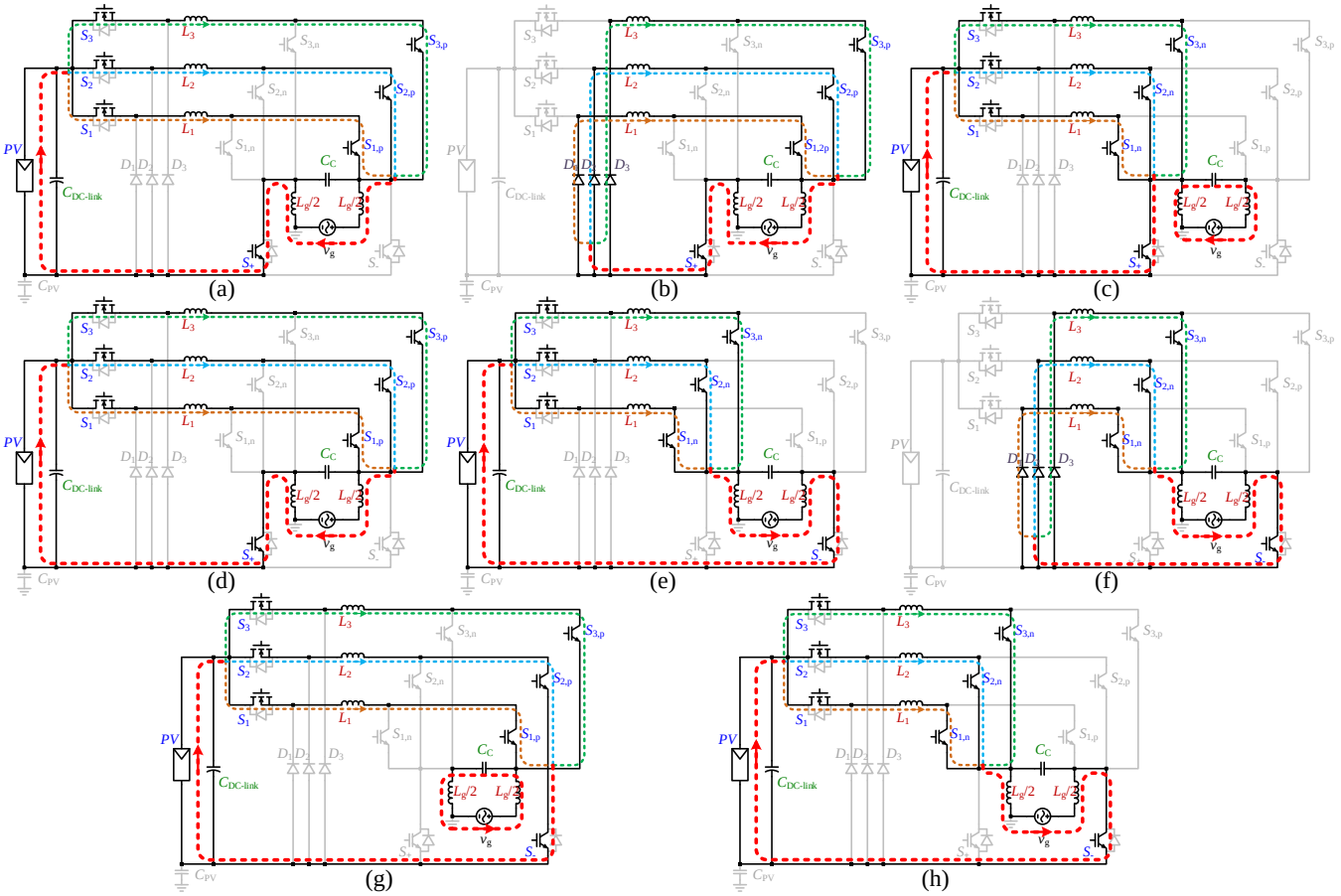

Fig. 3. Topological modes of the proposed converter: Positive half-cycle in buck mode, where (a) S_k is on, (b) free-wheeling current goes through D_k. Positive half-cycle in boost mode, where (c) $S_{k,n}$ is on, (d) $S_{k,p}$ is on. Negative half-cycle in buck mode, where (e) S_k is on, free-wheeling current goes through D_k. Negative half-cycle in boost mode, where (g) $S_{k,p}$ is on, (h) $S_{k,n}$ is on.

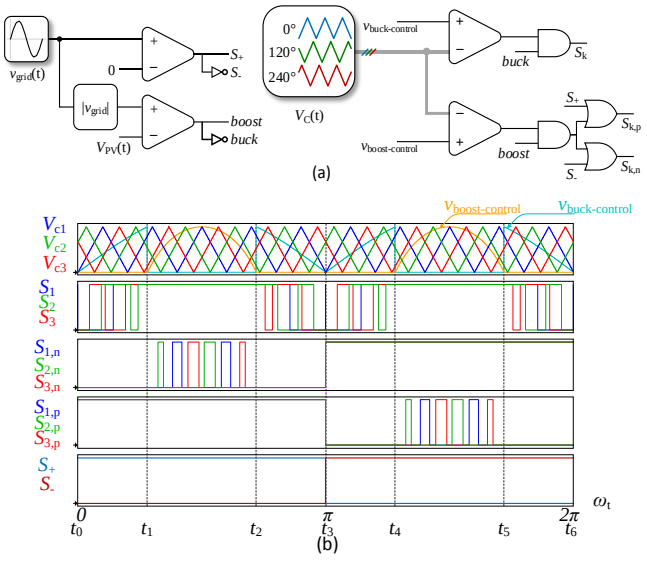

Fig. 4. Modulation strategy: (a) PWM implementation scheme and (b) PWM signals.

The value of grid side inductor, L_g, is chosen from the maximum allowed current ripple, Δi_g, as follows [15]

$$L_g \geq 0.5 T_s \, \Delta v_C / \Delta i_g \, . \tag{9}$$

With considering $v_g = 220\sqrt{2}\sin\omega_0 t$ and V_{PV} in the range of 200 to 400 V, the value of L_k from (4) and (5) can be plotted, as seen in Fig. 5(a), where the current ripple is assumed as 10%. The value of L_k is then chosen as 1 mH.

Figure 5(b) is also plotted by substituting from (7) and (8) in (6) with the assumption that the maximum voltage ripple is 40%. Then the required capacitance is about 2.2 µF.

Finally, from (9) and considering 1% as the maximum tolerable ripple of the injected current, the value of L_g is calculated as 700 µH.

C. Common Mode Analysis

The total parasitic capacitance between the PV panel and the ground is shown as C_{PV} in Fig. 1, which its value depends on the power rating, material, installation and panel frame structure, soil properties, air humidity and other weather conditions. The capacitor C_{PV} provides a common mode path for the leakage current, $i_{leakage}$, induced by the fast changing common mode voltage, V_{CM}. The capacitance varies between 60-110 nF/kW and 100-160 nF/kW for the standard and the thin-film PV modules, respectively [16]. The $i_{leakage}$ deteriorates the waveforms and causes severe damages to the PV panels, which its amplitude is strictly limited by standards [17].

The simple equivalent circuit of the proposed topology is shown in Fig. 6(a). The PV panels under study are assumed to be of standard type, so the total parasitic capacitance, i.e. $C_{PV} = C_{PV1}+C_{PV2}$ is considered in the range of 60-160 nF/kW. The ground resistance, R_g, is equal to 2 Ω in accordance to IEEE standard requirements [18]. In Fig. 6(b), the switching stages are replaced by PWM voltage sources; besides, V_{Sk} is the drain-source voltage of S_k, similarly, collector-emitter voltage of $S_{k,n}$ and $S_{k,p}$ are $V_{Sk,n}$ and $V_{Sk,p}$, respectively and V_{Lk} is the voltage across the inductor. To focus the analysis on $i_{leakage}$, the equivalent circuit, ignoring the grid is shown in Fig. 6(c), where the path of common-mode (dashed line) and differential-mode (dotted line) currents are depicted. With L_{g1} equal to L_{g2}, the effect of differential mode voltage can be neglected and only the common mode circuit is shown in Fig. 6(d). Therefore V_{CM}, $i_{leakage}$ and the common mode impedance (Z_{CM}) are defined as follows.

$$V_{CM} = \left(V_{AN} + V_{BN}\right)/2 \tag{10}$$

$$i_{leakage}(s) = V_{CM}(s)/Z_{CM}(s) \tag{11}$$

$$Z_{CM}(s) = 0.5 L_g s + R_g + \frac{1}{sC_{PV}} \tag{12}$$

The Bode magnitude plot of Z_{CM} is plotted in Fig. 7. It can be deduced that by increasing the equivalent switching frequency, f_s, beyond the resonance frequency of the common mode impedance ($f_{r,ZCM}$) the magnitude of Z_{CM} increases considerably and consequently $i_{leakage}$ is suppressed. Also as mentioned in [19], $f_{r,ZCM}$ must be much higher than the grid frequency, f_0, and at the same time much lower than the first switching sideband to avoid excessive $i_{leakage}$, i.e.

$$f_0 \ll f_{r,ZCM} \ll f_s \tag{13}$$

The equivalent switching frequency and consequently the first switching sideband frequency is three-times the frequency of PWM carrier signals, f_c. For our case and with f_c = 10 kHz, then the equivalent switching frequency is f_s = 30 kHz and evidently from Fig. 7 the $i_{leakage}$ is effectively attenuated with the high Z_{CM}. Therefore, increasing the equivalent switching frequency to 30 kHz with interleave connection of three converters, each operating at 10 kHz, provides a much wider affordable range for $f_{r,ZCM}$ with enough magnitude attenuation for $i_{leakage}$.

The transfer function of V_{CM} is expressed from (11) and (12) by

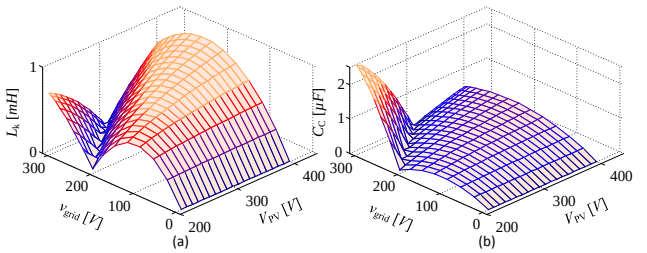

Fig. 5. Selection of: (a) L_k and (b) C_C.

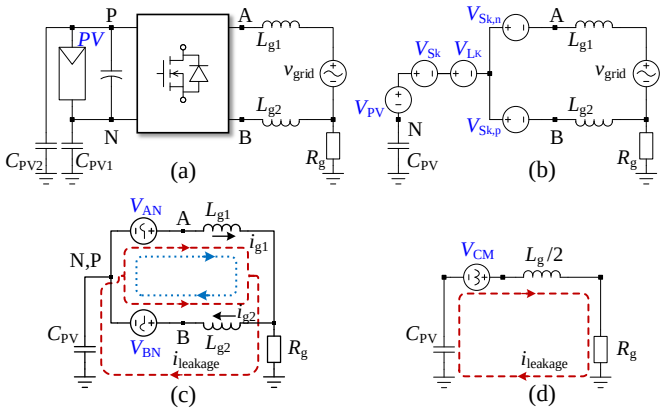

Fig. 6. (a) Simple equivalent circuit; (b) with PWM voltage source and grid; (c) with pole voltage; (d) Simplified common mode model.

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$$V_{CM}(s)=\left(0.5L_g s+R_g\right)i_{leakage}(s)-V_{CPV}(s) \tag{14}$$

where $i_{leakage}(s) = i_{g1}(s) - i_{g2}(s)$.

Based on (14) and the transfer functions of $i_{leakage}(s)$ and $V_{CPV}(s)$, which can be derived from the averaged state-space model of the converter, already given in Appendix, the transfer functions of the switching function S and v_g to the V_{CM} can be determined. The magnitude Bode plots of $V_{CM}(s)/S(s)$ and $V_{CM}(s)/v_g(s)$ in the buck and boost modes are plotted in Fig. 8.

For the sake of simplicity, V_{CM} can be analyzed in the low frequency range ($V_{CM,LF}$) around the DC and the baseband harmonics and the high frequency range ($V_{CM,HF}$) at discrete switching sideband harmonics. The low-frequency (*LF*) components of V_{CM} are also a composition of buck ($V_{CM,LF,buck}$) and boost ($V_{CM,LF,boost}$) components, i.e.

$$V_{CM,LF}=V_{CM,LF,buck}+V_{CM,LF,boost} \tag{15}$$

The *LF* components of V_{CM} are formulated as

$$V_{CM,LF,buck}=\left|\frac{\hat{V}_{CM,buck}(s)}{\hat{S}(s)}\right|S(\omega t)+\left|\frac{\hat{V}_{CM,buck}(s)}{\hat{v}_g(s)}\right|v_g(\omega t)= \frac{L_g V_{PV}}{L_g+L_k}\left[C_{00}+\sum_{n=1}^{\infty}C_{0n}\right]+\frac{L_k}{L_g+L_k}\sum_{n=1,3,\ldots}^{\infty}\left|v_{g,n}\right| \tag{16}$$

$$V_{CM,LF,boost}=\left|\frac{\hat{V}_{CM,boost}(s)}{\hat{S}(s)}\right|S(\omega t)+\left|\frac{\hat{V}_{CM,boost}(s)}{\hat{v}_g(s)}\right|v_g(\omega t)= \frac{L_g V_{PV}}{(1-D)^2 L_g+L_k}\left[C_{00}+\sum_{n=1}^{\infty}C_{0n}\right]+\frac{L_k}{(1-D)^2 L_g+L_k}\sum_{n=1,3,\ldots}^{\infty}\left|v_{g,n}\right| \tag{17}$$

where C_{00} and C_{0n} corresponds to the DC and the baseband harmonics, respectively in the Fourier series of the switching function, given below.

$$S(\omega t)=C_{00}+\sum_{n=1}^{\infty}C_{0n}\cos 2n\omega_0 t+\sum_{m=1}^{\infty}C_{m0}\cos m\omega_s t+\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}C_{mn}\cos\left(m\omega_s t+n\omega_0 t\right) \tag{18}$$

Similarly, the high-frequency (*HF*) components of V_{CM} in the buck and the boost modes are presented as

$$V_{CM,HF}=V_{CM,HF,buck}+V_{CM,HF,boost} \tag{19}$$

where

$$V_{CM,HF,buck}=\left|\frac{\hat{V}_{CM,buck}(s)}{\hat{S}(s)}\right|S(\omega t)=\frac{V_{PV}}{\omega_s^2 C_C L_k}\left[\sum_{m=1}^{\infty}C_{m0}+\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}C_{mn}\right] \tag{20}$$

$$V_{CM,HF,boost}=\left|\frac{\hat{V}_{CM,boost}(s)}{\hat{S}(s)}\right|S(\omega t)=\frac{I_{Lk}V_{PV}}{\omega_s C_C}\left[\sum_{m=1}^{\infty}C_{m0}+\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}C_{mn}\right] \tag{21}$$

where, C_{m0} and C_{mn} are the carrier and the sideband harmonics coefficients, respectively.

Following a procedure already described in [20], [21], the Fourier series coefficients in the buck and the boost modes can be derived for the proposed converter and the results are presented in (22) and (23), where M is the modulation index, $J_k(x)$ is the Bessel function of the first kind and $\psi=\cos^{-1}(1/M)$.

Obvious from (20) and (21) the amplitude of the high-frequency components of V_{CM} in the buck and the boost modes are inverse proportional to the square of the switching frequency ($|V_{CM,HF,buck}| \propto 1/\omega_s^2$) and the switching frequency itself ($|V_{CM,HF,boost}| \propto 1/\omega_s$), respectively, while the low frequency components remain unchanged.

The harmonic spectrum of V_{CM} from (15) and (19) is shown in Fig. 9, which again confirms that by increasing the equivalent switching frequency by interleaving technique, the low frequency components of V_{CM} are not affected, but the high frequency contents are drastically attenuated and from (11), $i_{leakage}$ will be reduced.

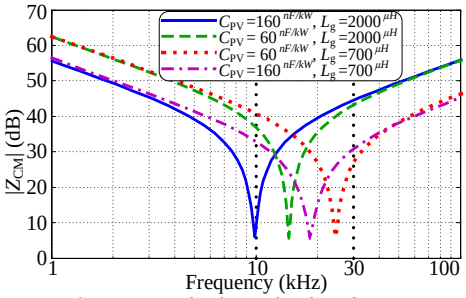

Fig. 7. Magnitude Bode plot of Z_{CM}.

buck mode:

$$C_{00}=\frac{2}{\pi}\left[\psi+M(1-\sin\psi)\right],\quad C_{0n}=\frac{2\sin 2n\psi}{n\pi}-\frac{4M}{\pi(4n^2-1)}\left[\cos n\psi(1-\sin\psi)-n\cos\psi\sin n\psi\right]$$

$$C_{m0}=\frac{4\psi\sin m\pi}{m\pi^2}+8\sum_{k=1}^{\infty}\frac{J_k(m\pi M)}{mk\pi^2}\sin\frac{k\pi}{2}\left(\sin\frac{k\pi}{2}-\sin k\psi\right) \tag{22}$$

$$C_{mn}=\frac{2\sin m\psi\sin 2n\psi}{mn\pi^2}+8\sum_{k=1}^{\infty}\frac{J_{2k-1}(m\pi M)\sin\frac{(2k-1)\pi}{2}}{m\pi^2(2k-1+2n)(2k-1-2n)}\left\{\begin{array}{l}-2n\left[\cos(2k-1)\psi\sin 2n\psi\right]+\\ (2k-1)\left[\cos 2n\psi\sin(2k-1)\psi+\sin\frac{(2k-1)\pi}{2}\cos n\pi\right]\end{array}\right\}$$

boost mode:

$$C_{00}=\frac{M}{2\pi}\left[2\psi+\sin\psi\right],\quad C_{0n}=-\frac{4M}{\pi(4n^2-1)}\left[\cos n\psi\sin\psi-n\cos\psi\sin n\psi\right],\quad C_{m0}=8\sum_{k=1}^{\infty}\frac{J_k(m\pi M)}{mk\pi^2}\sin\frac{k\pi}{2}\sin k\psi \tag{23}$$

$$C_{mn}=8\sum_{k=1}^{\infty}\frac{J_{2k-1}(m\pi M)\sin\frac{(2k-1)\pi}{2}}{m\pi^2(2k-1+2n)(2k-1-2n)}\left\{-2n\left[\cos(2k-1)\psi\sin 2n\psi\right]+(2k-1)\left[\cos 2n\psi\sin(2k-1)\psi\right]\right\}$$

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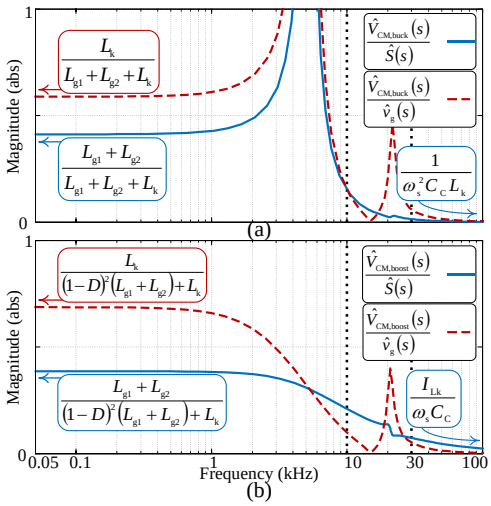

Fig. 8. Magnitude characteristic of (a) buck and (b) boost mode of operation.

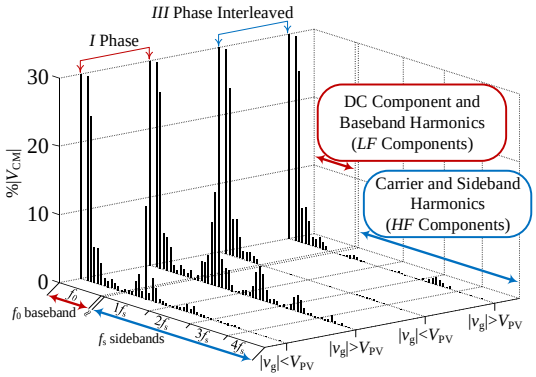

Fig. 9. Calculated V_{CM} harmonics spectrum in different modes.

III. CONTROL OF IIDMI

For unity power factor operation the current through L_g, shown as i_g, must be controlled as a sinusoid in phase with the grid voltage. As [11] has already proposed, in this work the indirect control of the converter through adjusting the current of L_k instead of i_g is adopted. Neglecting the losses, the following equation can be written

$$V_{PV}(t)\sum_{k=1}^{3} i_{Lk}(t) = v_g(t) i_g(t) \tag{24}$$

Based on (24), one can readily conclude that instead of i_g, the current i_{Lk} can be compensated. This rectified sinusoidal current can be regulated by directly calculating the optimal duty cycle for the next switching period by a dead-beat strategy [22]. As

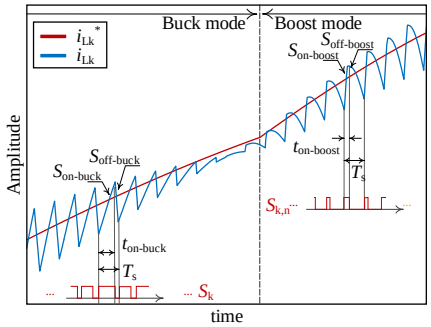

Fig. 10. Inductor L_k current of IIDMI in each mode.

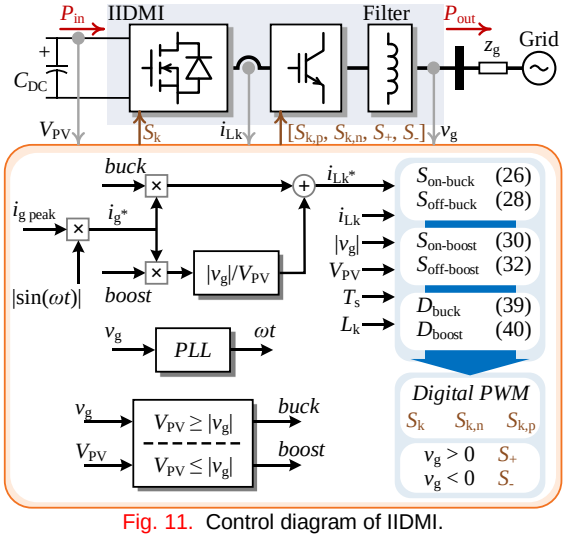

Fig. 11. Control diagram of IIDMI.

will be shown, the simple yet efficient dead-beat control technique only requires the value of L_k to directly calculate the switches duty cycles from the measured source and grid voltages, measured inductor current and its reference.

As shown in Fig. 10, in the buck operation mode, when S_k is ON, the voltage across the inductor L_k can be determined as

$$V_{Lk} = L_k \frac{di_{Lk}}{dt} = V_{PV} - v_g \tag{25}$$

The slope of the inductor current in S_k ON state ($S_{on\text{-}buck}$) can be determined as

$$S_{on\text{-}buck} = \frac{di_{Lk}}{dt} = \frac{V_{PV} - v_g}{L_k} \tag{26}$$

Similarly, when the switch S_k is OFF, the inductor voltage is

$$V_{Lk} = L_k \frac{di_{Lk}}{dt} = -v_g \tag{27}$$

The slope of the inductor current in S_k OFF state ($S_{off\text{-}buck}$) is

$$S_{off\text{-}buck} = \frac{di_{Lk}}{dt} = \frac{-v_g}{L_k} \tag{28}$$

In the boost operation mode, when $S_{k,n}$ is ON, the inductor voltage and the slope of the inductor current ($S_{on\text{-}boost}$) are

$$V_{Lk} = L_k \frac{di_{Lk}}{dt} = V_{PV} \tag{29}$$

$$S_{on\text{-}boost} = \frac{di_{Lk}}{dt} = \frac{V_{PV}}{L_k} \tag{30}$$

Similarly, when $S_{k,n}$ is OFF, the inductor voltage and the slope of the inductor current ($S_{off\text{-}boost}$) are

$$V_{Lk} = L_k \frac{di_{Lk}}{dt} = V_{PV} - v_g \tag{31}$$

$$S_{off\text{-}boost} = \frac{di_{Lk}}{dt} = \frac{V_{PV} - v_g}{L_k} \tag{32}$$

Now one can predict the inductor current at the next sampling period ($i_{Lk}[t+1]$) from its current value ($i_{Lk}[t]$), by using the slopes already given by (26) and (28) for the buck and by (30) and (32) for the boost modes of operation, i.e.

$$i_{Lk}[t+1] = i_{Lk}[t] + S_{on-buck} t_{on-buck} + S_{off-buck} t_{off-buck} \tag{33}$$

$$i_{Lk}[t+1] = i_{Lk}[t] + S_{on-boost}t_{on-boost} + S_{off-boost}t_{off-boost} \quad (34)$$

where $t_{on\text{-}buck}$ is the S_k ON state time, $t_{off\text{-}buck}$ is the S_k OFF state time during the buck operation and $t_{on\text{-}boost}$ is the $S_{k,n}$ ON state time, and $t_{off\text{-}boost}$ is the $S_{k,n}$ OFF state time during the boost operation.

By forcing the error between the reference current (i_{Lk}^*) and $i_{Lk}[t+1]$, depicted as i_{err}, to be zero, then

$$i_{err} = i_{Lk}^* - i_{Lk}[t+1] = \quad (35)$$
$$i_{Lk}^* - i_{Lk}[t] - S_{on-buck}t_{on-buck} - S_{off-buck}t_{off-buck} = 0$$

$$i_{err} = i_{Lk}^* - i_{Lk}[t+1] = \quad (36)$$
$$i_{Lk}^* - i_{Lk}[t] - S_{on-boost}t_{on-boost} - S_{off-boost}t_{off-boost} = 0$$

Therefore, $t_{on\text{-}buck}$ and $t_{on\text{-}boost}$ can be determined as

$$t_{on-buck} = \frac{i_{Lk}^* - i_{Lk}[t] - (S_{off-buck}T_s)}{S_{on-buck} - S_{off-buck}} \quad (37)$$

$$t_{on-boost} = \frac{i_{Lk}^* - i_{Lk}[t] - (S_{off-boost}T_s)}{S_{on-boost} - S_{off-boost}} \quad (38)$$

Using (37) and (38), the optimal duty cycles can be calculated as

$$D_{buck} = \frac{t_{on-buck}}{T_{samp}} = \frac{i_{Lk}^* - i_{Lk}[t] - (S_{off-buck}T_s)}{(S_{on-buck} - S_{off-buck})T_s} \quad (39)$$

$$D_{boost} = \frac{t_{on-boost}}{T_{samp}} = \frac{i_{Lk}^* - i_{Lk}[t] - (S_{off-boost}T_s)}{(S_{on-boost} - S_{off-boost})T_s} \quad (40)$$

It must be mentioned that the average current through the inductor L_k in each period is equal to the average current injected to the grid, since the average current of C_C is zero at the steady-state. Therefore, one can readily conclude that

$$i_{Lk}^* = \begin{cases} |i_g^*| & V_{PV} \geq |v_g| \\ |i_g^*||v_g|/V_{PV} & V_{PV} \leq |v_g| \end{cases} \quad (41)$$

where i_g^* is the reference grid current.

The simplified control diagram of IIDMI is shown in Fig. 11. By comparing the instantaneous grid voltage and the PV voltage, either buck or boost mode of operation is determined and consequently the reference current i_{Lk}^* is decided. This reference value and the measured current i_{Lk} are then fed to the DBC algorithm, which directly calculates the optimal duty cycles as already described above. A PWM modulator generates the switching pulses from the calculated duty cycles.

IV. Performance Evaluation

In order to support the theoretical achievements, a 2.2 kW laboratory prototype, shown in Fig. 12, is developed with the parameters listed in TABLE I. A STMicroelectronics STM32F407 floating point digital signal controller is used to implement the control algorithm.

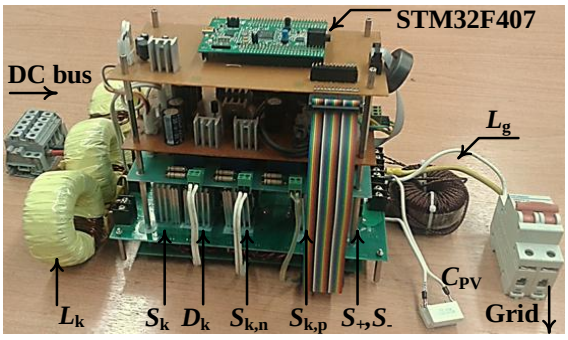

Fig. 12. Experimental hardware prototype.

Figures 13(a) and (b) show the steady-state performance of the converter in the buck (V_{PV} = 350 V) and the buck and boost (V_{PV} = 200 V) modes, respectively both with 2.2 kW output power. As already discussed, with V_{PV} = 350 V the boosting operation is not required and only S_k is working.

In Fig. 13(b) the measured waveforms of the IIDMI when the input PV voltage is 200 V are plotted. As can be seen in the figure, the buck and the boost switches do not work simultaneously, i.e. $S_{k,n}$ and $S_{k,p}$ are PWM controlled only when V_{PV} is lower than the instantaneous grid voltage and S_k is PWM controlled only when V_{PV} is higher than the instantaneous grid voltage. Obviously, the proposed converter with the DBC algorithm can provide a highly sinusoidal currents even with a harmonically polluted grid voltage as the current THD remains much below the specific requirements by standards, such as IEEE519 [23].

Figures 14(a) and (b) show the zoomed view of the grid current and i_{Lk} during transients from negative to positive half cycles and the buck to the boost modes of operation, respectively. Clearly, the grid current experiences a negligible distortion at transitions from the negative to the positive half-cycles. The same performance is already observed during the positive to the negative transition. The mode transition, demonstrated in Fig. 14(b), occurs with almost no detectable transients in the output current. The fast yet smooth current control transient performance is mainly attributed to the interleaved topology as well as the optimal duty cycle adjustment by the DBC.

The transient performance of the converter to step jumps of the input DC voltage (from 200 to 350 V) and the reference current amplitude (from half to full load) are demonstrated in Figs. 15(a) and (b), respectively. Figure 15(a) indicates that a high step change in the PV voltage almost has no effect on the output current waveform. Figure 15(b) again confirms the very fast and at the same time accurate dynamic current control performance of the proposed converter with the DBC control algorithm. The DBC provides some kind of prediction that highly enhances its dynamic performance in response to possible changes in the reference, inputs and disturbances.

As already mentioned, the leakage current is a major

TABLE I
Experimental Setup Parameters

Parameter	Value
Input voltage	200 to 350 V
Grid voltage	220 V / 50 Hz
Switching and sampling frequency	10 kHz
Inductor L_k	1 mH
Inductor L_g	0.7 mH
Capacitor C_C	2.2 µF
MOSFET switches S_k	SPW35N60CFD
Diodes D_k	IDW16G65C5
IGBT switches $S_{k,n}$ and $S_{k,p}$	IXGH48N60C3
IGBT switches S_+ and S_-	IXGH48N60A3
Gate drivers	TLP250 from Toshiba
Voltage and current sensors	LV25P and LTS25 NP from LEM

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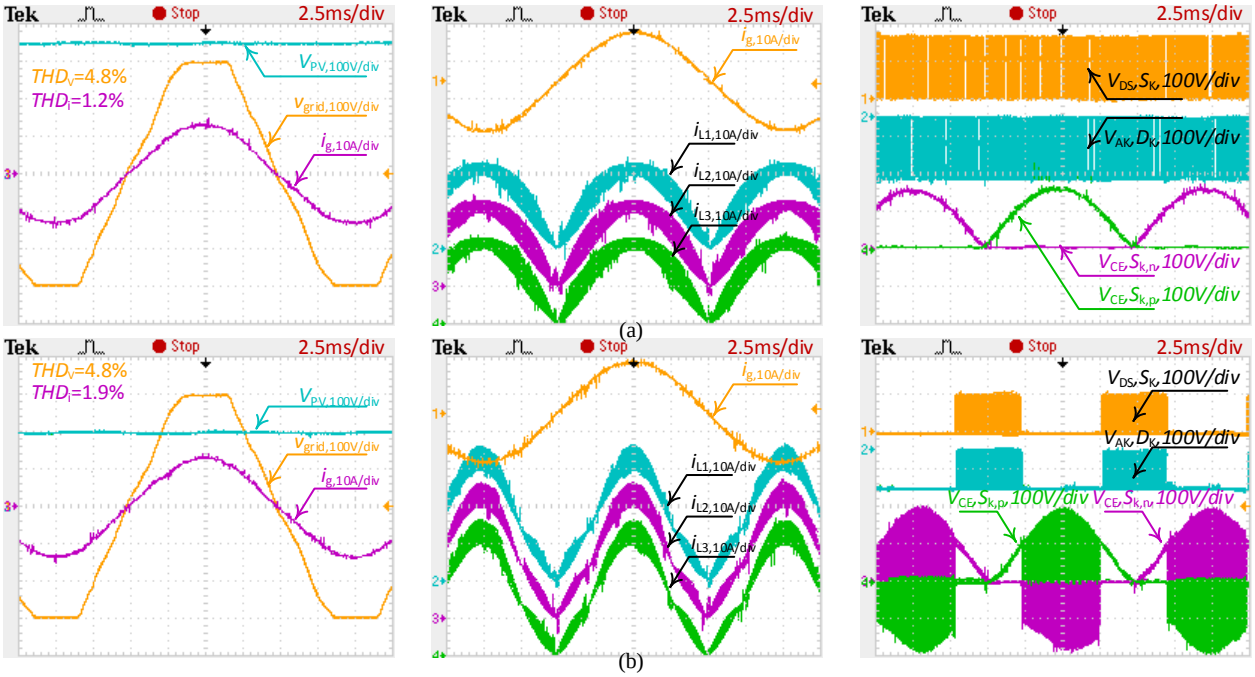

Fig. 13. Waveforms of PV voltage (V_{PV}), grid voltage (v_{grid}), grid current (i_g), inductor current (i_{Lk}), drain-source voltage of S_k, anode-cathode voltage of D_k, and collector-emitter voltage of $S_{k,n}$,$S_{k,p}$ when: (a) V_{PV} = 350 V and (b) V_{PV} = 200 V.

performance criteria that must be assessed for any grid connected PV converter. Figure 16 shows the experimental results of the common mode voltage and the resultant leakage current under different PV voltage levels. Obviously the HF component of the common mode voltage occurs at 30 kHz, which is three-times the switching frequency and outside the possible range of resonance frequency of the common mode impedance. As the result, the RMS value of the grid leakage current lies far below the standard requirements, for example the limit of 30 mA defined by [17]. The measured RMS currents are in close agreement with the analytical results presented in Section II.C.

As mentioned before, the DBC needs the value of L_k to predict the optimal duty cycle. As a result, the performance of the DBC, considering the L_k mismatches, denoted by ΔL_k, must be investigated. The performance of the controller, in terms of the THD of the injected current, with the mismatches in L_k is shown in Fig. 17. To obtain the results, the real value of L_k is fixed for all tests and only the used value in the controller algorithm is intentionally chosen different from its real value. The stable operation of the proposed DBC even with high mismatches is obvious. Besides the THD of the injected current remains below the standard requirement of 5%. The measured THD at different power levels are also presented in Fig. 18 (a). It is worth mentioning that for all tests the THD of the grid voltage is about 4.8% with the 3rd, 5th, 7th and 9th voltage harmonic orders as 3.9%, 2.5%, 0.6% and 0.9%, respectively. An important feature of the proposed dual-mode time-sharing converter is the reduced losses. This is investigated experimentally with input voltages of 200 V and 350 V. The results are plotted in Fig. 18 (b). As already expected, a very high peak efficiency of 98.4% is obtained. At all power and input voltage levels the efficiency is above 94%.

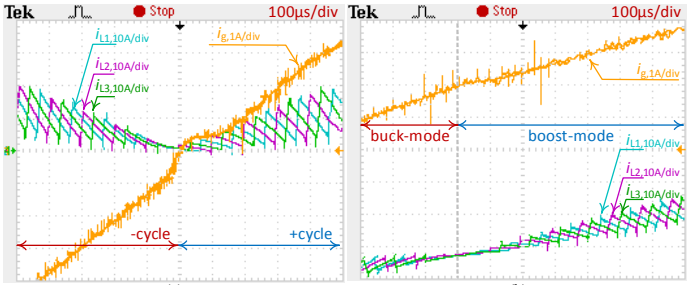

Fig. 14. Zoomed view of i_g and i_{Lk} at transition from (a) negative to positive half-cycle of grid and (b) buck to boost mode of operation.

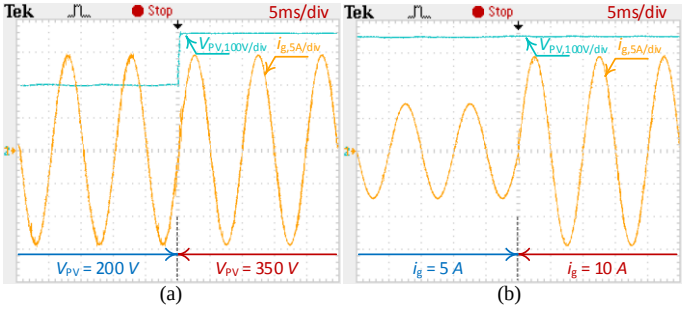

Fig. 15. Grid-injected current when: (a) the V_{PV} changes from 200 to 350 V. (b) the power changes from 1100 to 2200 W.

TABLE II

COMPARISON BETWEEN DIFFERENT STRUCTURES

Dual-mode inverter topologies	Power (W)	Peak efficiency	leakage current
Boost full-bridge [4]	1600	< 97%	High
Interleaved boost-full bridge [7]	2500	97.77%	High
Interleaved boost-H5 [7]	2500	97.64%	Low
Interleaved boost-dual buck [7]	2500	98.11%	High
Dual-mode cascaded [2]	3500	< 97%	-
Boost-buck [5]	1000	97.8%	Low
Aalborg [11]	2000	98.18%	-
Proposed	2200	98.4%	Low

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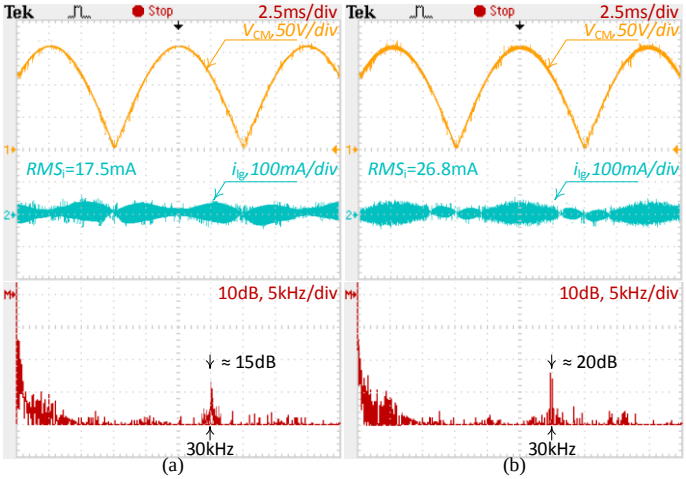

Fig. 16. Waveforms of V_{CM}, $i_{leakage}$ and harmonic spectrum of V_{CM} for the IIDMI topology when: (a) V_{PV} = 350 V and (b) V_{PV} = 200 V.

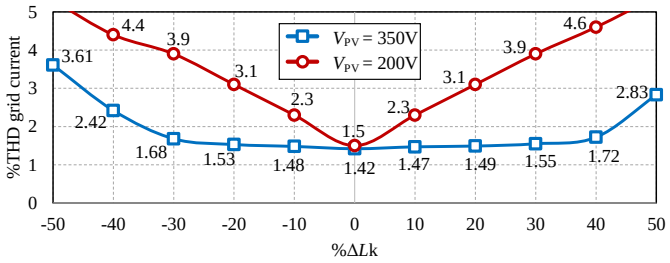

Fig. 17. Grid-injected current %THD versus inductance mismatch at the rated power.

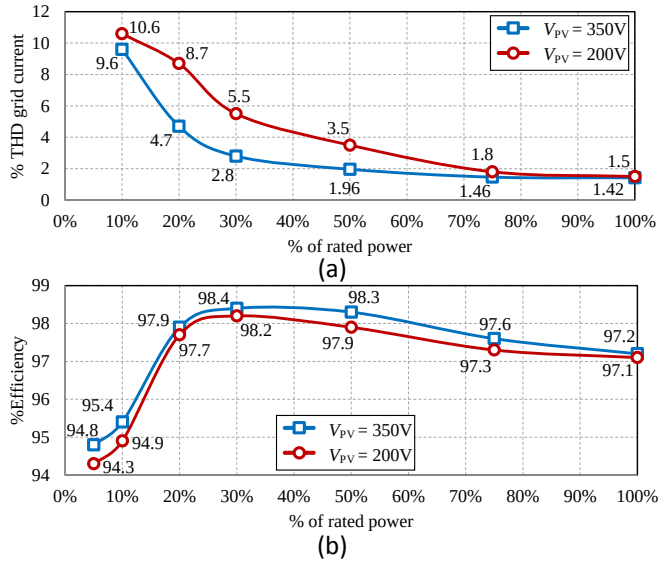

Fig. 18. (a) %THD of the grid-injected current and (b) %efficiency versus different power levels with two input DC voltages.

From Fig. 18 (b), the European Efficiency (EU) and the California Energy Commission (CEC), can be readily calculated as 97.76% and 97.75% (V_{PV} = 350 V) and 97.26% and 97.4% (V_{PV} = 200 V), respectively.

A numerical comparison of the efficiency and the leakage current among the proposed inverter and the available dual-mode time-sharing inverter topologies is presented in TABLE II. As can be seen, the leakage current is low and the efficiency is the highest among the competitors.

V. Conclusion

This paper proposes a novel dual-mode time-sharing converter by integration of a step-down and a dual step-up chopper, both with the interleaved topology. A fast and accurate control scheme based on the DBC is then proposed for the proposed converter, which simplifies its control and improves its performance, especially at mode transitions. Based on the theoretical analysis and the experimental results, the proposed converter has the following main advantages:

1) it retains the advantages of interleaved technology as follows: increasing the equivalent switching frequency, reducing the switching frequency of individual devices, reducing the output current ripple, decreasing the THD of the output current, increasing the frequency of main side-band of V_{CM} to reduce the leakage current through the C_{PV};
2) it retains the advantages of the dual-mode time-sharing inverters as follows: high conversion efficiency, only one power stage of buck or boost works in the high frequency stage at any time, which avoids unnecessary switching losses;
3) it retains the advantages of the DBC and indirect control as follows: fast response because it directly calculates the optimal duty cycles, high quality grid current, fast and smooth transitions between the buck and boost modes of operation;

Finally, the IIDMI effectively increases the conversion efficiency and decreases the leakage current, which makes it a reliable and efficient candidate for modern PV applications.

Appendix

Proposed Converter State-Space Model

The average state-space representation of the proposed converter can be obtained as

$$\dot{x}(t) = A_{\text{buck/boost}}x(t) + B_{\text{buck/boost}}u(t) \tag{42}$$

where $x = [i_{Lk}, i_{g1}, i_{g2}, v_C, v_{CPV}]^T$, $u = [S, v_g]^T$ and A and B for the buck and the boost modes of operation are:

$$A_{\text{buck}} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_k} & 0 \\ 0 & \frac{-R_g}{L_{g1}} & \frac{R_g}{L_{g1}} & \frac{1}{L_{g1}} & \frac{1}{L_{g1}} \\ 0 & \frac{R_g}{L_{g2}} & \frac{-R_g}{L_{g2}} & 0 & \frac{-1}{L_{g2}} \\ \frac{1}{C_C} & \frac{-1}{C_C} & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{PV}} & \frac{1}{C_{PV}} & 0 & 0 \end{bmatrix}, B_{\text{buck}} = \begin{bmatrix} \frac{1}{L_k} & 0 \\ 0 & \frac{-1}{L_{g1}} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{43}$$

$$A_{\text{boost}}=\begin{bmatrix} 0 & 0 & 0 & \frac{D-1}{L_{\text{k}}} & 0 \\ 0 & \frac{-R_{\text{g}}}{L_{\text{g1}}} & \frac{R_{\text{g}}}{L_{\text{g1}}} & \frac{1}{L_{\text{g1}}} & \frac{1}{L_{\text{g1}}} \\ 0 & \frac{R_{\text{g}}}{L_{\text{f2}}} & \frac{-R_{\text{g}}}{L_{\text{f2}}} & 0 & \frac{-1}{L_{\text{f2}}} \\ \frac{D-1}{C_{\text{C}}} & \frac{1}{C_{\text{C}}} & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{\text{PV}}} & \frac{1}{C_{\text{PV}}} & 0 & 0 \end{bmatrix}, B_{\text{boost}}=\begin{bmatrix} \frac{1}{L_{\text{k}}} & 0 \\ 0 & \frac{-1}{L_{\text{g1}}} \\ 0 & 0 \\ \frac{I_{\text{Lk}}}{C_{\text{C}}} & 0 \\ 0 & 0 \end{bmatrix} \quad (44)$$

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