A High Gain Buck PFC Synchronous Rectifier

Saeed Sharifi
Ferdowsi University of Mashhad
Mashhad, Iran
saeed.sharifi@mail.um.ac.ir

Mohammad Babaei
Ferdowsi University of Mashhad
Mashhad, Iran
mohammad.babaei@mail.um.ac.ir

Mohammad Monfared
Ferdowsi University of Mashhad
Mashhad, Iran
m.monfared@um.ac.ir

***Abstract*—This paper presents a high gain buck PFC synchronous rectifier which offers a high efficiency rectification and high quality waveforms. The Z-source network applied to the rectifier, helps to highly increase the quality of input current of the conventional rectifier. The input inductor of this Z-source network provides smooth and pure sine waveform for the AC source current. In addition, applying this Z-source network allows to decrease the high AC input voltage to a very low output voltage required for low voltage loads such as LED drivers. Also, the synchronous buck rectifier utilization with the simple average current control (ACC) method offers less power losses compared to conventional buck rectifier, in addition to less control complexity. The steady state operations of the proposed PFC rectifier are theoretically derived and analyzed. Then, the concept and the supremacy of the proposed PFC rectifier are verified through a set of simulations for a 48Vdc/500W rectifier.**

Keywords—High gain buck, power factor correction, synchronous rectifier, Z-source network

I. INTRODUCTION

The AC/DC converters supplies the loads in many applications such as UPS, telecom, chargers and adapters. The AC/DC converters are designed to reduce the harmonic content of the input current to meet power products requirements such as lighting equipments. These converters usually consist of two stage of the power converters combining the power factor corrector (PFC) and the DC/DC stage as shown in Fig. 1. In the PFC stage, the AC input voltage is converted to DC voltage with nearly unity PF and low total harmonic distortion (THD). The boost converter is the most popular PFC topology, in which the input inductor current can be easily shaped in the form of a pure rectified sine waveform [1]–[4] The boost type PFC converters suffer from many drawbacks which include the DC output voltage which is always higher than the peak input voltage, the input to output isolation cannot be implemented easily, the startup inrush current is high, and there is a lack of current limiting during overload conditions [5]. However, its important drawback remains the control detuning phenomenon that it presents at the zero-crossings of the source voltage, which increases the distortion of source current and restrict the performance of this type of PFC rectifier [2]. These drawbacks of a boost PFC pre-regulator can be overcome by using a buck converter for the rectifier [6]. The buck PFC converter has higher low-line efficiency and lower EMI noise compared to the boost PFC converter. The buck PFC rectifier has some attractive merits. First, the output voltage of buck converter is always regulated lower than the boost converter. Second, the voltage across the main switch of the buck converter is almost clamped to the input voltage [7] and [8]. Therefore, the buck PFC rectifier can achieve relatively high efficiency within the universal input voltage range. The traditional buck PFC rectifier and its steady state operation waveforms are shown in Fig. 2. Due to the inherent dead angle in the input current when the input voltage is lower than the output voltage, the buck PFC usually has limited PF and high current distortion, which is hard to meet the current harmonic requirements. The buck power factor correction has attracted a lot of research interests for its low output voltage and high efficiency at low input condition. However, the traditional buck PFC converter usually has low power factor (PF) and poor harmonic performance due to the inherent dead angle of the input current, especially at low input condition [9].

This paper introduces a PFC rectifier utilizing the Z-source networks to alleviate some of the aforementioned shortcomings of the conventional buck rectifier. At the same time, with the Z-source employment, the power conversion is achieved using only one stage of the power converter leading to less converter size and cost as in [10] and [11]. Also, very low step-down gains can be easily achieved due to the high gain buck operation of the rectifier which allows to simply increase the switching frequency and thus, lowering the passive elements size. The advantages of the proposed PFC rectifier makes it

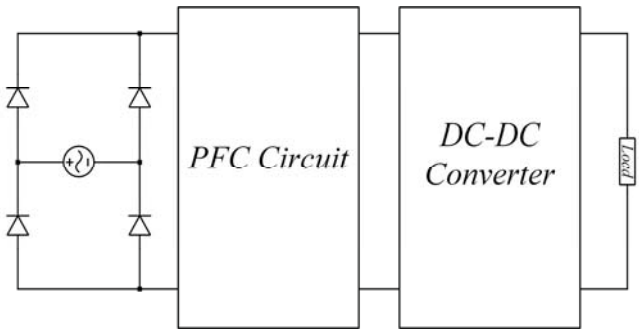

Fig. 1. Conventional AC/DC power supply.

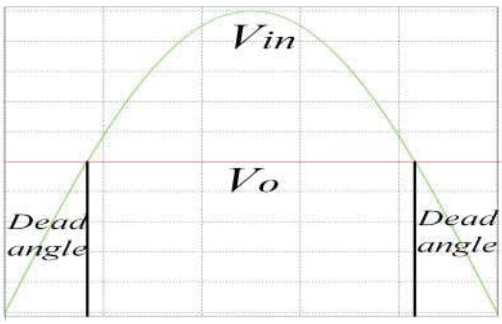

Fig. 2. Input voltage and dead angle of a PFC buck rectifier.

978-1-5386-4916-9/18/$31.00 ©2018 IEEE

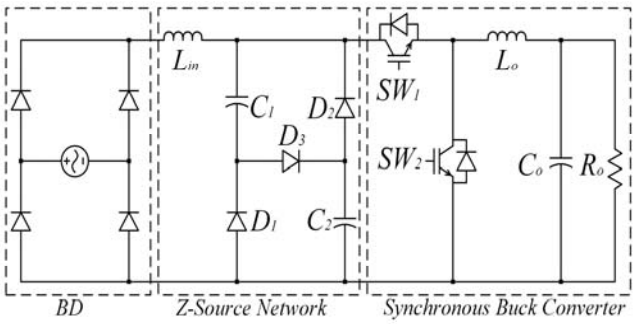

Fig. 3. Circuit configuration of the proposed PFC rectifier.

suitable for different applications such as telecom and electric vehicles (EVs) chargers [12]. All modes of the operation of the proposed PFC rectifier are theoretically analyzed and then successfully supported by the simulations.

II. Proposed Rectifier Circuit and Performance Analysis

A. Circuit Configuration

The circuit configuration of the proposed single-phase high gain buck synchronous power factor correction (PFC) rectifier is shown in Fig. 3. As can be seen from this figure, the proposed rectifier is realized by applying a diode bridge for the input voltage rectification, a Z-source network and the buck converter which serves the output load and steps down the DC-link voltage as a switching converter. The Z-source network consists of the input inductor for the power factor correction at the AC input side and at the same time for providing the charging current path for a set of switched capacitors proposed in [13]. Furthermore, the switched capacitors help to decrease the DC-link voltage more than the buck converter. In other words, this Z-source network is a high gain step-down switched network featuring an input inductor. In fact, the Z-source network applies to the front-end of a buck converter offering a high gain DC-link step-down operation with a proper power factor correction capability. All of the advantages of the proposed PFC buck rectifier are obtained through the only one power converter stage with the utilization of the switched capacitor Z-source network. In addition, for the switching stage of the PFC rectifier at the load side, the buck converter is realized as a synchronous buck rectifier with two controlled switches due to lower switching power losses. The theoretical principles of the PFC rectifier performance are analyzed and the converter advantages are all characterized through a detail investigation in the following.

B. Performance Analysis

In order to easily investigate the proposed PFC rectifier modes of operation, the simplified circuit configurations of the rectifier are shown in Fig. 2(a) and (b) during the positive half cycle of the AC input voltage. The rectifier modes of operation are all the same in both the positive and the negative half cycles of the AC input voltage. The rectifier has two modes of operation in each half cycle of the AC input voltage which are analyzed as follows.

1) Mode I [$DT_s \sim T_s$]:

This mode is shown in Fig. 2(a) in which the switch SW_1 is turned off while the anti-parallel diode of SW_2 is forward biased and thus conduct. Thus, the output inductor L_o current flows through this conducting diode. At the same time, the switch SW_2 is switched on to reduce the on state voltage drop of its anti-parallel diode. Furthermore, the input inductor L_{in} provides the charging current path of the capacitors C_1 and C_2 which are in series with the conducting diode D_3 while having the diodes D_1 and D_2 reversed biased. Also, the capacitors C_1 and C_2 are the same and equal, thus, their voltages are the same, i.e. $V_{C1} = V_{C2} = V_{C1,2}$. The peak voltage and current equations of the converter components for this mode of the operation are obtained as follows.

$$\begin{cases} \hat{V}_{Lin} = 2\hat{V}_{C1,2} - \hat{V}_{in} \\ \hat{V}_{Lo} = \hat{V}_{Co} \\ \hat{I}_{in} = \hat{I}_{Lin} = \hat{I}_{C1,2} \\ \hat{I}_{Lo} = \hat{I}_{Co} + \hat{I}_{o} \end{cases} \quad (1)$$

2) Mode II [$0 \sim DT_s$]:

In this mode, the switches SW_1 and SW_2 are turned on and off, respectively. As shown in Fig. 2(b), the diodes D_1 and D_2 are forward biased and connect the capacitors C_1 and C_2 in parallel. Then, the input inductor L_{in} and the paralleled capacitors C_1 and C_2 feed the output load and charge the output filter capacitor C_o. The peak voltage and current equations are

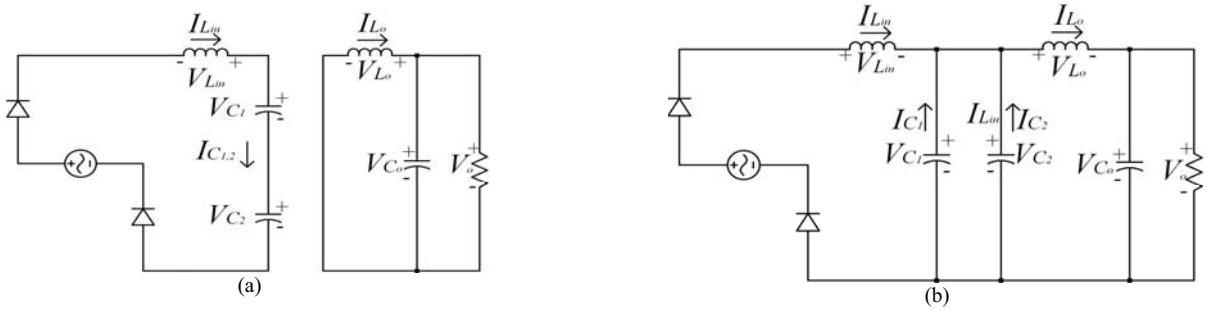

Fig. 4. Operation modes (a) I [$DT_s \sim T_s$], and (b) II [$0 \sim DT_s$] of the proposed PFC rectifier.

derived as in (2).

$$\begin{cases} \hat{V}_{Lin} = \hat{V}_{in} - \hat{V}_{C1,2} \\ \hat{V}_{Lo} = \hat{V}_{C1,2} - \hat{V}_{Co} \\ \hat{I}_{in} = \hat{I}_{Lin} \\ \hat{I}_{Lo} = \hat{I}_{Lin} + 2\hat{I}_{C1,2} \end{cases} \quad (2)$$

It should be mentioned the rectifier modes of operation in both positive and negative half cycles of the AC input voltage source are the same as mode I and II described above.

By applying volt-sec balance on the input inductor L_{in} and the output one (L_o), the capacitors C_1, C_2 and the output peak voltage equations of the proposed synchronous buck PFC rectifier is obtained as in (3).

$$\begin{cases} \hat{V}_{C1,2} = \dfrac{1}{2-D}\hat{V}_{in} \\ \hat{V}_{Co} = \hat{V}_o = \dfrac{D}{2-D}\hat{V}_{in} \end{cases} \quad (3)$$

The gain curve of the proposed rectifier is plotted in terms of the duty cycle (D), shown in Fig. 5. As obviously seen from this figure, for a same duty cycle, the proposed rectifier offers a much lower step-down gain than the conventional buck rectifier. In other words, for achieving the same step-down voltage gain, the proposed rectifier requires higher duty cycle than the conventional one. This leads to the possibility of increasing the switching frequency without the concern of the parasitic elements effect on the switching. This increase in switching frequency is desired due to the passive components reduction in size resulting in less converter volume and cost. Also, the only one stage power conversion possibility helps to achieve higher efficiency and reliability in addition to lower converter size and complexity of the circuit topology and control method.

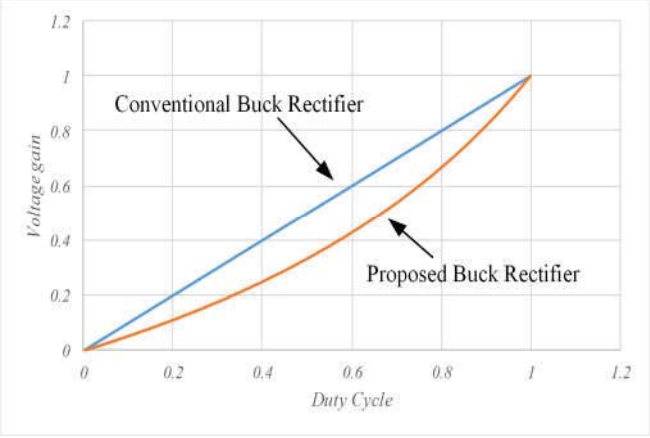

Fig. 5. Gain curve of the proposed vs. conventional PFC buck rectifier.

III. Components Desig and Stress Analysis

This section is dedicated for passive and active component design, and voltage and current stresses analysis.

A. Inductors

The inductors are designed and selected based on the desired ripple current being a constant percent of the average inductor current, i.e. $\Delta I_L = \%x I_L$. The two input and output inductors of the proposed rectifier are selected using the equations given in (4). Also, the continuous conduction mode conditions for L_{in} and L_o are given in (5).

$$\begin{cases} L_{in} = \dfrac{D(1-D)}{\%x\,(2-D)} \dfrac{\hat{V}_{in}^{\,2}}{f_s P_{out}} \\ L_o = \dfrac{D(1-D)}{\%x\,(2-D)} \dfrac{\hat{V}_{in}^{\,2}}{f_s P_{out}} \end{cases} \quad (4)$$

$$\begin{cases} L_o > \dfrac{R_o(1-D)}{2f_s} \\ L_{in} > \dfrac{R_o(2-D)(1-D)}{2Df_s\hat{V}_{in}} \end{cases} \quad (5)$$

B. Capacitors

For the capacitors selection, the %y is assumed as the percent of the capacitors voltage ripple. Thus, all of the capacitors can be designed using the following equations.

$$\begin{cases} C_o = \dfrac{(1-D)}{\%y8L_o f_s^2} \\ C_{1,2} = \dfrac{(-DE+2-D)D}{\%y2R_o f_s(2-\mathrm{D})} - \dfrac{(1-D)D}{\%y2f_s^{\,2}}\left(\dfrac{1}{L_o} - \dfrac{1}{L_{in}}\right) \end{cases} \quad (6)$$

C. Diodes and Switches

The peak voltage and current stresses of the diodes and switches of the proposed rectifier are given in the following equations.

$$\begin{cases} \hat{V}_{D1,2,3} = \dfrac{\hat{V}_{in}}{2-D} \\ \hat{V}_{SW1} = \dfrac{2\hat{V}_{in}}{2-D} \\ \hat{V}_{SW2} = \hat{V}_{D_{SW2}} = \dfrac{\hat{V}_{in}}{2-D} \end{cases} \quad (7)$$

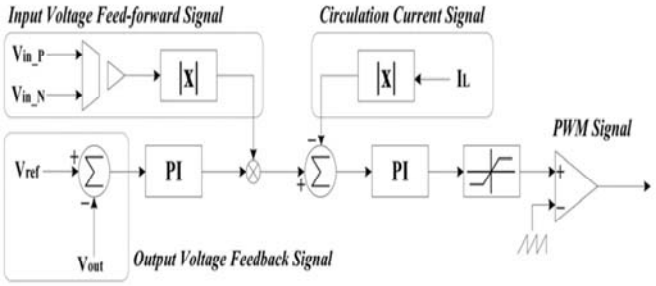

Fig. 6. Block diagram of the average current control method.

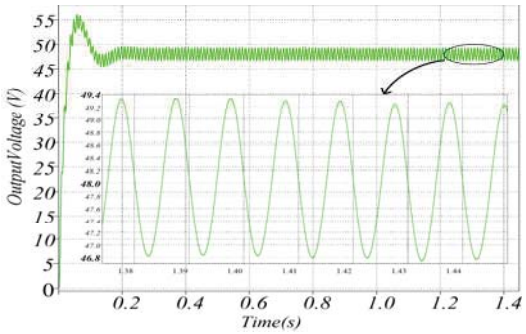

Fig. 7. Output voltage of the proposed rectifier, V_o.

$$\begin{cases} \hat{I}_{D1,2} = \dfrac{\hat{V}_{in}D(2-2D)}{2(2-\mathrm{D})^{2}} - \dfrac{\hat{V}_{in}D(1-D)T_s}{4(2-D)}\left(\dfrac{1}{L_o}-\dfrac{1}{L_{in}}\right) \\ \hat{I}_{D3} = \hat{I}_{L_{in},\max} = \dfrac{D^2\hat{V}_{in}}{R_o(2-D)^2} + \dfrac{\hat{V}_{in}D(1-D)T_s}{2(2-D)L_{in}} \\ \hat{I}_{SW1} = \hat{I}_{L_o,\max} = \dfrac{\hat{V}_{in}D}{R_o(2-D)} + \dfrac{\hat{V}_{in}D(1-D)T_s}{2(2-D)L_o} \\ \hat{I}_{D_{SW2}} = \hat{I}_{L_o,\max} = \dfrac{\hat{V}_{in}D}{R_o(2-D)} + \dfrac{\hat{V}_{in}D(1-D)T_s}{2(2-D)L_o} \end{cases} \quad (8)$$

Where, $\hat{V}_{D_{SW2}}$ and $\hat{I}_{D_{SW2}}$ are the peak voltage and current stresses of the diode of the SW_2.

IV. Control Method

The block diagram of the control method is depicted in Fig. 6. This simple and known method has already been proposed in [4] which is called Average Current Control (ACC) method. Also, the other control methods for power factor correction are proposed as in [14]-[16]. In this control method, the desired output voltage and the input current requirement are achieved by double loops of control, i.e. the outer voltage control and the inner current control loops. As it is obvious in Fig. 6, the error signal of the output voltage and its reference is compensated using a simple PI controller then, this signal is multiplied by an ideal rectified sine waveform to produce the input inductor (L_{in}) current. This current reference is then almost appeared in the input inductor current when its error signal with L_{in} current being fed to a PI controller.

TABLE I. Simulation Conditions and Parameters.

Description	Values
Rated power, P_o	500W
Input AC voltage, V_{in}	160-265Vrms
Output DC voltage, V_o	48V_{dc}
Switching frequency, f_s	50 kHz
Capacitors: C_1, C_2 and C_o	1 µF, 1 µF and 2×(6.8 mF, ESR = 19 mΩ)
Input inductor (L_{in})	3 mH, (ESR = 346 mΩ)
Output Inductor (L_o)	1 mH, (ESR = 120 mΩ)
Diodes, D_1, D_2, D_3	Powerex CS240650
IGBT switches, SW_1, SW_2	IXGH40N60C2

V. Simulation Results

In order to verify the adequacy of the proposed PFC rectifier, a set of simulations are done in this section. The simulation conditions are all given in Table I. The simulation of the proposed PFC rectifier is performed using Thermal Module of the PSIM software for considering loss related parameters. The nominal AC input voltage is assumed 230Vrms and the proposed rectifier supplies a 500W load with a regulated 48Vdc voltage.

Fig. 7 shows the output regulated 48Vdc with its ripple depicted in the center of the figure. The output voltage ripple is only 2.5V, i.e. 5.2% of 48V, which is in the acceptable range. Fig. 8 shows the AC input voltage and current of the source and the obtained input power factor (PF) is also indicated for the nominal condition. As shown in this figure, the power factor of input source is as high as 0.998 which is considerably comparable with the low input PF of conventional buck rectifier. Also, the dead zone of the input current is shorter than the conventional buck as a result of the Z-source network utilization at the front-end of the buck converter. In order to verify the high efficiency rectification of the proposed PFC rectifier, Fig. 9 is presented. The efficiency is obtained with the various output loads as low as 10% to the nominal output power. For the sake of a fair comparison, the efficiency of the proposed and the conventional rectifier reported in [17] are also plotted in the same operating conditions. The maximum efficiency is 98.5% for 10% of nominal load and minimum efficiency is 94.1% for the nominal load. As can be seen, the efficiency of the proposed PFC rectifier is higher than the

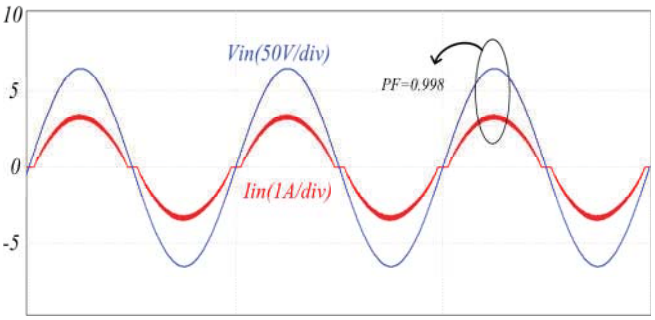

Fig. 8. Input voltage and current of the proposed rectifier.

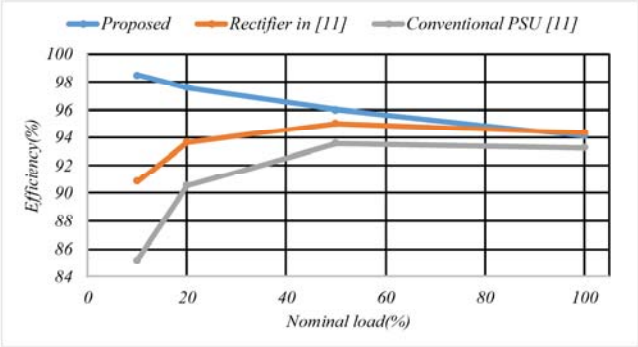

Fig. 9. The efficiency versus the percent of the nominal load.

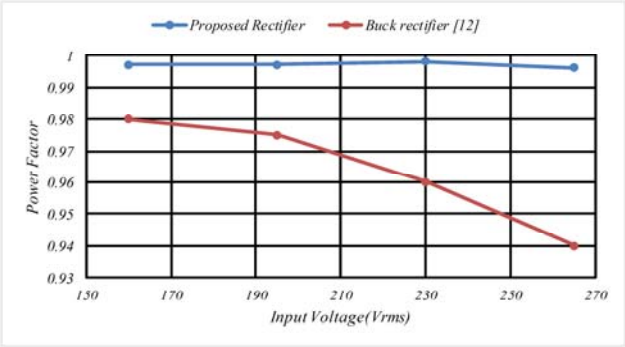

Fig. 11. The power factor (PF) versus the input voltage (V_{in}).

others, especially for low output powers which can be a remarkable feature for variable load applications. To investigate the quality parameters of the input waveforms, the total harmonic distortion (THD) of the input current and the power factor (PF) of the input source are plotted for a range of the AC input voltage and in nominal output power, shown in Figs. 10 and 11, respectively. For the validation of the low magnitude harmonic contents of the input current, the Fig. 12 is presented. According to the standard IEC61000-3-2, the proposed rectifier can be categorized as a class D rectifier. As shown in Fig. 12, the input current harmonics are significantly lower than the standard harmonics magnitude of class D rectifiers.

In order to compare the proposed PFC rectifier with the already reported rectifiers, the Table II is also presented. As can be seen from this table, the proposed PFC rectifier offers suitable input/output current/voltage characteristics which are comparable with the other rectifiers. Also, the proposed PFC rectifier requires acceptable number of components with the ability of AC/DC conversion using only one stage of the power converters. According to the analysis results, the derived theoretical operations of the proposed rectifier are all well-supported by the simulations which confirms the validity of the proposed PFC rectifier.

VI. Conclusion

This paper introduces a high gain buck synchronous PFC rectifier, which utilizes a Z-source network at the front-end of a synchronous buck converter. The input inductor of the Z-source network provides the possibility of improvement in the input current THD and power factor (PF) of the proposed rectifier. Also, the Z-source network employment allows to convert the input AC voltage to the desired and regulated output DC voltage using only one stage of the power converter. The well-known and simple control method called average current control (ACC) is applied to the synchronous buck converter to decrease control complexity and increase the efficiency of the proposed PFC rectifier.

References

[1] Liu Ping, Meng Yu, Kang Yong, Zhang Hui, and Chen Jian, "Analysis of single-phase boost power factor correction (PFC) converter," in *Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99 (Cat. No.99TH8475)*, 1999, no. July, pp. 933–937 vol.2.

[2] H. Y. Kanaan and K. Al-Haddad, "Boost Preregulators for Power Factor Correction in Single-Phase Rectifiers," *Power Electron. Renew. Energy Syst. Transp. Ind. Appl.*, pp. 503–533, 2014.

[3] Y.-S. Kim, W.-Y. Sung, and B.-K. Lee, "Comparative Performance Analysis of High Density and Efficiency PFC Topologies," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2666–2679, Jun. 2014.

[4] Onsemi, *"Power Factor Correction (Hand Book)"*, 5th ed. Onsemi, 2014.

[5] M. Mahdavi and H. Farzanehfard, "High efficiency step up/down PFC Rectifier," *Int. Conf. Appl. Electron.*, pp. 3–6, 2012.

[6] J. Yang, J. Zhang, X. Wu, Z. Qian, and M. Xu, "Performance comparison between buck and boost CRM PFC converter," in *2010*

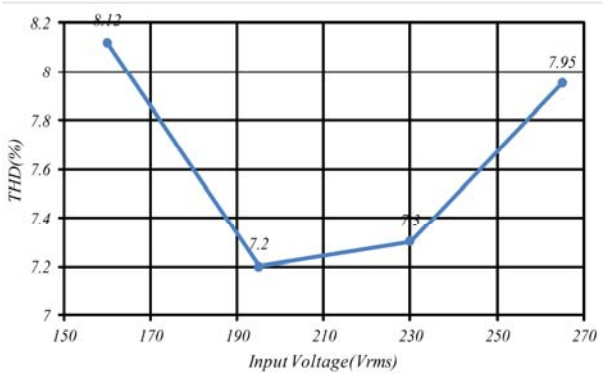

Fig. 10. The input current THD versus the input voltage (V_{in}).

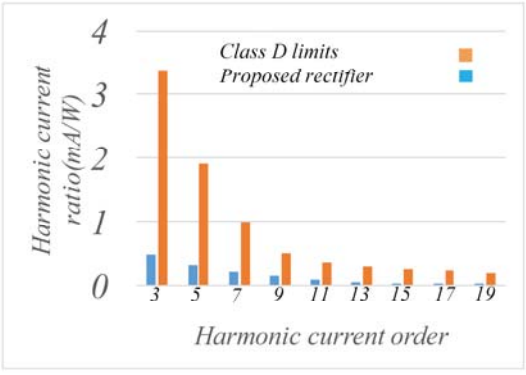

Fig. 12. The input current harmonics content.

TABLE II. COMPARISON OF THE REPORTED AND THE PROPOSED PFC RECTIFIER.

	[17]	[18]	[18]	[19]	[9]	[20]	**Proposed**
Topology	Boost +DC-DC Stage	Buck+Buck-Boost	Buck+Flyback	Bridgeless Buck-Boost	Bridgeless Buck	Bridgeless Buck-Boost	High Gain Buck
Input Voltage	180-264V_{rms}	90-265V_{rms}	90-265V_{rms}	110V_{rms}	100V_{rms}	85-264V_{rms}	160-265V_{rms}
Output Voltage	48V_{dc}	80V_{dc}	80V_{dc}	48V_{dc}	50V_{dc}	18V_{dc}	48V_{dc}
Output Power	480W	150W	150W	---	31.25W	200W	500W
Magnetic Components	3	1	1	1	3	2	2
Capacitors	4	1	1	1	2	2	3
Diode	7	6	6	2	4	2	7
Control Switch	5	2	2	2	2	4	2
Power Factor	---	0.92-0.995	0.91-0.99	0.998	0.84-0.97	0.76-0.995	0.99-0.998
Peak Efficiency	95.04%	96.2%	96%	---	---	92%	98.5%

IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL), 2010, pp. 1–5.

[7] L. Huber, L. Gang, and M. M. Jovanović, "Design-oriented analysis and performance evaluation of buck PFC front end," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 85–94, 2010.

[8] B. Keogh, G. Young, H. Wegner, and C. Gillmor, "Design considerations for high efficiency buck PFC with half-bridge regulation stage," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 1384–1391, 2010.

[9] X. Lin and F. Wang, "A Novel Bridgeless Buck PFC Converter With Half Dead Zones," pp. 602–606, 2016.

[10] S. Sharifi and M. Monfared, "Series and Tapped Switched-Coupled-Inductors Impedance Networks," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1–1, 2018.

[11] S. Sharifi, F. Jahani, and M. Monfared, "Direct single phase AC-AC converters based on novel series impedance networks," *IEEE Trans. Power Electron.*, vol. 8993, no. c, 2018.

[12] M. Monfared, H. D. Heydary, and A. Saeedi, "Techno Economic Assessment of Different Electrochemical Energy Storage Systems for Use in Khorasan , Iran," pp. 156–161, 2015.

[13] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 55, no. 2, pp. 687–696, 2008.

[14] H. Heydari-doostabad, R. Keypour, M. R. Khalghani, and M. H. Khooban, "A new approach in MPPT for photovoltaic array based on Extremum Seeking Control under uniform and non-uniform irradiances," *Sol. Energy*, vol. 94, pp. 28–36, 2013.

[15] H. Heydari-Doostabad, M. R. Khalghani, and M. H. Khooban, "A novel control system design to improve LVRT capability of fixed speed wind turbines using STATCOM in presence of voltage fault," *Int. J. Electr. Power Energy Syst.*, vol. 77, pp. 280–286, 2016.

[16] P. Sarvghadi, R. Ghazi, and H. Heydari, "A new Approach for Predictive Control System Design to Improve Power Factor and Reduce Harmonic Current Injection using D-STATCOM," *8th Annu. Int. Power Electron. Drive Syst. Technol. Conf. (PEDSTC 2017), 2017*, pp. 14–16, 2016

[17] J.-I. Baek, J.-K. Kim, J.-B. Lee, H.-S. Youn, and G.-W. Moon, "A Boost PFC Stage Utilized as Half-Bridge Converter for High-Efficiency DC–DC Stage in Power Supply Unit," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7449–7457, Oct. 2017.

[18] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A Family of Single-Phase Hybrid Step-Down PFC Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5271–5281, Jul. 2017.

[19] B. Zhao, R. Ma, A. Abramovitz, and K. Smedley, "Bridgeless buck-boost PFC rectifier with a bidirectional switch," *2016 IEEE 8th Int. Power Electron. Motion Control Conf. IPEMC-ECCE Asia 2016*, pp. 2747–2751, 2016.

[20] M. Scherbaum, M. Reddig, and M. Schlenk, "An Isolated, Bridgeless, Quasi-Resonant ZVS- Switching, Buck-Boost Single-Stage AC-DC Converter with Power Factor Correction (PFC)," pp. 74–81, 2017.