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Dynamic model development and control for multiple-output flyback converters in DCM and CCM

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Summary

Multiple-output flyback converters are widely used in switching power supplies due to their low component count and cost-effective structure. The main problem of this structure is how to balance output voltages in different load conditions. This paper proposes a new approach for single-input multiple-output flyback converters operating in DCM and CCM by a small-signal averaged model. The averaged model is derived by presenting the piecewise-linear waveform for the inductor currents inside the converter. In DCM, the magnetizing current and currents through the output windings reach zero when the switch is turned off. In CCM, the magnetizing current of the converter is continuous over a switching interval and this possibility exists that only some of the output diodes completely conduct when the switch is off. The proposed model of the converter can be used in a wide range of operations within identical and non-identical loading conditions. Using a laboratory prototype, several case studies and input-to-output transfer functions are considered to verify the proposed model. The controller design is performed for the both CCM and DCM, and then dynamic characteristics of the overall system are evaluated.

KEYWORDS

multiple-output DC-DC converter, flyback converter, averaged model, small-signal model, discontinuous conduction mode (DCM), continuous conduction mode (CCM)

1 | INTRODUCTION

Some of the design requirements dictate that the switching power supplies to provide isolated and regulated voltages to be applied to various loads. Several techniques are applied to regulate output voltages of multiple-output converters such as a multiple-output flyback converter.[1-9] Successful implementation of these techniques requires a perfect model of the converter which can be used in various operating modes and loading conditions. In this regard, in this paper, the focus is on presenting a suitable model for the converter to derive the dynamic characteristics and then design the controller and check the stability once the loop is closed by any regulation technique.

Averaged modeling of DC-DC converters is necessary for small-signal analysis and large-signal, time-domain transient studies. Up to one third of the switching frequency, the small-signal responses of a switched-mode power converter may be accurately predicted, using proper averaged models.[10] In 1 approach, the operation of a power

converter can be described by averaged equations achieved based on zero-order averaging directly state variable waveforms (state-space averaging)[10-15] or averaging switching network.[15-17] The resulted average model does not include any switching events such as switching ripples and causes smoothly varying signals. The analytical approach of the averaging method initially depends on operating modes, continuous, and discontinuous condition mode (CCM and DCM). In this way, approximations involved in behavioral models and then derived equivalent circuits have a major role in dynamic model order.[11,12] Analytical models are generally based on presenting a piecewise-linear format of the inductor current waveforms due to neglecting conduction losses.[10,18] Considering conduction losses or other parasitic elements can improve the accuracy of the dynamic model but may slightly cause nonlinearity of the current and voltage waveforms and complicates the modeling process.[14] These challenges will intensify when we face a converter with numerous operating modes, such as multiple-output flyback converter. Among the parasitic elements, the leakage inductances have a major role in operation of a multiple-output flyback converter.[1] It is necessary to predict the possible operating range for different loading conditions and also the cross coupling and cross-regulation factors (a significant challenge in the design of multiple-output flyback converters) among the outputs. They complicate model formulation and lead to increase dynamic order in conventional modeling techniques. Previous publications don't work well for this case.[2,8,16]

Based on the analytical analysis, large-signal averaged model and then the small-signal model are derived in different operating modes. The small-signal model and then ac equivalent circuit model can be constructed by applying a suitable linearization approach on averaged equations.[19-21] This model is proper to extract the input-to-output transfer functions and other frequency-dependent properties.

This paper proposes an averaged model based on presenting the piecewise-linear waveforms of the inductances inside a multiple-output flyback converter. The proposed methodology considers the transformer leakage inductances without increasing the dynamic order. This modeling can accurately predict the possible operating range for different loading conditions. In fact, the waveforms of output currents in the converter are strongly influenced by the transformer leakage inductances. The model is presented for both discontinuous and continuous magnetizing current mode. In DCM, the currents of the output windings become zero before beginning of the next switching cycle. In CCM, this may not be set for all secondary leakage inductances. In other words, some of them can reach zero before the beginning of the next switching cycle. In previously published works, such as Lee et al,[2] Naresh et al,[8] and Barrado et al,[16] the presented models can be used in CCM in which the currents in all secondary windings are continuous until the next switching cycle begins. But, this paper considers a wide range of converter operations in CCM, in which all of output diodes are not required to conduct completely when the switch is off. This is accounted to develop model of multiple-output converter with non-identical loading in its outputs. In the closed-loop concept, this paper considers the weighted feedback method to regulate output voltages in different loading conditions based on the proposed model. However, the presented methodology can be used in other regulation techniques. To verify the proposed model, a laboratory-scale prototype with 3-output flyback converter is implemented. Using the proposed model, the controller design is performed for both CCM and DCM operations, and then dynamic characteristics of the overall system are evaluated.

In short, the contributions of this paper are mentioned as follows:

- This paper proposes an averaged model based on presenting the piecewise-linear waveform for the currents of the inductances inside a multiple-output flyback converter.
- The proposed methodology considers the transformer leakage inductances which have an important role in operation of the converter, without increasing the dynamic order.
- The proposed model can be used in DCM, CCM, and transition between DCM and CCM.
- Using the proposed model, the controller design is performed for both CCM and DCM operations, and then dynamic characteristics of the overall system are evaluated.
- The proposed model has been validated with a laboratory-scale prototype and a detailed simulation.

This paper is organized as follow; Section 2 presents an analytical model of the converter and its operational principle in DCM and CCM. Based on this analysis, the averaged and linearized model is presented in Section 3. The dynamic characteristics and voltage loop controller design are performed in Section 4. In Section 5, using a laboratory-scale prototype, the dynamic performances of the converter are investigated to show the good agreement of the proposed model.

2 | ANALYTICAL MODEL AND OPERATIONAL PRINCIPLE OF FLYBACK CONVERTER

A multiple-output flyback converter provides an isolation between input and outputs. The converter periodically stores energy from dc source in the transformer magnetizing inductance when its switch is on and then transfers energy to the load when its switch is off. A schematic of a typical multiple-output flyback converter with a RC clamp is shown in Figure 1. In previous publications, various circuit models are presented for the converter transformer.[22] Here, T-model is utilized containing 1 leakage inductance per winding. This model is well-suited for averaged modeling because there is only 1 magnetizing (shunt) inductance for coupling between windings, and because each parameter of transformer can be directly measured. Therefore, the converter transformer is modeled with a magnetizing inductance, L_m, a primary leakage inductance, L_{kp}, corresponding to primary winding and secondary leakage inductances, L_{ks_1}, L_{ks_2}, and L_{ks_3}, for secondary windings 1 to 3, respectively. The clamping circuit is used in order to dissipate the energy of the primary leakage inductance, L_{kp}, and also some part of magnetizing inductance energy before current transfer to the output windings in order to limit the voltage spike on the switch, when the switch is turned off. In order to simplify the analysis, resistance of windings is neglected.

For beginning the analysis, the following assumptions are considered: (1) MOSFET, Q, is an ideal switch with anti-parallel diode and without parasitic parameters. (2) The diodes D_{o_1}, D_{o_2}, and D_{o_3} are identical without parasitic parameters. (3) The output capacitors are identical with very low ESR. (4) The loads are arbitrarily arranged such that $R_1 > R_2 > R_3$. This arrangement provides the regular analysis of the converter operation. (5) The voltage across the RC clamp is constant and then C_s is treated as a constant voltage source at the switching frequency scale. In the following, the given topology is analytically analyzed for both DCM and CCM operations.

2.1 | DCM

The sequential operating modes of the converter are depicted in Figure 2. Magnetizing inductor voltage and current waveforms for the converter are shown in Figure 3A. According to assumptions, without loss of generality, it is assumed that the magnetizing inductance current reaches zero in the fourth discharging subinterval. In this case, the switching interval is divided into 6 modes corresponding to topological switching functions, d, d_0, d_1 to d_0, d_2 to d_1, d_3 to d_2, and $(1 - d_1\text{-}d_3)$ which will be examined individually. dT_s is the on-time interval of the flyback switch, d_0T_s is the conduction interval of the clamp diode, and d_1T_s, d_2T_s, and d_3T_s are the conduction interval of the output diodes D_{o_1}, D_{o_2}, and D_{o_3}, respectively.

Mode 1. $0 \le t \le t_0$

The switch, Q, is turned on during $[0, t_0 = dT_s]$ and the input voltage, v_g, is applied to the primary side of transformer. The magnetizing current, i_{lm}, will increase from zero with a slope of $v_g/(L_m + L_{kp})$ to reach its peak, i_{p_0}, at t_0.

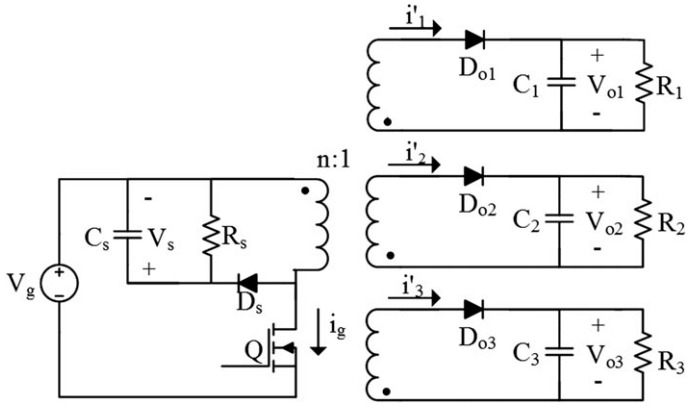

FIGURE 1 A typical single-input multiple-output flyback converter

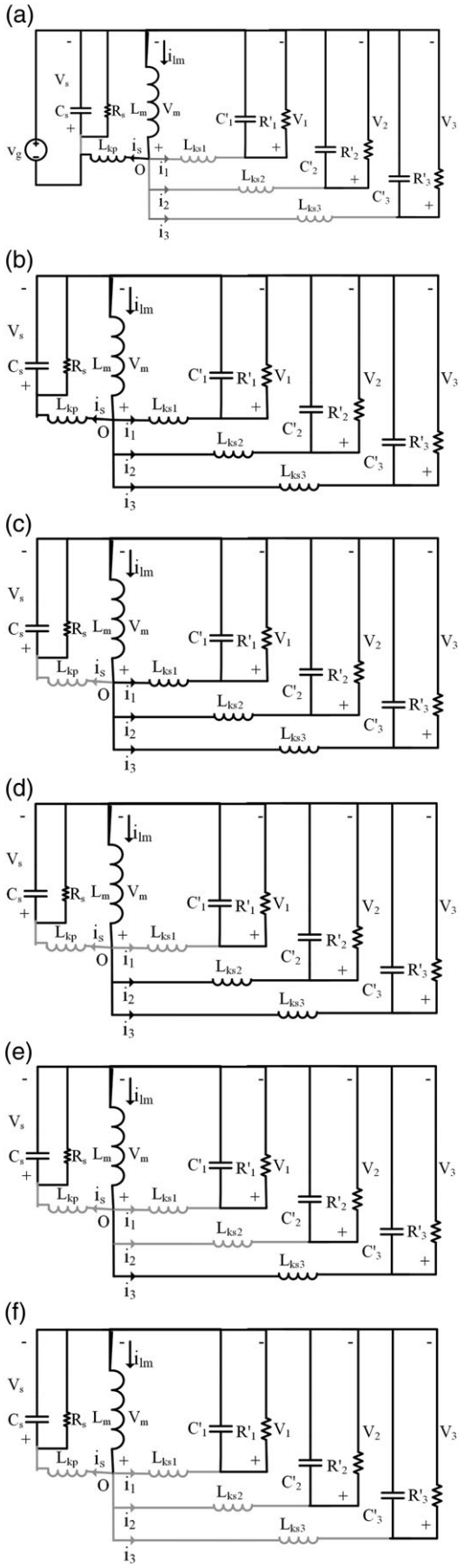

FIGURE 2 Equivalent circuits of the converter in sequential operating modes. (A) Mode 1: [0, t_0] (B) mode 2: [t_0, t_1] (C) mode 3: [t_1, t_2] (D) mode 4: [t_2, t_3] (E) mode 5: [t_3, t_4] (F) mode 6: [t_4, T_s]

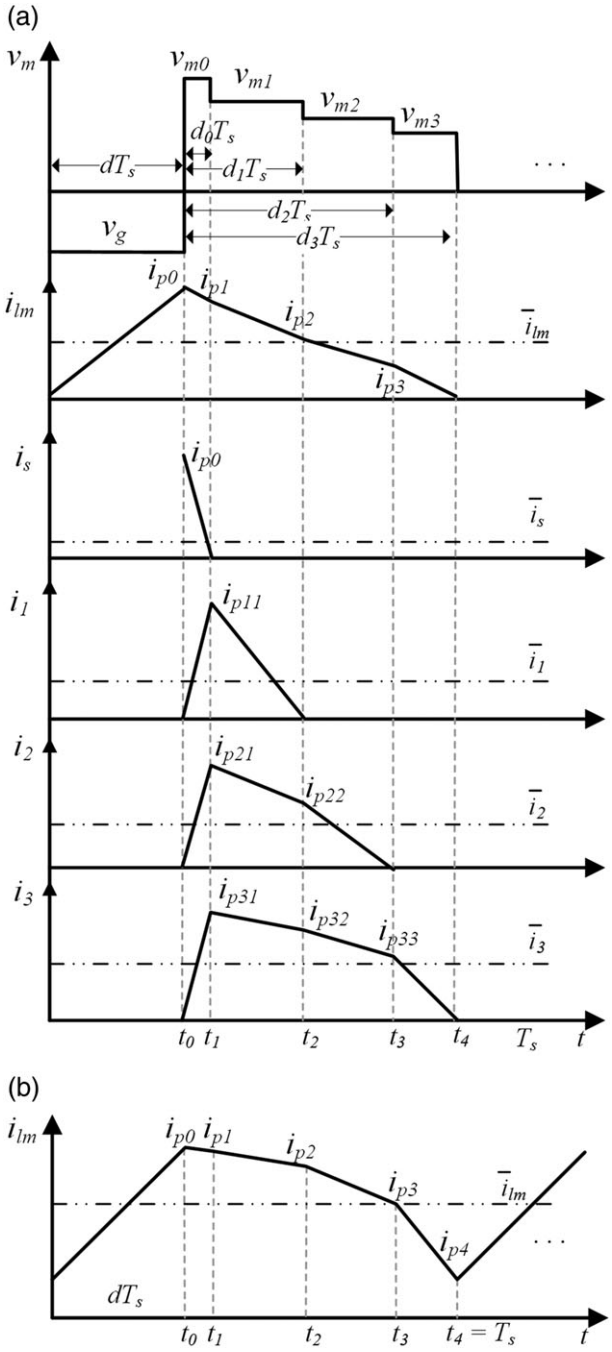

FIGURE 3 Piecewise-linear representation of voltage and current waveforms during 1 switching cycle in (A) DCM, (B) CCM.

$$i_{p_0} = \frac{v_g}{L_m + L_{kp}} \cdot t_0, t_0 = dT_s \tag{1}$$

where, v_g is input dc voltage, T_s is switching period, and d is duty cycle of the switch.

Mode 2. $t_0 \le t \le t_1$

During $[t_0, t_1]$, the switch is turned off, and a large portion of the magnetizing current will flow in the capacitor of RC clamp circuit due to the primary and secondary leakage inductances. Figure 2B shows the equivalent circuit of the converter in Mode 2 of operation. The secondary sides are transferred to the primary side of the transformer. The

capacitance of C_s, C_1, C_2, and C_3 are assumed to be large enough so that the voltage across them can be considered constant during the entire switching cycle. In this mode, the output currents through the leakage inductances, L_{ks_j} for $j = 1,2,3$ increase and the magnetizing current, i_{lm}, decreases. By implementing Kirchhoff's circuit law in node O is obtained by

$$i_{lm} = i_s + i_1 + i_2 + i_3. \tag{2}$$

Differentiating Equation 2 yields to Equation 3 and substitution of the current charging rates of inductor currents and capacitor current of clamp circuit into Equation 3 gives Equation 4.

$$\frac{di_{lm}}{dt} = \frac{di_s}{dt} + \frac{di_1}{dt} + \frac{di_2}{dt} + \frac{di_3}{dt} \tag{3}$$

$$-\frac{v_{m_0}}{L_m} = \frac{v_{m_0} - V_s}{L_{kp}} + \frac{v_{m_0} - v_1}{L_{ks_1}} + \frac{v_{m_0} - v_2}{L_{ks_2}} + \frac{v_{m_0} - v_3}{L_{ks_3}} \tag{4}$$

$$v_j = n.v_{o_j}, j = 1, 2, 3$$

n is turn ratio of transformer, and v_1, v_2, v_3 are output side voltages transferred to the primary side. Voltage across RC clamp is V_s which is assumed to have a fixed value associated with operating point of converter. The voltage across magnetizing inductance, v_{m_0}, in this subinterval can be found as follows:

$$v_{m_0} = \frac{V_s/L_{kp} + \sum_{j=1}^{3} v_j/L_{ks_j}}{1/L_m + 1/L_{kp} + \sum_{j=1}^{3} 1/L_{ks_j}}. \tag{5}$$

In this subinterval, the clamp diode, D_s, conducts. The current following into C_s can be expressed as

$$i_s(t) = \frac{v_{m_0} - V_s}{L_{kp}} . (t - t_0) + i_{p_0}, t_0 \le t \le t_1. \tag{6}$$

The duty cycle of the clamp diode, d_0, is calculated by considering $i_s(t) = 0$ and substituting i_{p_0} from Equation 1.

$$d_0 = \frac{L_{kp} \quad v_g d}{L_m + L_{kp}(V_s - v_{m_0})} \tag{7}$$

At the end of t_1 when $i_s(t)$ reaches zero, D_s is reverse biased, and the currents through the output windings rise to

$$i_{p_{j1}} = \frac{v_{m_0} - v_j}{L_{ks_j}} . (d_0 T_s), j = 1, 2, 3. \tag{8}$$

Mode 3. $t_1 \le t \le t_2$

According to the equivalent circuit in this mode that is shown in Figure 2C, by implementing Kirchhoff's circuit law in node O, voltage across the magnetizing inductance, L_m, can be calculated by

$$v_{m_1} = \frac{\sum_{j=1}^{3} v_j/L_{ks_j}}{1/L_m + \sum_{j=1}^{3} 1/L_{ks_j}}. \tag{9}$$

The current associated with lighter load will reach zero before others due to its higher voltage. Therefore, in this mode, the first output current, i_1 drops to zero, and the diode, D_{o_1}, is reversely biased up to the next switching cycle. The rest of conduction interval and then duty cycle of D_{o_1}, d_1, can be obtained by equating $i_1(t) = 0$ and substituting

$i_{p_{11}}$ from Equation 8.

$$i_1(t) = \frac{v_{m_1} - v_1}{L_{ks_1}}.(t - t_1) + i_{p_{11}}, t_1 \le t \le t_2 \tag{10}$$

$$d_1 = \frac{v_{m_0} - v_{m_1}}{v_1 - v_{m_1}} d_0 \tag{11}$$

At the end of this mode, the currents of other outputs can be derived by

$$i_{p_{j2}} = \frac{v_{m_1} - v_j}{L_{ks_j}}.(d_1 - d_0)T_s + i_{p_{j1}}, j = 2, 3. \tag{12}$$

Mode 4. $t_2 \le t \le t_3$

According to Figure 2D, during this mode, the magnetizing current is transferred to the second and third outputs. In similar way, the voltage across the magnetizing inductance, L_m, can be obtained by

$$v_{m_2} = \frac{\sum_{j=2}^{3} v_j / L_{ks_j}}{1/L_m + \sum_{j=2}^{3} 1/L_{ks_j}}. \tag{13}$$

In this mode, the second output current drops to zero, and the conduction interval of D_{o_2} is determined according to the time that i_2 reaches zero.

$$i_2(t) = \frac{v_{m_2} - v_2}{L_{ks_2}}.(t - t_2) + i_{p_{22}}, t_2 \le t \le t_3 \tag{14}$$

$$d_2 = \frac{(v_{m_1} - v_{m_2})d_1 + (v_{m_0} - v_{m_1})d_0}{v_2 - v_{m_2}} \tag{15}$$

where, d_2 is the duty cycle of D_{o_2}. At the end of Mode 4, the current of the third output can be found by

$$i_{p_{33}} = \frac{v_{m_2} - v_3}{L_{ks_3}}.(d_2 - d_1)T_s + i_{p_{32}}, j = 2, 3. \tag{16}$$

Mode 5. $t_3 \le t \le t_4$

According to Figure 2E, in this mode, the output diodes D_{o_1} and D_{o_2} are reverse biased and i_3 reaches zero at $(d + d_3)$ T_s. During this mode, only L_m and L_{ks_3} are conducting current. The voltage across the magnetizing inductance and duty cycle of D_{o_3} can be expressed as

$$v_{m_3} = \frac{L_m v_3}{L_m + L_{ks_3}} \tag{17}$$

$$i_3(t) = -\frac{v_3}{L_m + L_{ks_3}}.(t - t_3) + i_{p_{33}}, t_3 \le t \le t_4 \tag{18}$$

$$d_3 = d_2 + \frac{L_m + L_{ks_3}}{L_{ks_3} v_3}.\{v_{m_2}(d_2 - d_1) + v_{m_1}(d_1 - d_0) + v_{m_0} d_0 - v_3 d_2\} \tag{19}$$

Mode 6. $t_4 \le t \le T_s$.

According to Figure 2F, during this mode, the magnetizing inductance voltage and current are zero. In this mode, the switching function is expressed by (1- d_1 – d_3).

According to Figure 3A, v_{m0}, v_{m1}, v_{m2}, and v_{m3} reduce the magnetizing current, i_{lm}, piecewise-linear to i_{p1}, i_{p2}, i_{p3} and zero in the subsequence discharging subintervals, d_0T_s, d_1T_s, d_2T_s, and d_3T_s, respectively. i_{p1}, i_{p2}, and i_{p3} can be easily found by summing the peak values of the output currents obtained by Equations 8, 12, and 16 in the corresponding operating modes.

2.2 | CCM

In CCM, the magnetizing current is continuous over a switching interval, and it is possible that the current through some of the secondary windings reach zero before the start of the next switching cycle. Without loss of generality, it is assumed that duty cycles of the first and second output diodes are always less than $1 - d$, and duty cycle of third output diode is equal to $1 - d$. Figure 3B illustrates derived magnetizing current in this condition. The other waveforms are similar to that shown in Figure 3A with the difference that the third output current does not reach zero before T_s in the last discharging subinterval. In this case, the switching interval is divided into 5 modes corresponding to topological switching functions, Mode 1 ($0 \le t \le dT_s$), Mode 2 ($(dT_s \le t \le (d + d_0)T_s$), Mode 3 ($(d + d_0)T_s \le t \le (d + d_1)T_s$), Mode 4 ($(d + d_1)\ T_s \le t \le (d + d_2)T_s$), and Mode 5 ($(d + d_2)\ T_s \le t \le T_s$). In these modes, the analytic analysis is done same as previous section for Mode 1, Mode 2, Mode 3, Mode 4, and Mode 5 of DCM operation, respectively.

In Mode 1, the switch, Q, is turned on during [0, t_0] and the input voltage, v_g, is applied to the primary side of transformer. The magnetizing current, i_{lm}, will increase from a non-zero minimum current with a slope of $v_g/(L_m + L_{kp})$ to reach its peak, i_{p0}, at t_0 which can be obtained as follows,

$$i_{p0} = \bar{i}_{lm} + \frac{v_g}{2\left(L_m + L_{kp}\right)} dT_s \tag{20}$$

where $\bar{i}_{lm}$ is average value of magnetizing current over a switching cycle. In the next modes, Mode 2, Mode 3, Mode 4, and Mode 5, the analysis is done similar to the corresponding modes of DCM operation. In Mode 5, the switching function, d_3, is $1 - d$.

In general loading conditions, duty cycle of the output diodes can be determined by

$$d_j = \min\left\{\frac{i_{p_{jj}} L_{ks_j}}{T_s\left(v_j - v_{m_j}\right)} + d_{j-1}, 1-d\right\}, j = 1, 2, 3 \tag{21}$$

where, $i_{p_{jj}}$ must be substituted by Equations 8, 12, and 16. v_{m_j} is calculated by Equations 9, 13, and 17, and the duty cycle of clamp diode, d_0, is obtained by Equation 7.

The possible operating ranges can be defined based on the loads at the outputs with the variations in duty cycle of converter switch. Equation 21 is formulated for both DCM and CCM and can automatically determine the operating mode of the averaged model. In this way, if the left term is chosen, it will indicate discontinuity in j*th* output, and if this result is chosen for all outputs, operating in DCM will be detected. Otherwise, if the right term is selected for j*th* output, operating in CCM will be confirmed. The presented approach provides an algorithmic process for analytical modeling in DCM, CCM, and transition between DCM and CCM which can be used in different loading conditions. In other words, the model can cover a wide range of non-identical loading in converter outputs.

3 | AVERAGED AND LINEARIZED DYNAMIC MODEL

An averaged model implies the disappearance of any switching events (hence discontinuities) to the benefit of a smoothly varying and continuous signal. The switching ripple in the inductor current and capacitor voltage waveforms can be removed by averaging over 1 switching period. It is notable, that average values are allowed to vary from 1 switching period to the next. Thanks to this approach, the behavior of a power converter can be described by averaged equations. Once linearized across an operating point, these equations will lead to the so-called averaged small-signal model, useful to illustrate the dynamic response of the converter and then design controller and check the stability once the loop is closed.

3.1 | Averaged model

State variables are usually associated with storage elements such as capacitors and inductors with different order of rates in a certain time interval for example, 1 switching cycle. The dynamics of some variables such as inductor current become fast especially in DCM so they can be neglected at low frequencies. It is a fundamental assumption in order to present the reduced-order models. The model can be derived in more streamline solution when the assumption is explicitly made beforehand. In the previous section, some implicit assumptions applicable in proposed averaged model are used. A general averaging method, first introduced in the converter averaging concept in Sun et al,[23] can be rewritten here. The method consists of 5 steps, specified as follows:

1. Consider slow variable v_{o_1}, v_{o_2}, and v_{o_3} as constant over a switching cycle;
2. Calculate the current of leakage inductances, i_1, i_2, and i_3 as very fast variables. These can be easily formulated by Figure 3 for DCM and CCM.
3. Substitute the very fast variables resulting from step 2) in the state equations of slow variables.

$$\frac{\partial v_{o_j}}{\partial t} = \begin{cases} -\dfrac{v_{o_j}}{C_j R_j} & 0 \le t \le dT_s \\ \dfrac{n i_j}{C_j} - \dfrac{v_{o_j}}{C_j R_j} & dT_s \le t \le (d+d_j)T_s \\ -\dfrac{v_{o_j}}{C_j R_j} & (d+d_j)T_s \le t \le T_s \end{cases} \quad j = 1,2,3 \tag{22}$$

4. Averaging the right-hand side of the above slow variable models over a switching cycle gives the averaged function.

$$\frac{\partial \overline{v}_{o_j}}{\partial t} = f_{j+1}\left(\overline{i}_{lm}, \overline{v}_o, d, \overline{v}_g\right) = \frac{n\overline{i}_j}{C_j} - \frac{\overline{v}_{o_j}}{C_j R_j} j = 1,2,3 \tag{23}$$

where $\overline{i}_j$ is as average value of leakage inductance current which should be substituted for Equation 23 and vectors, $\overline{v}_o$ are defined as

$$\overline{v}_o = \{\overline{v}_{o_1}, \overline{v}_{o_2}, \overline{v}_{o_3}\} \tag{24}$$

$$\overline{i}_j = \frac{1}{T_s} \int_{dT_s}^{(d+d_j)T_s} i_j(t)dt = \frac{i_{p_{j1}}}{2} \cdot d_0 + \sum_{k=1}^{j} \frac{\left(i_{p_{jk}} + i_{p_{j(k+1)}}\right)}{2} \cdot (d_k - d_{k-1}) \quad j = 1,2,3. \tag{25}$$

It should be noted that Equation 25 is generally written for the both DCM and CCM operations with different loading. So, if a parameter appeared in it that is not defined in Figure 3, it must be substituted by zero. For example, for $j = 1$, the current waveform of output 1, i_1, does not have $i_{p_{12}}$ in DCM operation so in calculating $\overline{i}_1$, it will be substituted by zero in Equation 25.

5. The net change in magnetizing inductance current, i_{lm} as a variable faster than output voltage can be correctly predicted by use of the average voltage across it over a switching cycle.

$$L_m \frac{\partial \overline{i}_{lm}}{\partial t} = f_1\left(\overline{i}_{lm}, \overline{v}_o, \mathrm{d}, \overline{v}_g\right) = d\overline{v}_g - d_0\overline{v}_{m_0} - (d_1 - d_0)\overline{v}_{m_1} - (d_2 - d_1)\overline{v}_{m_2} - (d_3 - d_2)\overline{v}_{m_3} \tag{26}$$

where $\overline{v}_{m_0}, \overline{v}_{m_1}, \overline{v}_{m_2}$, and $\overline{v}_{m_3}$ are average values of voltage across L_m imposed by the reflected output voltages in sequential subintervals when the switch is off. This is a result of taking non-identical loading in outputs which leads to periodically change of i_{lm} in sequential subintervals within the switching cycle.

Therefore, the state variables will be the average value of capacitor voltage, $\overline{\mathrm{v}}_{o_1}$, $\overline{\mathrm{v}}_{o_2}$, and $\overline{\mathrm{v}}_{o_3}$, and the average value of magnetizing current, $\bar{i}_{lm}$. In order to determine the state space averaged description, state vector, $\overline{x}(t)$, the input vector, $\overline{u}(t)$, and output vector, $\overline{y}(t)$, are defined as follows,

$$\begin{aligned}\dot{\overline{x}}(t) &= f(\overline{x}(t), \mathrm{d}(t), \overline{u}(t))\\ \overline{y}(t) &= g(\overline{x}(t), \mathrm{d}(t), \overline{u}(t))\end{aligned} \tag{27}$$

$$\boldsymbol{x}(\boldsymbol{t}) = \begin{bmatrix} \bar{i}_{lm} \\ \overline{\mathrm{v}}_{o_1} \\ \overline{\mathrm{v}}_{o_2} \\ \overline{\mathrm{v}}_{o_3} \end{bmatrix}, \mathrm{u}(\boldsymbol{t}) = \left[\overline{\mathrm{v}}_g\right], \boldsymbol{y}(\boldsymbol{t}) = \left[\bar{i}_g\right]$$

where, the input vector, $\overline{u}(t)$, contains input voltage, $\overline{v}_g$. Duty cycle of the flyback switch is denoted by d. Here, output vector $\overline{y}(t)$ includes the input current, $\bar{i}_g$, to construct the small-signal equivalent circuit.

$$\bar{i}_g = g\left(\bar{i}_{lm}, \overline{\mathrm{v}}_o, \mathrm{d}, \overline{\mathrm{v}}_g\right) = \begin{cases} \dfrac{\overline{v}_g d^2 T_s}{2\left(L_m + L_{kp}\right)}, & DCM \\ d\bar{i}_{lm}, & CCM \end{cases} \tag{28}$$

3.2 | Small signal modeling

The averaged model described in the previous section is nonlinear, because the equations involve the multiplication of low-frequency variables. Most of frequency domain techniques of time-varying circuit are not applicable for the nonlinear systems. In this case, the equations are linearized around the quiescent operating point, $P\,(I_{lm}, V_o, D, V_g)$ to construct a small-signal model. In 1 approach, small-signal model can be provided by using Taylor expansion on equations of Equation 27 around P. Notably, the quiescent point of the converter, with applying converter parameters summarized in Appendix and input variables, V_g and D, can be determined by letting the right-hand sides of differential equations derived from Equations 23 and 26, equal to zero and solving the derived algebraic equations for $(\bar{i}_{lm}, \overline{v}_{o_1}, \overline{v}_{o_2}, \overline{v}_{o_3})$. In the linearization step, the higher-order nonlinear terms generated by Taylor expansion are neglected. For simplicity of notation, these equations can be rewritten in the following form.

$$L_m \frac{\partial \hat{i}_{lm}}{\partial t} = r_m \hat{i}_{lm} + \sum_{k=1}^{3} g_{v_k} \hat{v}_{o_k} + g_{vd} \hat{d} + g_{v_g} \hat{v}_g \tag{29}$$

$$\begin{aligned} &C_j \frac{\partial \hat{v}_{o_j}}{\partial t} + \frac{\hat{v}_{o_j}}{R_j} = g_{i_j m} \hat{i}_{lm} + \sum_{k=1}^{3} \frac{1}{r_{jk}} \hat{v}_{o_k} + g_{i_j d} \hat{d} + g_{i_j v_g} \hat{v}_g \\ &j = 1, 2, 3 \end{aligned} \tag{30}$$

$$\hat{i}_g = \begin{cases} \dfrac{1}{r_g} \hat{v}_g + g_{i_g d} \hat{d}, & DCM \\ D\hat{i}_{lm} + I_{lm} \hat{d}, & CCM \end{cases} \tag{31}$$

where, the terms are defined as follows:

$$\left.\frac{\partial f_1\left(\bar{i}_{lm}, V_o, \mathrm{D}, \mathrm{V_g}\right)}{\partial \bar{i}_{lm}}\right|_{\bar{i}_{lm}=I_{lm}} = \begin{cases} 0, & DCM \\ r_m, & CCM \end{cases}$$
$$\left.\frac{\partial f_1\left(I_{lm}, V_o, \mathrm{d}, \mathrm{V_g}\right)}{\partial d}\right|_{d=D} = g_{vd}$$
$$\left.\frac{\partial f_1\left(I_{lm}, V_o, D, \overline{\mathrm{v}}_g\right)}{\partial \overline{\mathrm{v}}_g}\right|_{\overline{\mathrm{v}}_g=V_g} = g_{v_g} \tag{32}$$
$$\left.\frac{\partial f_1\left(I_{lm}, \overline{\mathrm{v}}_{o_k}, V'_{o_k}, \mathrm{D}, \mathrm{V_g}\right)}{\partial \overline{\mathrm{v}}_{o_k}}\right|_{\overline{\mathrm{v}}_{o_k}=V_{o_k}} = g_{v_k}, k = 1, 2, 3$$

$$\frac{D^2 T_s}{2\left(L_m + L_{kp}\right)} = \frac{1}{r_g}$$
$$V_g D T_s / \left(L_m + L_{kp}\right) = g_{i_g d} \tag{33}$$

$$\frac{n\partial \bar{i}_j\left(\bar{i}_{lm}, V_o, \mathrm{D}, \mathrm{V_g}\right)}{\partial \bar{i}_{lm}} = \begin{cases} 0, & DCM \\ g_{ijm}, & CCM \end{cases}, j = 1, 2, 3$$
$$\left.\frac{n\partial \bar{i}_j\left(I_{lm}, \overline{\mathrm{v}}_{o_k}, V'_{o_k}, \mathrm{D}, \mathrm{V_g}\right)}{\partial \overline{\mathrm{v}}_{o_k}}\right|_{\overline{\mathrm{v}}_{o_k}=V_{o_k}} = \frac{1}{r_{jk}}, \begin{matrix} k = 1, 2, 3 \\ j = 1, 2, 3 \end{matrix} \tag{34}$$
$$\left.\frac{n\partial \bar{i}_j\left(I_{lm}, V_o, \mathrm{d}, \mathrm{V_g}\right)}{\partial d}\right|_{d=D} = g_{i_j d}, j = 1, 2, 3$$
$$\left.\frac{n\partial \bar{i}_j\left(I_{lm}, V_o, \mathrm{D}, \overline{\mathrm{v}}_g\right)}{\partial \overline{\mathrm{v}}_g}\right|_{\overline{\mathrm{v}}_g=V_g} = g_{ijvg}, j = 1, 2, 3$$

In this case, V'_{o_k} is a set of output voltages without V_{o_k} in accordance with k*th* output. Notably, above equivalent terms have different values in DCM and CCM.

Using each of derived differential and algebraic equations, the small-signal equivalent circuit can be constructed to investigate comprehensively the dynamic behavior of the converter. As it is shown in Figure 4, this circuit is including 5 sub-circuits associated with each of small-signal equations. Figure 4A corresponds to algebraic equation in Equation 31. The differential equations in Equations 29 and 30 connected to $\hat{i}_{lm}, \hat{v}_{o_1}, \hat{v}_{o_2}$, and $\hat{v}_{o_3}$ correspond to the sub-circuits depicted in Figure 4B to E. This circuit covers the converter operation for the both CCM and DCM. In CCM, r_g is replaced with open circuit and $g_{i_g d}$ sets at zero. In DCM, $r_m \hat{i}_{lm}$ is replaced with short circuit and independent current sources, $g_{i_j m}\hat{i}_{lm}$ set at zero. Using this circuit, the small-signal transfer functions from any input-to-any output and other frequency-

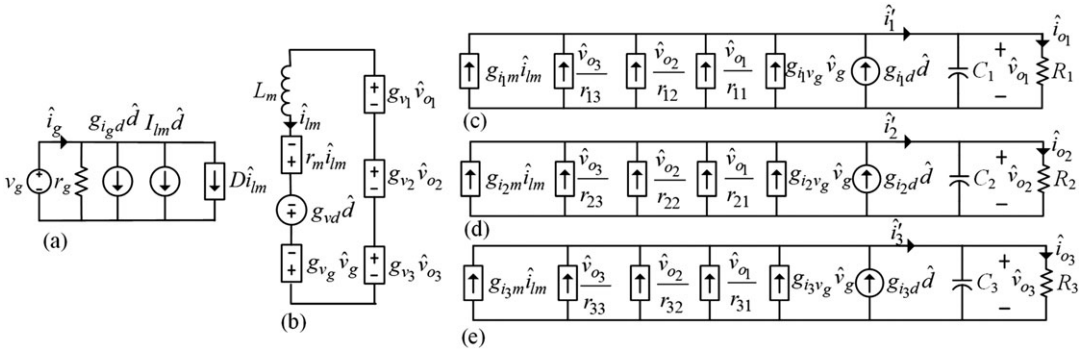

FIGURE 4 Small-signal equivalent circuit of the converter

dependent properties can be extracted. In Figure 4, the independent terms, such as $\hat{v}_g$ and $I_{lm}\hat{d}$, are shown as independent voltage and current sources. The dependent terms such as $D\hat{i}_{lm}$ and $g_{v_g}\hat{v}_g$, are also shown as dependent sources.

3.3 | Input-to-output transfer functions

Figure 5 illustrates the dynamic interactions between small-signal input and output variables of the multiple output flyback for analyzing the weighted voltage-mode regulation. There are 3 types of transfer functions of interest. In this case, input voltage-to-output voltages ($H_{\hat{v}_{o_j}/\hat{v}_g}$) are considered to analyze the line regulation performance. Input duty cycle-to-output voltages ($H_{\hat{v}_{o_j}/\hat{d}}$) are seen to design the closed-loop system. The load regulation performance is investigated by self-output impedances and cross-output impedances $\left(Z_{\hat{v}_{o_j}/\hat{i}_{o_k}}\right)$. These functions can be found by the small-signal equivalent circuit depicted in Figure 4.

$$H_{\hat{v}_{o_j}/\hat{v}_g}(\mathrm{s}) = \left.\frac{\hat{v}_{o_j}(\mathrm{s})}{\hat{v}_g(\mathrm{s})}\right|_{\hat{d}=0} \quad j = 1,2,3 \tag{35}$$

$$H_{\hat{v}_{o_j}/\hat{d}}(\mathrm{s}) = \left.\frac{\hat{v}_{o_j}(\mathrm{s})}{\hat{d}(\mathrm{s})}\right|_{\hat{v}_g=0} \quad j = 1,2,3 \tag{36}$$

$$Z_{\hat{v}_{o_j}/\hat{i}_{o_k}}(\mathrm{s}) = -\left.\frac{\hat{v}_{o_j}(\mathrm{s})}{\hat{i}_{o_k}(\mathrm{s})}\right|_{\hat{v}_g=0,\hat{d}(\mathrm{s})=0} \quad j = 1,2,3, k = 1,2,3 \tag{37}$$

Here, $Z_{\hat{v}_{o_j}/\hat{i}_{o_k}}$ for $j = k$, represents the self-output impedance, and $Z_{\hat{v}_{o_j}/\hat{i}_{o_k}}$ for $j \neq k$, represents the cross- output impedance. These can be easily obtained by applying a voltage disturbance on the output sides. It is notable that these transfer functions depend on the operating points of the converter.

4 | VOLTAGE LOOP CONTROLLER DESIGN

In the intended voltage control method, weighted output voltages, $\hat{v}_w$ and switching duty cycle, $\hat{d}$ are considered as output and input signals, respectively. In this way, from Equations 29 and 30, the dynamic model of the converter can be developed as follows:

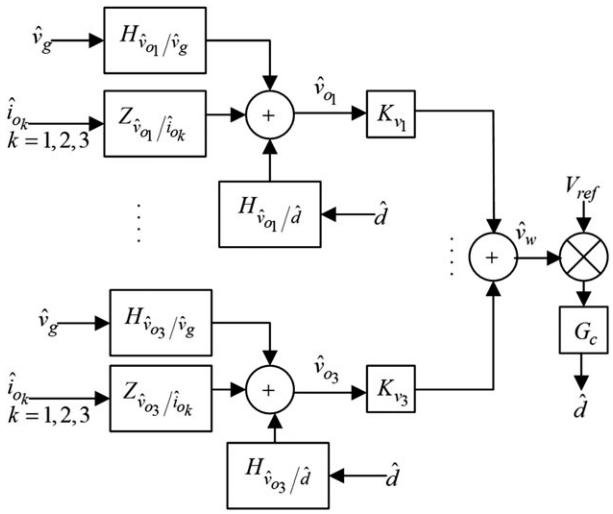

FIGURE 5 Dynamic interactions between small-signal input and output variables

$$
\begin{aligned}
&\dot{\hat{\mathbf{x}}}=\mathbf{A}_{wr}\hat{\mathbf{x}}+\mathbf{B}_{wr}\hat{\mathbf{u}}\\
&\hat{\mathbf{y}}=\mathbf{C}_{wr}\hat{\mathbf{x}}\\
&\hat{\mathbf{x}}=\begin{bmatrix}\hat{i}_{lm}\\ \hat{v}_{o_1}\\ \hat{v}_{o_2}\\ \hat{v}_{o_3}\end{bmatrix},\hat{\mathbf{y}}=[\hat{v}_w],\hat{\mathbf{u}}=\begin{bmatrix}\hat{d}\end{bmatrix}\\
&\mathbf{C}_{wr}=\begin{bmatrix}0 & K_{v_1} & K_{v_2} & K_{v_3}\end{bmatrix}\\
&\mathbf{A}_{wr}=\begin{bmatrix}\frac{r_m}{L_m} & \frac{g_{v_1}}{L_m} & \frac{g_{v_2}}{L_m} & \frac{g_{v_3}}{L_m}\\ \frac{g_{i_1m}}{C_1} & \frac{R_1-r_{11}}{C_1R_1r_{11}} & \frac{1}{C_1r_{12}} & \frac{1}{C_1r_{13}}\\ \frac{g_{i_2m}}{C_2} & \frac{1}{C_2r_{21}} & \frac{R_2-r_{22}}{C_2R_2r_{22}} & \frac{1}{C_2r_{23}}\\ \frac{g_{i_3m}}{C_3} & \frac{1}{C_3r_{31}} & \frac{1}{C_3r_{32}} & \frac{R_3-r_{33}}{C_3R_3r_{33}}\end{bmatrix},\mathbf{B}_{wr}=\begin{bmatrix}\frac{g_{vd}}{L_m}\\ \frac{g_{i_1d}}{C_1}\\ \frac{g_{i_2d}}{C_2}\\ \frac{g_{i_3d}}{C_3}\end{bmatrix}
\end{aligned}
\tag{38}
$$

where r_m, g_{i_1m}, g_{i_2m}, and g_{i_3m} are substituted by zero in DCM. K_{v_1}, K_{v_2}, and K_{v_3} are weighting coefficients of v_{o_1}, v_{o_2}, and v_{o_3}, respectively. The control-to-output transfer function, $H_{\hat{v}_w/\hat{d}}$, is obtained by

$$
H_{\hat{v}_w/\hat{d}}(\mathrm{s})=\left.\frac{\hat{v}_w(\mathrm{s})}{\hat{d}(\mathrm{s})}\right|_{\hat{v}_g=0}=\mathbf{C}_{wr}(s\mathbf{I}-\mathbf{A}_{wr})^{-1}\mathbf{B}_{wr}. \tag{39}
$$

The feedback loop control contains a compensation circuit, and its output is connected to PWM block. Compensation is designed based on stability analysis and to achieve proper bandwidth. In multi-input multi-output time-invariant system, all poles of the closed-loop transfer functions from any input-to-any output, or the eigenvalues of the closed-loop system matrix must be lain on the left-half-plate to achieve a stable system. These functions can be found by small-signal control block diagram depicted in Figure 5. A PID controller, $G_c(s)$, is suggested here in order to regulate the weighted voltages in DCM and CCM. Figure 6 illustrates the proposed control diagram. As shown in Figure 6, the loop gain $T_{wr}(s)$ can be written as

$$
T_{wr}(\mathrm{s})=G_c(\mathrm{s})H_{\hat{v}_w/\hat{d}}(\mathrm{s}). \tag{40}
$$

5 | CASE STUDIES

5.1 | Circuit description

In this paper, a laboratory-scale flyback converter with single input-3 outputs and a RCD clamp is implemented which its electrical parameters are reported in Appendix. The clamping circuit is generally used in order to limit the voltage spike on the switch, when the switch is turned off. The converter can operate in both DCM and CCM as the load condition, duty cycle of switch, and input voltage vary. The converter power rating is 45 W, and maximum average current of 2.5 A is achievable for each output. Maximum duty cycle of flyback switch sets to be 0.6, and input voltage range is limited between 15 and 38 V. The full load condition is realized by operating in CCM. For operation in both modes, the

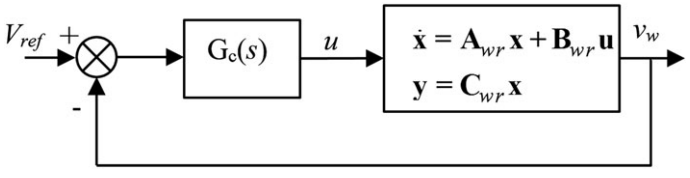

FIGURE 6 Closed-loop system block diagram

magnetizing inductance of the transformer is designed based on full load condition with minimum input voltage, $V_g = 15$ V and $D = 0.6$ and considering power conversion efficiency of 80%. In the transformer design, an EE type ferrite core with suitable size is selected. The primary winding is placed innermost on the bobbin, and then the secondary windings are placed close to the primary side winding on the next layers. A power MOSFET IRF740 is used as the converter switch with $V_{DS(max)} = 400$ V. Three MBRF20100CT Schottky diodes are placed in secondary sides. At the output side of the converter, several electrolytic and polyester capacitors in parallel are usually used to achieve a very low output ripple voltage. Figure 7 shows hardware setup in which the controller schemes in DCM and CCM are implemented on an ARM Cortex-M3. Based on the limited computation and ADC capabilities of the microcontroller, a sampling time equal to 0.2 ms was used, and controller design is done according to this sampling time. The control algorithm is downloaded from a laptop to the header board via a USB JTAG programmer. In following studies, non-identical loading condition in outputs is also considered in evaluating system performance.

5.2 | Steady-state performance

In this analysis, the focus is on illustrating the convergence of modeling predictions and experimental results. Figure 8 shows current and voltage waveforms of the converter obtained by measurement data for a specific operating point in DCM. In this operating point, $R_1 = 14.9\ \Omega$, $R_2 = 10\ \Omega$, and $R_3 = 7\ \Omega$, and V_g and D set at 32.2 V and 0.3, respectively. Table 1 reports the parameters of the current waveforms from modeling predictions and measurement data. According to Figure 3A, piecewise-linear representation for magnetizing current waveform leads to staircase waveform for voltage across magnetizing inductor which is suitable for averaging purposes. As can be seen in Figure 8E, a staircase waveform for voltage across primary side (which can be assumed to be approximately as the magnetizing voltage, v_m) has also been achieved in the practical case. As shown, the measured parameters are in good agreement with their predictions. Minor differences are due to non-ideality components and mismatching in actual component values between the averaged model and hardware prototype. It is notable that the oscillations of the currents in Figure 8 are due to reverse recovery time of the diodes and the parasitic capacitance of the MOSFET. These oscillations do not have a considerable effect on accurate dynamic modeling and do not change the equilibrium point. Because, the equilibrium point refers to average-value of state and other input/output variables, which will not change significantly in the presence of the ringing, reverse recovery effects, and switching edge transients. On the other hand, as previously mentioned, the small-signal responses of a switched-mode power converter may be accurately predicted up to one third of the switching frequency (ie, much slower than the very fast dynamics related to the parasitic phenomena's), using proper averaged models. Therefore, because the average value of the ringing's due to parasitic elements and also diode reverse recovery are zero within a duty cycle (as can be seen in Figure 8), these oscillations do not have any effect while using average model.

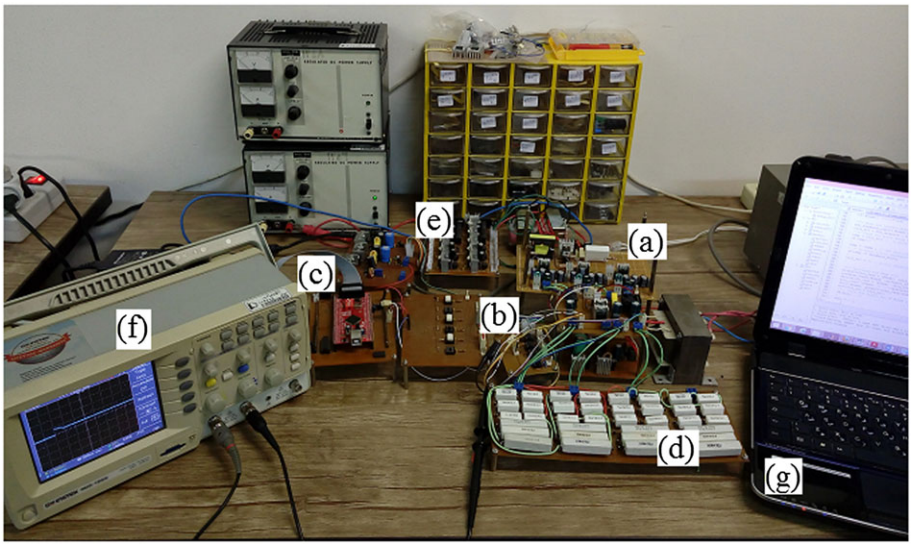

FIGURE 7 Hardware setup: (A) multiple-output flyaback converter, (B) sensor board, (C) ARM board, (D) output loads, (E) DC sources, (F) oscilloscope, (G) laptop [Colour figure can be viewed at wileyonlinelibrary.com]

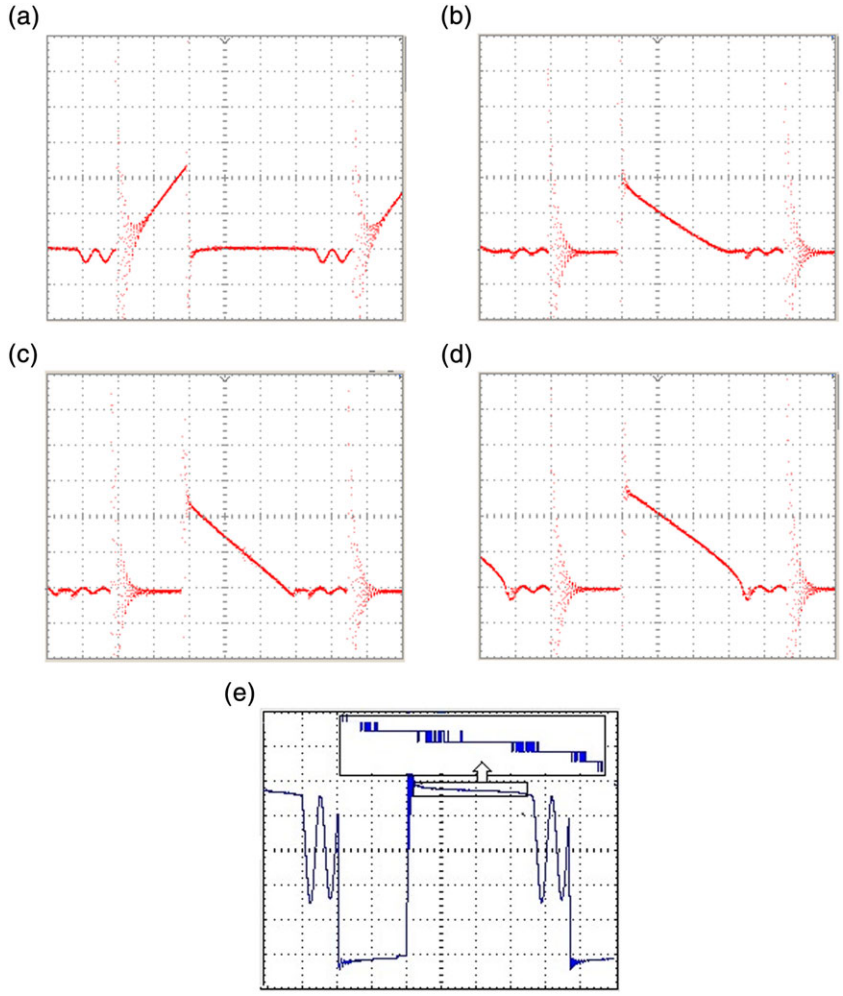

FIGURE 8 Measured waveforms for operating in DCM with $D = 0.3$ and $V_g = 32.2$, (A) i_g, (B) i'_1, (C) i'_2, (D) i'_3, scale is 1 A/div, and (E) voltage across primary winding, scale is 10 V/div. Time scale is 5 μs/div [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Calculated and measured waveform parameters related to Figure 8

Parameter	D_1	D_2	D_3	i_{p_0}, A	$i_{p_{11}}$, A	$i_{p_{21}}$, A	$i_{p_{31}}$, A	$i_{p_{22}}$, A	$i_{p_{32}}$, A	$i_{p_{33}}$, A
Calculated	0.38	0.44	0.51	2.7	2.3	2.36	2.5	0.51	1.2	0.85
Measured	0.39	0.43	0.52	2.5	2	2.4	2.65	0.3	0.95	0.7

5.3 | Dynamic performance

5.3.1 | Frequency response

In Section 3.3, 3 types of input-to-output transfer function are defined for the converter. In each type, several input-to-output transfer functions can be identified for the converter. Here, a sample of each type, namely $H_{\hat{v}_{o_1}/\hat{d}}$, $H_{\hat{v}_{o_1}/\hat{v}_g}$, $Z_{\hat{v}_{o_1}/\hat{i}_{o_1}}$, and $Z_{\hat{v}_{o_1}/\hat{i}_{o_2}}$ are considered to show the agreement between modeling predictions, simulation and measurement results in frequency domain. To investigate the ability of the proposed model in various operational modes of the converter, the operating points of the converter to supply different output loads are D = 0.3 and V_g = 32.2 V (for DCM), D = 0.55 and V_g = 25 V (for CCM_1), and D = 0.6 and V_g = 15 V (for CCM_2). In CCM_1, i_1 drop to zero before the switching cycle is completed at T_s. However, due to continuation of i_2 and i_3 until T_s, i_{lm} will be continuous in the entire switching

period. In CCM_2, the output diodes conduct current for the whole duration of $(1 - d)T_s$. The bode plots of $H_{\hat{v}_{o_1}/\hat{d}}$ are depicted in Figure 9 for DCM, CCM_1, and CCM_2 operations. Figure 10 shows magnitude plots of $H_{\hat{v}_{o_1}/\hat{v}_g}$, and Figure 11 illustrates the magnitude plot of the self-output impedance $\left(Z_{\hat{v}_{o_1}/\hat{i}_{o_1}}\right)$ and cross-output impedance $\left(Z_{\hat{v}_{o_1}/\hat{i}_{o_2}}\right)$ for DCM and CCM_2 operations. In these figures, the solid line curves represent the predicted results, and marks (○) and (■) denote numerical simulation and hardware measurement results, respectively. Numerical simulations are conducted using PSIM software. As shown in Figures 9–11, there is an acceptable match between modeling predictions, simulation, and measurement results for DCM and CCM operations of the converter.

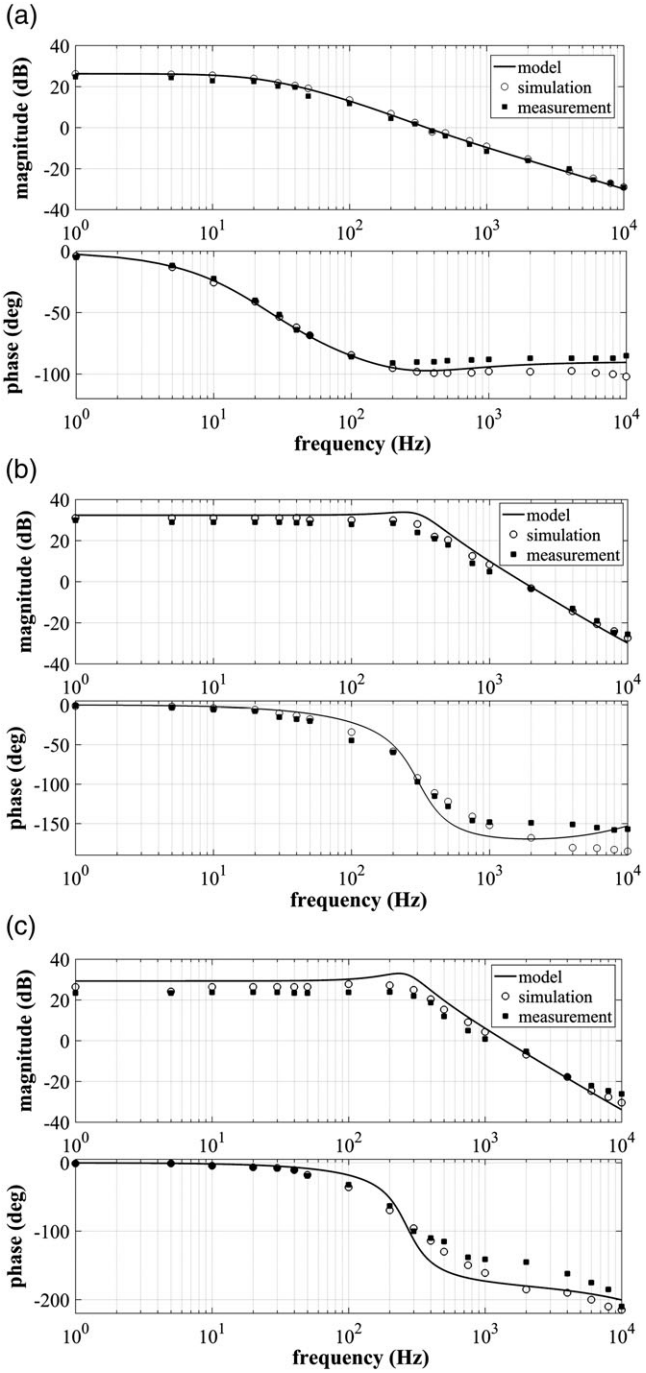

FIGURE 9 Prediction, simulation, and measurement of $H_{\hat{v}_{o_1}/\hat{d}}$ in (A) DCM, (B) CCM_1, and (C) CCM_2 operations

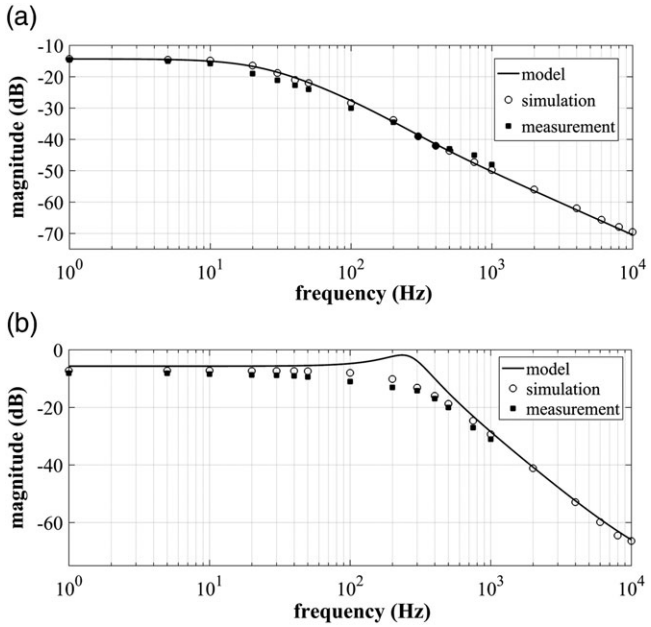

FIGURE 10 Prediction, simulation, and measurement of $H_{\widehat{v_{o_1}}/\widehat{v_g}}$ in (A) DCM and (B) CCM_2 operations

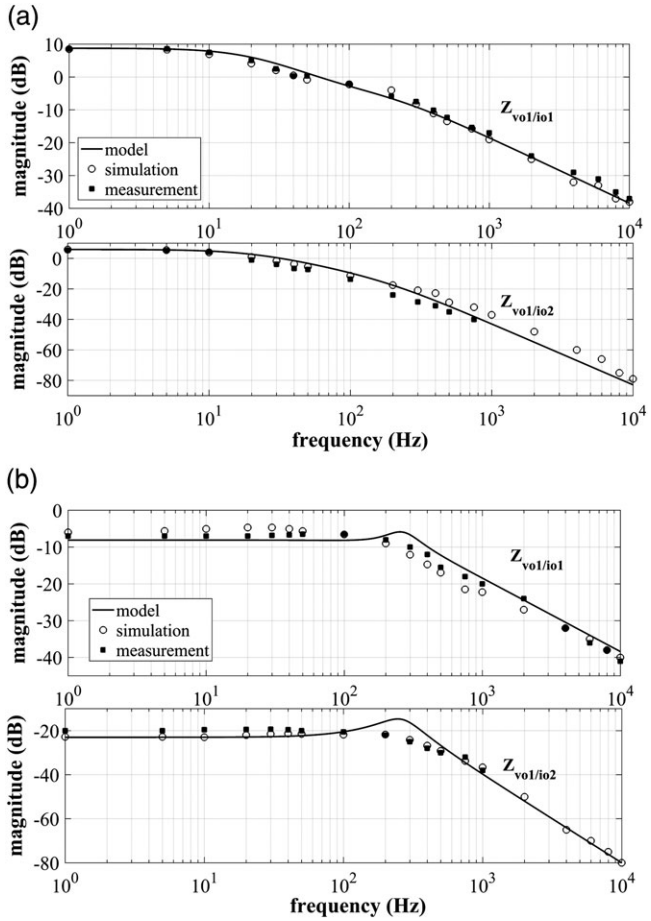

FIGURE 11 Prediction, simulation, and measurement of $Z_{\hat{v}_{o_1}/\hat{i}_{o_1}}$ and $Z_{\hat{v}_{o_1}/\hat{i}_{o_2}}$ in (A) DCM and (B) CCM_2

5.3.2 | Closed-loop system

The focus in this section is to examine the closed loop system performance when the feedback loop is designed according to the proposed dynamic model. With respect to the weighted voltage-mode control based on duty cycle (of switch) input-to-weighted output voltages, Table 2 shows the numerical gain, poles, and zeroes of intended transfer function which are conducted using MATLAB software. As can be seen, the transfer function of continuous condition modes includes a right half-plate (RHP) zero. Contrary to CCM, there is no RHP zero in DCM. The presence of a RHP zero in CCM operation of the flyback converter has been proven in previous researches, in which the currents through all output windings continue until the next switching cycle.[2] In CCM, due to a RHP zero in transfer function, both operating conditions CCM_1 and CCM_2 are considered to develop the closed-loop system. This helps in choosing the operating point as the criteria for feedback network design. It is shown that a RHP zero is also observed in CCM_1 in which only some of the induced currents in the output windings are continuous and the others may be discontinuous when the switch is off. But, this zero is much farther to the right than the RHP zero of CCM_2.

TABLE 2 Numerical poles, zeros, and gain of $H_{\hat{v}_w/\hat{d}}$

Operation	Poles	Zeros	Gain
$DCM^{(i)}$	−2118, −1248, −147.9	−1212, −2093	20.27
$CCM_1{}^{(ii)}$	$-781 \pm j1760$, −1492, −2223	−1610, −2218, 3.789×10^5	39.73
$CCM_2{}^{(iii)}$	$-561.5 \pm j1583.3$, −1789, −1928	−1786, −1912, 3.407×10^4	27.11

(i) $D = 0.3$, $V_g = 32.2$ V, output loads: $R_1 = 14.9\ \Omega$, $R_2 = 10\ \Omega$, $R_3 = 7\ \Omega$.

(ii) $D = 0.55$, $V_g = 25$ V, output loads: $R_1 = 10\ \Omega$, $R_2 = 7\ \Omega$, $R_3 = 3.9\ \Omega$.

(iii) $D = 0.6$, $V_g = 15$ V, output loads: $R_1 = 4.7\ \Omega$, $R_2 = 3.9\ \Omega$, $R_3 = 2.5\ \Omega$.

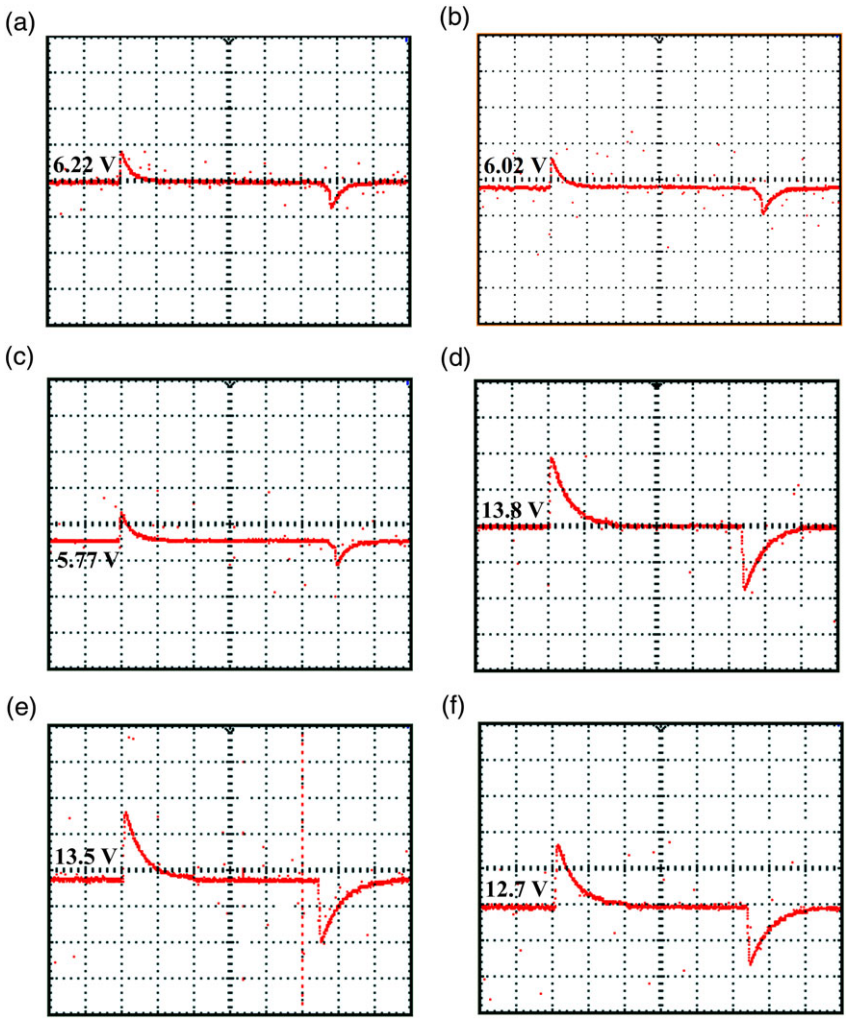

FIGURE 12 Measurement converter response to ±5-V step change in V_g, (A) V_{o_1}, (B) V_{o_2}, and (C) V_{o_3} for DCM and (D) V_{o_1}, (E) V_{o_2}, and (F) V_{o_3} for CCM, scales are 1 V/div and 500 ms/div [Colour figure can be viewed at wileyonlinelibrary.com]

A RHP zero in transfer function causes a reversal phase and response in high frequencies and therefore limits control bandwidth. If PID zeroes are tuned lower than RHP zero, then phase lag due to RHP zero is canceled out and the closed-loop system can still be stabilized with adequate bandwidth. In addition to avoid a further phase lag due to resonant frequencies[2] of the converter circuit, it is better that PID zeroes are placed around resonant frequencies. It must be noted that optimum tuning of controller coefficients, K_p, K_i, and K_d is not within the scope of this paper. These coefficients are tuned to stabilize the system with larger bandwidth in various loading conditions. One simple and practical way is designing the feedback network for low input voltage and heavy load condition with enough phase and gain margin. So, K_p, K_i, and K_d are set at 5×10^{-4}, 25, and 5.65×10^{-8}, respectively, for CCM operation and are set at 9.6×10^{-3}, 0.3, and zero, respectively, for DCM operation. Meanwhile, in this study, weighting factors $K_{v_1} = 0.3$, $K_{v_2} = 0.33$, and $K_{v_3} = 0.37$ are considered.

1. *Line regulation*. Line regulation is one of the general approaches to predict the closed-loop performance of the converter. In this approach, regulation ability of the closed-loop system in attenuating small-signal disturbance from input voltage to converter output voltage is investigated. In this connection, the frequency response of the converter was depicted in Figure 10. Figure 12 shows dynamic response of the closed-loop system to 2 step changes (±5 V) in the input voltage, V_g for both DCM and CCM operations. In DCM, initial input voltage is equal to 32.2 V, and the output loads have been adjusted in $R_1 = 14.9\ \Omega$, $R_2 = 10\ \Omega$, and $R_3 = 7\ \Omega$. In CCM, the initial input voltage is same as before and the output loads are $R_1 = 25.6\ \Omega$, $R_2 = 14.9\ \Omega$, and $R_3 = 7\ \Omega$. The proposed controller adjusts the duty cycle to change input current of the converter and achieves a constant output voltage.
2. *Load regulation*. The load regulation performance of the closed-loop system to 100% step changes in the load, R_1, is illustrated in Figure 13 for DCM and CCM operations. In this case, input voltage is kept constant, and controller

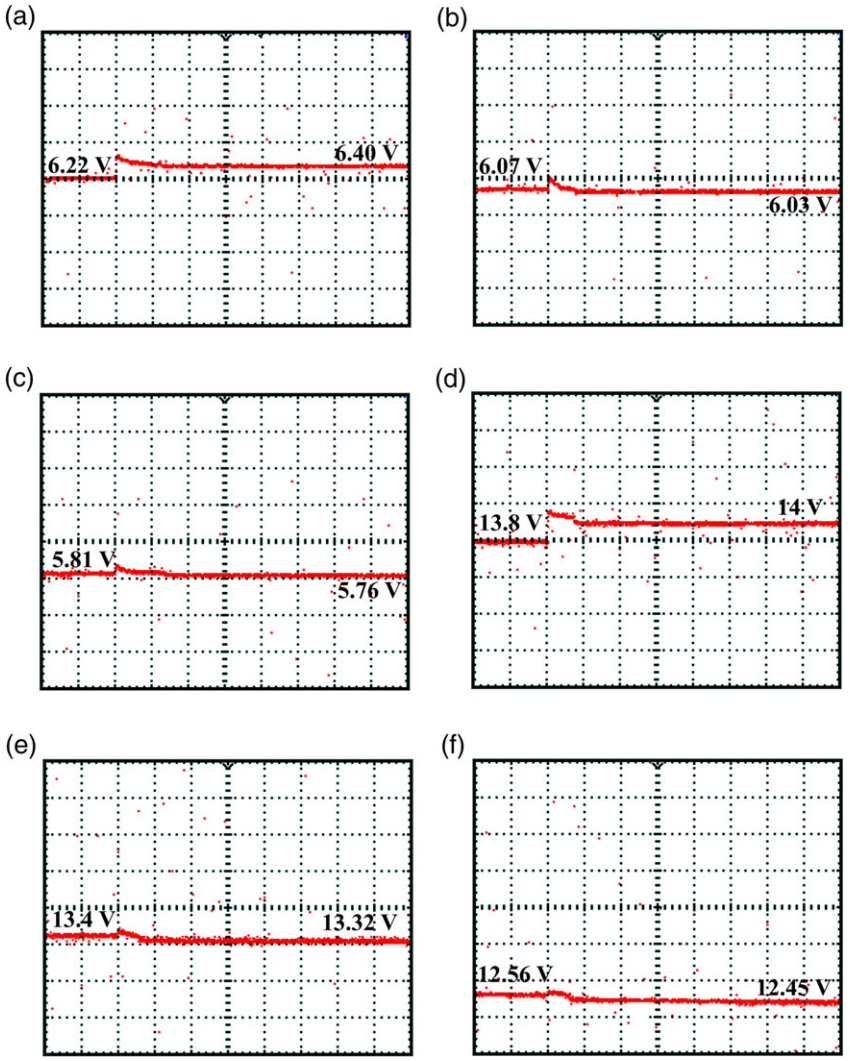

FIGURE 13 Measurement converter response to 100% step change in R_1, (A) V_{o_1}, (B) V_{o_2}, and (C) V_{o_3} for DCM and (D) V_{o_1}, (E) V_{o_2}, and (F) V_{o_3} for CCM, scales are 0.5 V/div and 500 ms/div [Colour figure can be viewed at wileyonlinelibrary.com]

adjusts duty cycle of switch to regulate weighted output voltages, V_w, in a narrow band around of a fixed value. As shown in Figure 13, the output voltages are not constant individually, but V_w is kept in desired level by controller. Meanwhile, here the input voltage and the output loads are considered the same as previous study.

6 | CONCLUSION

This paper proposes a new approach to generate a small-signal averaged model for multiple-output flyback converters. This approach is based on an analytical model derived by analyzing the piecewise-linear current waveforms of the inductances inside the converter. The operational principle of the analytical model has been investigated in both continuous and discontinuous condition mode (CCM and DCM). The proposed averaged model can be useful in identical and non-identical loading conditions. Dynamic characterization study is performed for analyzing the weighted voltage-mode regulation. The proposed model is verified using a laboratory-scale prototype under the time and frequency domain studies. The controller design is done for both CCM and DCM, and then dynamic performances of the overall system are evaluated. As shown, the measurement results justify the proposed model.

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APPENDIX

1. Semiconductor devices:

   MOSFET: IRF740; diodes: MBRF20100CT

2. Circuit parameters:

$f_s = 30$ kHz (switching frequency), $L_m = 115$ μH, $L_{kp} = 5$ μH, $L_{ks_j} = 10$ μH for $j = 1,2,3$ (referred to primary side), $n = 20/7$, $R_s = 10$ KΩ, $C_s = 15$ nF, $C_1 = C_2 = C_3 = 1320$ μF.

3. Feedback loop micro-controller:

   LPC1768 32-bit ARM Cortex-M3/NXP.