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Realization of a broadband Hybrid X-Band Power Amplifier Based on f_T-Doubler Technique

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Abstract: This paper presents the design steps for the fabrication of a hybrid microwave power amplifier (PA) based on f_T-doubler technique. The PA is implemented using two 6 W discrete GaN-HEMTs on SiC substrate. The f_T-doubler technique is used to enhance the frequency response and bandwidth of the PA as compared to the common source (CS) configuration. Accurate simulation results show about 90% improvement in the unity current gain frequency (f_T) for the f_T-doubler structure in comparison with a common-source parallel structure. However, the hybrid realization of a high-frequency PA based on f_T-doubler technique is challenging mainly due to severe thermal management failures and large parasitic effects of the interconnections such as bond wires and long microstrip lines. The proposed hybrid integrated strategy relieves the thermal problem while the parasitic effects are well controlled. Thermal analysis and accurate 3D thermal simulation of the proposed hybrid integrated structure show that the channel temperature of transistors does not exceed its maximum tolerable value. Implementing the optimal source/load pulls for the transistors and well-designing the input/output matching networks by considering the parasitic effects of the interconnections result in a fabricated PA with a broad bandwidth of 6.5-10.4 GHz, a sufficient small-signal gain of 10 dB, a considerably high output power (P_{out}) of around 10 W and a power added efficiency (PAE) of 43% at 8 GHz.

Index Terms—Darlington pair amplifier, f_T-doubler technique, high electron mobility transistor (HEMT), microwave power amplifier, thermal management.

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I. INTRODUCTION

Microwave power amplifiers (PAs), as the main part of a transceiver, are often used in different applications such as telecommunication systems and medical instruments. Microwave PAs are designed based on monolithic integrated circuits (MMIC) and hybrid circuits. Designs based on MMIC procedure are reliable and well-suited for mass production; however, it is expensive for limited production. The hybrid fabrication is cost-effective and straightforward for customized production in a short production lead time.

Hybrid microwave PAs are often realized using discrete high electron mobility transistors (HEMTs), especially discrete GaN-HEMT on SiC, due to the high-velocity saturation, the big breakdown voltage of GaN and excellent thermal conductivity of SiC substrate [1-4]. Microwave PAs are usually configured as common-source (CS) and categorized into different classes for achieving optimum efficiency, power gain, and output power [5]. Sometimes several transistors are used in parallel to enhance output power capability. It is apparent that the output power of the parallel structure is proportional to the number of transistors; however, the frequency response of a parallel structure usually degrades by increasing the number of transistors. In general, a hybrid PA based on CS configuration is easy to realize; however, achieving a broad bandwidth without sacrificing gain or output power is still a challenging task.

The limited bandwidth of a hybrid PA originates from the undesired parasitic effect of the interconnections as well as the limited frequency response of the discrete transistors. For enhancing the frequency response of the integrated amplifier, some techniques such as cascode configuration, distributed amplifiers, and Darlington structure have been proposed [6-13]. The cascode structure is used in high gain applications to reduce the Miller effect of the gate-drain capacitor. To achieve high output power, the cascode configuration needs a higher power supply in comparison with a similar CS configuration. In the distributed

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technique, the parasitic effects of each transistor are absorbed into the transmission lines which leads to improving f_{max} and gain-bandwidth product [14]. Although the bandwidth of the distributed amplifier is proportional to the number of transistors, the output power of the distributed amplifier is limited. Darlington cell is also used to improve f_T greater than twice of that of a CS configuration so that the amplifier based on Darlington cell has more gain-bandwidth than a conventional CS structure. The output power of a Darlington configuration demonstrates a linear dependency on the number of transistors. However, this technique suffers from inequality of the drains current at low frequencies [15]. To resolve the inequality problem of the Darlington cell, some researchers have proposed a modified Darlington cell, known as f_T-doubler cell [15-18]. The amplifier based on the f_T-doubler cell is suited for both high output power (proportional to the number of transistors) and high-frequency response.

Realization of the microwave PAs based on Darlington/f_T-doubler cells in MMIC technology has been reported in some previous publications [15, 18, 19]. However, based on our best knowledge, the hybrid realization of the microwave PA based on the f_T-doubler cells with broad bandwidths has not been reported yet. This paper focuses on the integration of a broadband hybrid microwave PA based on the f_T-doubler technique using discrete GaN-HEMTs on SiC. The realization of a hybrid f_T-doubler cell is accompanied by thermal challenging, instability and undesired effects of the interconnections on the output performance. In this paper, a methodical approach is followed to resolve the thermal problem and take the advantages of the f_T-doubler configuration.

The rest of this paper is organized as follows. Section 2 investigates a conventional f_T-doubler configuration, a parallel CS configuration, and a Darlington pair. In Section 3, the thermal issues in the realization of the PA based on the f_T-doubler cell are investigated. In Section 4, the design considerations related to the load-pull and matching networks are presented. The simulation and measurement results are presented in Section 5.

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II. Theoretical Consideration of the Conventional F_T-Doubler Structure

Fig. 1(a) shows the modified Darlington configuration consists of a conventional Darlington pair and a series combination of R_S and L_S. Essentially Darlington pair is used to enhance the electrical characteristics of an amplifier such as current gain and frequency response. The output power of a well-matched Darlington pair is the same as that of the parallel configuration (Fig. 1(b)). Hence, the Darlington pair is a superior topology in high power, high speed, and broadband applications. The Darlington structure is made of two or more discrete HEMTs, particularly in the integration of a PA for high-frequency applications [19]. In Fig. 1(a), the Darlington structure comprises two transistors in which the first transistor (T_1) amplifies the input signal and drives the second transistor (T_2).

Fig. 2 shows a simplified small signal hybrid-pi model of a 1.25 mm GaN-HEMT on SiC adapted from TriQuint Company [20]. In Fig. 2, the gate-source terminal, consists of C_{gs} and R_i, acts as a high-pass filter and suppresses low frequencies components. For Darlington structure, the gate-source of T_2, which is in series with T_1, represents a high-pass filtering behavior. As a result, the output current at low frequencies, cannot pass through T_1, that is,

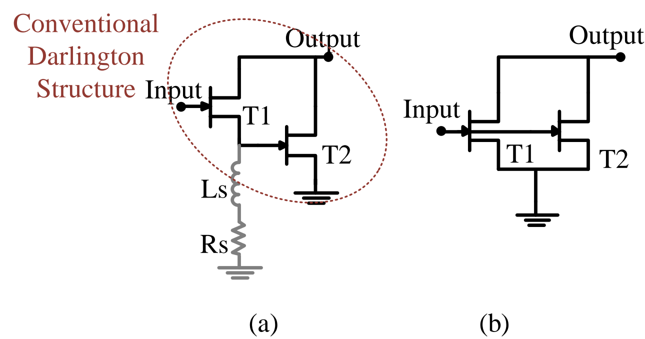
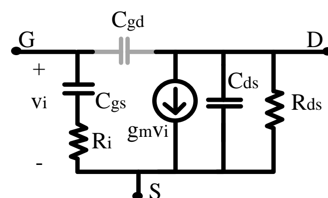


Fig. 1. a) Modified Darlington configuration (f_T-doubler cell). b) Parallel common-source configuration.



Notation	Value	Unit
C_{gd}	0.064	pF
C_{gs}	1.79	pF
C_{ds}	0.308	pF
R_i	0.26	Ω
R_{ds}	124	Ω
g_m	0.27	℧

Fig. 2. Simple small-signal hybrid-pi model of the GaN-HEMT on SiC adapted from [20].

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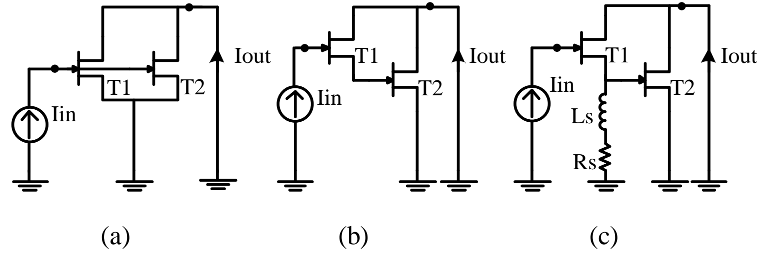

Fig. 3. Different configurations used for simulating the current gains versus frequency; a) parallel common-source configuration, b) Darlington configuration, and c) f_T-doubler configuration.

the whole output current passes through T_2 [15, 16]. In other words, the drains current ratio of T_1 to T_2 varies in term of frequency, so that, at high frequencies both T_1 and T_2 provide the output current whereas at low frequencies the output current is just provided by T_2. Therefore, the power capability of T_2 should be at least twice that of T_1.

The f_T-doubler cell is a modified Darlington pair to resolve the inequality of the drains current. The f_T-doubler cell uses a series combination of an inductor (L_S) and a resistor (R_S) in parallel with the gate-source of T_2 [15]. The time constant of the series combination of L_S and R_S, (L_S/R_S), should be less than or equal to the time constant of C_{gs} and R_i, ($R_i \times C_{gs}$). In this state, at low frequencies, the drain current of T_1 passes through L_S and R_S.

As already mentioned, the Darlington pair and f_T-doubler cells provide better high-frequency responses compared to the common-source configuration. Just for a brief frequency comparison, the unity current gain frequency (ω_T) of three configurations, as shown in Fig. 3,

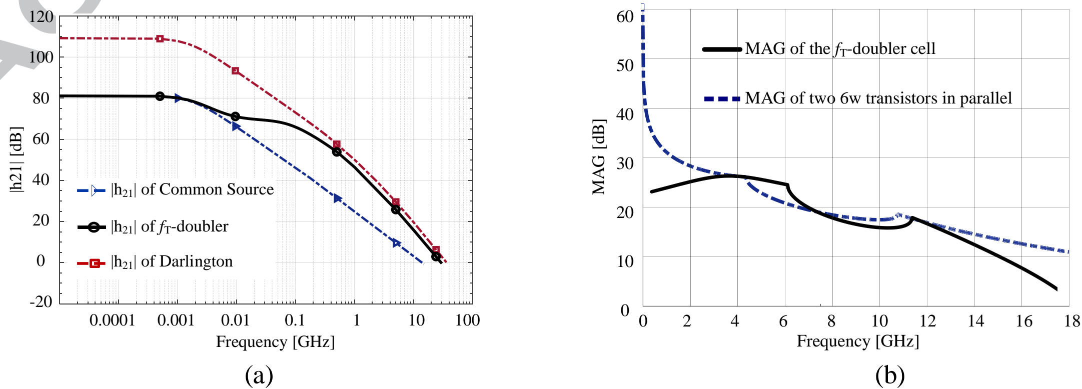

Fig. 4. a) Magnitude of h_{21} versus frequency for the parallel common-source, Darlington and f_T-doubler configuration, b) MAG of the f_T-doubler cell (shown in Fig. 1(a)) with *Ls* of 0.3 nH and *Rs* of 20 Ω in comparison with that of the parallel structure in Fig. 1(b).

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are analyzed and simulated. The analyses are performed based on the small signal hybrid-pi model shown in Fig. 2 by neglecting the effect of C_{gd}.

For the parallel common-source structure shown in Fig. 3(a), ω_T is calculated as follows.

$$\frac{I_{out}}{I_{in}}(j\omega_T)=1 \Rightarrow \omega_{T_{CS}} \approx \frac{g_m}{C_{gs}} \tag{1}$$

where, g_m shows transistor transconductance, and C_{gs} is the gate-source capacitor.

Based on Fig. 3(b), ω_T for the Darlington pair is calculated as follows.

$$\frac{I_{out}}{I_{in}}(s)=\left(2g_m+g_m^2\left(\frac{1}{C_{gs}s}+R_i\right)\right)\times\left(\frac{1}{C_{gs}s}+R_i\right) \tag{2}$$

$$\frac{I_{out}}{I_{in}}(s)\approx\left(\frac{2g_mC_{gs}s+g_m^2}{C_{gs}^2s^2}\right) \tag{3}$$

$$\omega_{T_{Darlington}} \approx \frac{\left(1+\sqrt{2}\right)g_m}{C_{gs}} \approx 2.41\omega_{T_{CS}} \tag{4}$$

According to (4), Darlington configuration has a bigger ω_T than a common-source structure that makes it an excellent choice for high-speed applications [19, 21].

For the f_T-doubler structure shown in Fig. 3(c), ω_T varies with the value of the parallel inductance, Ls, as follows (for the sake of simplicity the effect of Rs is neglected).

$$\frac{I_{out}}{I_{in}}(s)\approx\frac{2g_mL_SC_{gs}s+g_m^2L_S}{L_SC_{gs}^2s^2+C_{gs}} \tag{5}$$

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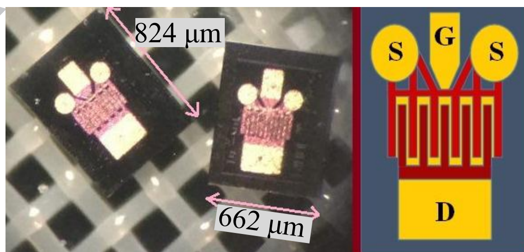
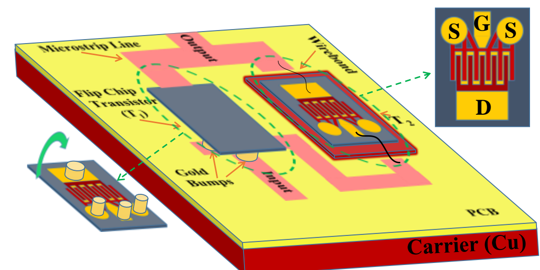


(a)



(b)

Fig. 5. a) Discrete HEMT (662 µm × 824 µm × 100 µm) with one gate pad (G), two source pads (S) and one drain pad (D). b) Design using Flip-chip and surface mounted transistors in order to realize a low power Darlington cell. The bottom plate of the flip-chip mounted transistor does not prepare a suitable path to transfer the heat. The picture is not in real scale.

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Thus, the unity current gain frequency for $L_S \geq (C_{gs}/2g_m^2)$ is obtained as follows.

$$\omega_{T_{f_T_doubler}} \approx \frac{\left(1+\sqrt{2-\frac{C_{gs}}{L_S g_m^2}}\right) g_m}{C_{gs}} \leq \omega_{T_{Darlington}} \qquad (6)$$

Equation (6) shows that the $\omega_{T(f_T\text{-doubler})}$ degrades by decreasing the value of L_S. A well-designed f_T-doubler cell can have a ω_T around twice that of a single transistor.

In Fig. 4(a), a comparison is made among the magnitude of h_{21} for different configurations using the Advanced Design System (ADS) based on the nonlinear model (provided by Modelithics Inc.) [22]. In this simulation, L_S and R_S are 0.3nH and 20 Ω, respectively. According to Fig. 4(a), the f_T values for the parallel common-source PA, f_T-doubler PA and Darlington cell are around 15, 29.5 and 35 GHz, respectively. Fig. 4(b) shows the simulated maximum available gain (MAG) of the f_T-doubler and the parallel CS circuit on one plot.

III. REALIZATION OF THE HYBRID F_T-DOUBLER

The discrete GaN-HEMT, shown in Fig. 5(a), consists of four pads (two symmetrical source contacts, a gate contact, and a drain contact) in front of the transistor and a bottom plate, which is electrically connected to the source pads. An important function of the bottom plate is to disperse the heat away from the transistor channel. Unlike a parallel CS, in an f_T-doubler PA (see Fig. 1(a)) the bottom plate of the source degeneration transistor (T_1) must electrically be isolated from the bottom plate of T_2 and carrier. An answer to this problem can be the flip-chip assembly of T_1 as shown in Fig. 5(b) [23]. Although this approach provides low parasitic interconnections and can be successfully implemented for low power microwave applications, it fails in high power applications, such as microwave PAs, due to the high thermal resistance of T_1 in combination with air. Therefore, to fabricate a hybrid f_T-doubler PA, a suitable structure must be prepared for the realization of a well thermally managed source degeneration transistor (T_1) in series with a grounded transistor (T_2).

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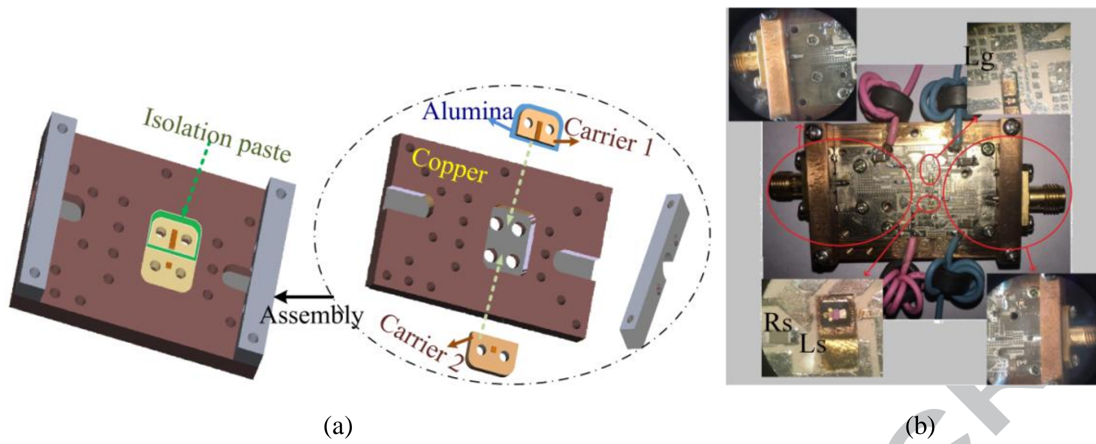

Fig. 6. a) The implemented set-up for electrically isolation of Carrier1 from Carrier2. b) Top view of the fabricated PA using two GaN HEMTs in f_T-doubler configuration.

A. Methods of Fabrication

As already mentioned, and as depicted in Fig. 5(b), the flip-chip mounted T_1 on the printed circuit board (PCB) suffers from a high thermal resistance. In fact, from the thermal management perspective, the bottom plate of the flip-chip mounted transistor is suspended in the air and cannot provide a proper conduction path to transfer the channel heat to the heat-sink [24]. The mismanagement of the channel temperature consequently leads to the degradation of the transistor performance. In this section, a method of fabrication is proposed to resolve the thermal problems to such an extent. The proposed method is explained as follows. At the first step, as shown in Fig. 6(a), two distinct, small and non-identical pieces of copper (Carrier1 and Carrier2) as well as a copper baseplate with a big pit to hold the carriers are provided. The width, length and the thickness of Carrier1 are 5.5 mm, 9 mm and 2.7 mm, respectively, whereas those of Carrier2 are 6.5 mm, 10 mm and 3 mm, respectively. T_1 and T_2 are attached to the copper carriers using $Au_{80}Sn_{20}$ preforms. Note that, separating the two carriers is useful not only for providing a proper electrical connection between the transistors and resolving the heat transfer issue but also it is suitable for reattaching the transistors if needed.

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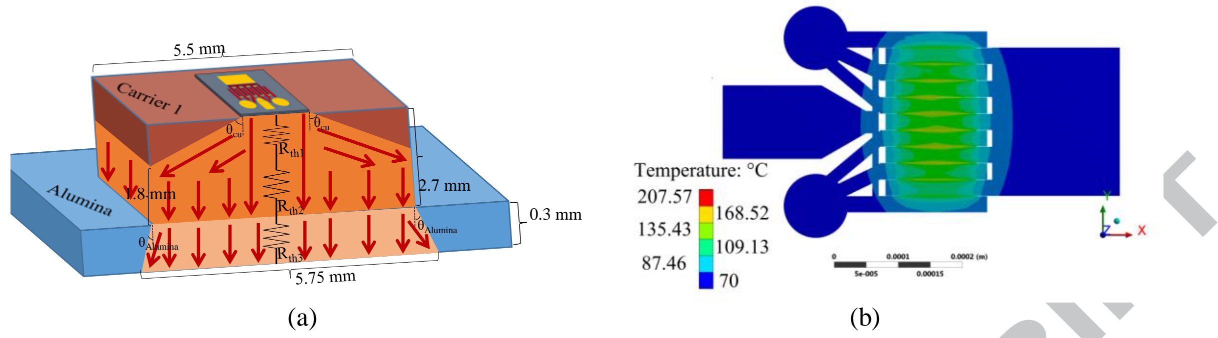

Fig. 7. a) Heat path through Carrier1 and the Alumina layer. b) 3D thermal simulation of T_1 using ANSYS software.

At the second step, the carriers with attached transistors are placed into the pit of the main baseplate. The small dimensions of Carrier1 as compared to the dimensions of Carrier2 is for the electrical separation of Carrier1 from the baseplate. For the electrical isolation, the thickness discrepancy between Carrier1 and Carrier2 is compensated using a layer of Alumina with a thickness of 0.3 mm between the bottom plate of Carrier1 and the floor of the baseplate pit. The Alumina layer functions as a thermally conductive and electrically insulator. The gap between the sidewalls of Carrier1 and the baseplate pit is filled up with an electrically isolated thermal paste. After fixing the carriers, a PCB substrate is placed on the base plate using a thin layer of silver paste as well as five screws.

A photograph of the fabricated PA with f_T-doubler technique is shown in Fig. 6(b).

B. *Thermal behavior*

The PA circuit based on f_T-doubler technique is fabricated using two 6 W discrete GaN on SiC HEMTs with a gate width of 1.25 mm from TriQuint Inc. The power dissipation of the transistors with V_{DD} = 28 V and I_d = 62.5 mA is 1.75 W that under RF drive rises to around 5 W with a 43 percent of PAE. Refer to the transistor datasheet [20]; the thermal resistance of the T_2 in the mentioned condition is 23.2°C/W. With a baseplate temperature of 70°C, the channel temperature is 186°C which is much less than the maximum tolerable channel temperature (275°C). The channel temperature of T_1 is different due to the presence of an Alumina layer under its carrier (Carrier1). Based on the developed method in [24], the

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channel temperature of T_1 is estimated as follows. Note that, the thermal conductivities of Alumina, $Au_{80}Sn_{20}$ preform, and copper are 35 (W/m°C), 57 (W/m°C) and 385 (W/m°C), respectively, also the baseplate temperature is fixed at 70°C.

For a solid, the heat spread angle (θ) is calculated as follows [24, 25]:

$$\theta = 90tanh\left(0.355\left(\frac{\pi k}{180}\right)^{0.6}\right) \tag{7}$$

According to (7) and considering the mentioned thermal conductivities (k); the heat spread angles for copper and Alumina are equal to 72 and 23 degrees, respectively.

Depending on the average heat source area (A) and thicknesses of Carrier1 and Alumina (L), as illustrated in Fig. 7(a), three thermal resistors including R_{th1}, R_{th2} (related to Carrier1), and R_{th3} (across Alumina path) can be calculated as follows [24, 26].

$$R_{th1} = \frac{L}{k.A} = \frac{9\times10^{-4}}{385\times\left(\left(662\times10^{-6}+5.5\times10^{-3}\right)/\,2\right)\times824\times10^{-6}} \approx 0.92\left(\frac{^{o}C}{W}\right) \tag{8}$$

$$R_{th2} = \frac{18\times10^{-4}}{385\times5.5\times10^{-3}\times824\times10^{-6}} \approx 1\left(\frac{^{o}C}{W}\right) \tag{9}$$

$$R_{th3} = \frac{3\times10^{-4}}{35\times\left(\left(5.5\times10^{-3}+5.75\times10^{-3}\right)/\,2\right)\times824\times10^{-6}} \approx 1.85\left(\frac{^{o}C}{W}\right) \tag{10}$$

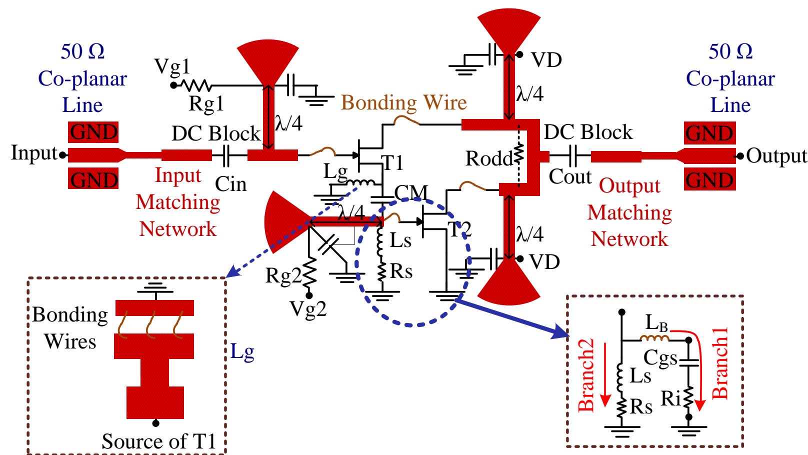

Fig. 8. Schematic diagram of the designed PA based on the f_T-doubler technique. Input and output matching networks are not in real design.

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Therefore, the total thermal resistance from the transistor channel to the bottom plate of the Alumina layer is

$$R_{total} = R_{th\text{-}HEMT} + R_{th1} + R_{th2} + R_{th3} \approx 27\left(\frac{^{\circ}C}{W}\right) \qquad (11)$$

By applying the power of 5 W (Q=5 W) on the channel of T_1, the temperature difference (ΔT) between the channel and the bottom plate of the Alumina layer is calculated as follows.

$$\Delta T = R_{total} \times Q = 27 \times 5 \approx 135\ ^{\circ}C \qquad (12)$$

With the baseplate temperature of 70 °C, the channel temperature would be 205 °C, which is less than the maximum tolerable channel temperature (275 °C). Fig. 7(b) shows the thermal simulation of Fig. 7(a) in a steady state using commercial 3D software of ANSYS. The simulation result is in agreement with the calculations.

IV. Design considerations

Fig. 8 shows the schematic circuit of the PA using the f_T-doubler technique. In this design, the matching networks are realized using microstrip lines. Besides, the wire bonding method is used to make the interconnects between the transistor pads and the matching networks. For the sake of simplicity, each bonding wire is modeled as an equivalent inductor. Momentum simulation in ADS shows that each single bonding wire (with diameter of 25μm and length of

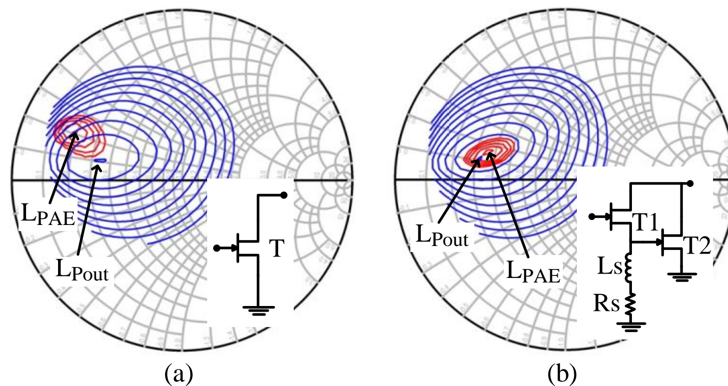

Fig. 9. Load-pull optimizations for the best PAE (L_{PAE}) and the best output power (L_{Pout}). a) Common-source PA (CS). b) f_T-doubler PA.

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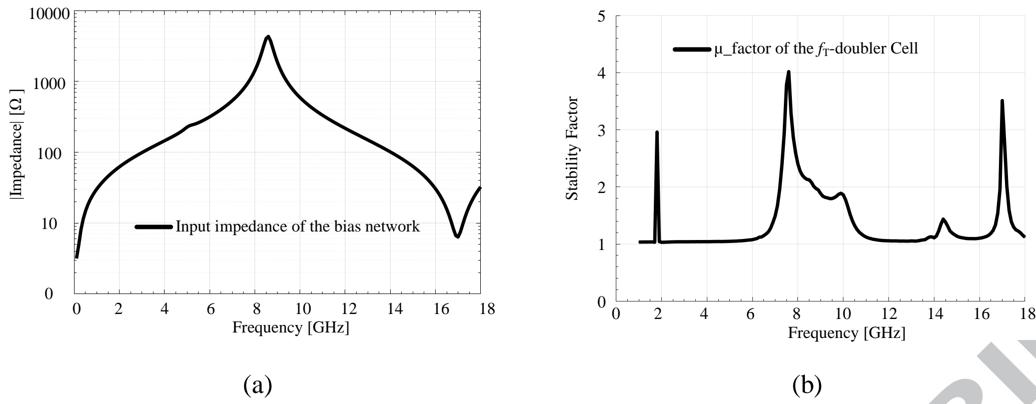

Fig. 10. a) The input impedance of the broadband bias network in term of frequency. b) μ factor of the designed PA based on f_T-doubler technique. μ greater than 1 shows that the circuit is stable.

450μm) represents an inductive behavior of 0.3 nH. The gate interconnects are realized by two bonding wires with an equivalent inductor of 0.15 nH. Four individual bonding wires are used per each drain pad.

The first step in the design of the PA based on Fig. 8 is to calculate L_S and R_S values. As shown in Fig. 8, the combination of L_S and R_S is in parallel with the series combination of the gate bonding wires and the gate-source terminals of T_2. Considering Fig. 8, the resonance frequency (f_r) of Branch1 is calculated as follows.

$$f_r = \frac{1}{\sqrt{C_{gs} \times L_B}} \approx 10\ GHz \qquad (13)$$

where, L_B is used to denote the inductive effect of the gate bonding wires. Note that Branch1 represents a capacitive behavior for frequencies lower than the resonance frequency of 10 GHz. In order to have equal drains currents at low frequencies, the cut-off frequency of Branch2 ($f_{\text{cut-off}}$) should be higher than 10 GHz.

$$f_{cut-off} = \frac{R_S}{2\pi \times L_S}$$

In this design, L_S is realized using a single bonding wire with the inductance of 0.3 nH. To have a cut-off frequency more than 10GHz, R_S should be bigger than 18 Ω. Note that the value of R_S affects the load-pull design and the stability of PA.

Fig. 9(a) shows the load-pull simulation of the CS configuration for the best PAE and output power. The results show that under the condition of V_{DD}=28 V and I_D=62.5 mA (in

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class AB), the optimal load reflection coefficient for the best output power is around 0.47∠165° at 10 GHz. In these conditions, under RF drive, the GaN-HEMT produces around 6W of output power with 59 percent of PAE.

For the f_T-doubler cell, a conservative output power of 5W for each transistor is selected to relax the thermal management and the load/source pulls optimizations. Also, both transistors should have similar load-pulls. The load-pulls and the source pull can be tuned by varying R_S in an iterative approach. Fig. 9(b) shows the simulation results of the optimum load-pull achieved by iteration at 8 GHz. Based on the large-signal simulation results [22], the best source-pull reflection coefficient of T_1 and the similar load-pull reflection coefficient for T_1 and T_2 are 0.8∠-165° and 0.56∠173°, respectively. In Fig. 8, according to the aforementioned calculated source/load pulls, the matching networks are designed using multi-section matching transformers and finally the matching circuits are optimized using ADS to reach the optimum bandwidth. All the passive matching networks are implemented on a laminate ceramic-filled PTFE composite (RO3010) from Rogers corporation with a dielectric constant of 11, the dissipation factor of 0.0022 and the thickness of 10 mils. Several additional practical hints should be considered for the reliable realization of a hybrid X-band PA, based on f_T-doubler technique. They are briefly described as follows.

First, in order to facilitate the successful implementation of the hybrid PA and exploit the advantages of the f_T-doubler configuration, optimum interconnects should be used between the source pad of T_1 and the gate pad of T_2.

Another issue that must be considered is the phase discrepancy between the drain pads of T_1 and T_2 which is solved by adding an extra transmission line to the drain of T_1. Furthermore, in order to achieve an efficient PA with a low phase discrepancy, the path between the source of T_1 and the gate of T_2 must be lossless and as short as possible.

Also, the width of the SMA connectors is wider than that of a microstrip line with the

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characteristic impedance of 50 Ω on RO3010 which causes imperfections and discontinuities. To resolve this problem, as shown in Fig. 8, an input/output 50 Ω co-planar network is designed to coincide with the width of the SMA connectors.

L_g provides a *dc* path for the source of T_1 which is realized using a microstrip line in series with long bonding wires as shown in Fig. 8. The inductive effect of L_g must be considered which is around 5 nH.

The required broadband bias network is obtained using a radial stub followed by a λ/4 microstrip line [27], and its frequency response is shown in Fig. 10(a).

R_g guarantees the even-mode stability of the circuit and reduces the low frequencies noise of the gate power-supply. R_g is equal to 100 Ω.

Also, selecting a proper value for R_S and providing optimum input/output matching networks improve the even-mode stability. Fig. 10(b) depicts the large signal stability simulation of the designed PA. The result shows that the well-designed circuit is stable from 1 to 18 GHz.

Finally, some ferrite rings are used to reduce the unwanted low-frequency noises at the *dc* bias inputs as shown in Fig. 6(b).

V. RESULTS AND DISCUSSION

High frequency response as compared to a common source configuration, proper input/output matching networks and employing broadband bias networks have significant effects on the bandwidth of the circuit. A major challenge here is the trade-off between bandwidth and power gain. In order to reach an optimal result, the matching networks and the elements value, especially R_S, are tuned after fabrication. Note that the matching networks and the quantities of L_S and R_S have a noticeable effect on the even-mode stability of the *PA*.

Fig. 11(a) shows the small-signal simulation and measurement results of the fabricated PA. The small discrepancy between the simulated and measured results is mainly related to the

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parasitic elements due to the solder pasting of the surface of Carrier1 to the pad of capacitor CM and inductor L_g that is very difficult to be considered in simulation. The measurement results show a bandwidth of 3.9 GHz with a small-signal gain of 10 dB.

The large-signal measurement is performed using an average microwave power meter of Marconi 69604 with a thermocouple power sensor which works up to 20 GHz. In doing so, a continuous wave signal generator with a maximum output power of 13 dBm in series to a 2W broadband MMIC PA with a gain of 30 dB excites the input port of the PA. The power of the signal generator is swept from -40dBm to 4dBm, gradually. For each input power, the output power and the *dc* power of the fabricated PA are extracted. Fig. 11(b) shows the extracted output power and PAE versus input power at 8GHz. The output power and the maximum PAE are more than 10W and 43%, respectively. The large-signal gain for the maximum output power is around 9dB. Fig. 11(c) shows maximum output powers in term of frequency.

Due to the lack of successful broadband hybrid Darlington PA designs, our work is compared with some previously fabricated broadband MMIC Darlington PAs in TABLE I. Based on TABLE I, this work provides higher output power and PAE with a comparable gain bandwidth over f_T (GBW/f_T). Generally, two figure of merits (FOM) are used in literature for the evaluation of the broadband microwave PAs [36-40]. They are expressed as follows.

$$FOM_{PA} = P_{out}\,(W) \times PAE(\%) \times Gain(dB) \times f_o^2(GHz) \quad (13)$$

$$FOM_{PA,BW} = FOM_{PA} \times BW(\%) \quad (14)$$

where P_{out}, PAE, $Gain$, f_0 and BW are output power in W, power added efficiency (in percent), the small-signal gain in dB, center frequency in GHz and BW over f_0 (in percent), respectively. TABLE II provides an insight into the output characteristics and performance of the fabricated PA based on the f_T-doubler technique in comparison with the other PAs with different technologies and configurations. Based on TABLE II and from the $FOM_{PA,BW}$ point

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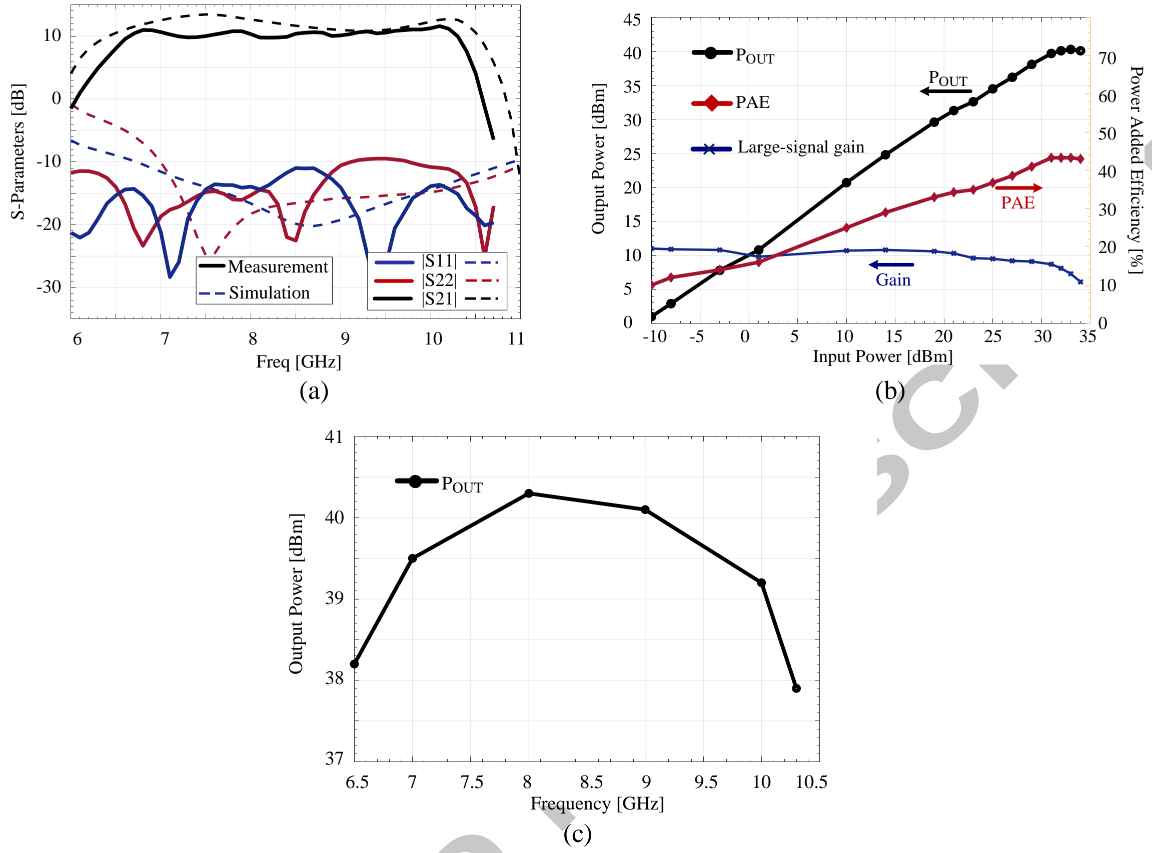

Fig. 11. a) Small signal simulated and measured results of the fabricated f_T-doubler PA b) The measured results of the output power, PAE and large signal gain for the fabricated PA at 8 GHz. c) The maximum output power of the fabricated PA in term of frequency.

of view, our work shows a superior performance in comparison with the previously reported broadband microwave PAs.

TABLE I. Comparison between the performances of the fabricated hybrid PA based on the f_T-doubler technique and some previously published monolithic microwave broadband Darlington PAs.

Ref	Technology	BW (GHz)	$\|S_{21}\|$ (dB)	Pout (W)	PAE_{max} (%)	GBW/f_T	FOM_{PA}	$FOM_{PA,BW}$
[19]	0.25μm MMIC GaAs pHEMT	1.5 - 29.5	17.8	0.033	2.5	217/65	3.5	6.3
[28]	0.8μm RFIC GaN HFET	1 - 6	12.2	2	37	Not reported	111	159
[13]	IPC GaN HEMT	0.2 - 4	10	< 1	25	Not reported	11	20
[10]	MMIC GaAs HEMT	DC - 29.8	10	> 0.1	Not reported	94/36	---	---

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[8]	0. 5µm GaAs HEMT	DC - 16	13	0.063	22.9	71.5/30	12	24
[11]	2µm SABM HBT	1 - 20	7	Not reported	Not reported	42.5/30	---	---
[12]	2µm InGaP/GaAs HBT	0.1 - 6	24 - 13	0.25	Not reported	50/30	---	---
[15]	0.7µm MMIC GaN HEMT	0.2 - 6	12	0.2	25	23/18	5.8	10.9
This work	0.25µm Hybrid GaN HEMT	6.5 - 10.4	10	10	43	12.33/15	3143	1434

TABLE II. Comparison between the fabricated hybrid PA based on the f_T-doubler technique and some broadband PAs with the output power range from 0.6 W to 30 W.

Ref	Technology	BW (GHz)	|S21| (dB)	Pout (W)	PAEmax (%)	GBW (GHz)	FOM(PA)	FOM(PA,BW)
[29]	GaN HEMT	1.5 – 2.4	12	20	56	3.6	511	236
[30]	0.1µm GaAs pHEMT	3.5 - 7	11	0.6	62	12.4	113	75
[31]	0.25µm GaN pHEMT	7 - 17	13.1 – 18.6	5.3 – 6.6	10.2 – 12.3	62	1528	1273
[32]	GaN HEMT	2 – 2.7	10	12.6	48	2.2	334	99.5
[33]	GaN HEMT	2 – 2.9	11.5 – 12.5	12.6	58 - 72	3.6	590	217
[34]	GaN HEMT	8.8 – 9.6	14	6	57	4	4053	352
[35]	0.14µm GaN HEMT	9.9 – 11.5	10.8	9.2	61.1	5.55	6951	1039
[27]	0.25µm Hybrid GaN HEMT	8.8 – 9.8	9.2	30	53	2.88	12652	1360
This work	0.25µm Hybrid GaN HEMT	6.5 - 10.4	10	10	43	12.33	3143	1434

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VI. CONCLUSION

The modified Darlington structure (f_T-doubler), consists of a source degeneration transistor in connection with a grounded transistor, is an efficient way to enhance the frequency response of a microwave circuit. A successful hybrid PA based on the f_T-doubler cell with two 6 W GaN-HEMTs is implemented. The thermal issue of the source degeneration transistor is resolved using a proposed method of assembly. The load/source pulls of the f_T-doubler cell are tuned to achieve the output power of 10W. The input and output matching networks are designed for maximum bandwidth without declining the power gain and the output power. The measured results confirm a bandwidth of 3.9 GHz with the output power of more than 10W and PAE of 43% for the fabricated PA.

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