Received: 21 July 2018 | Revised: 26 November 2018 | Accepted: 4 January 2019

DOI: 10.1002/2050-7038.2836

RESEARCH ARTICLE

WILEY

A new digital control of four-leg inverters in the natural reference frame for renewable energy–based distributed generation

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Summary

Nowadays, stand-alone dispersed generation (DG) supplied from renewable energies is rapidly growing. In such a condition, four-leg inverter can be considered as a successful option to supply unbalanced loads, especially in transformerless systems. In this paper, four-leg inverter is modeled considering the fourth line inductor. The neutral (fourth) line inductor causes a high coupling through control variables in the natural reference frame. To avoid several transformations among reference frames, a new digital controller based on deadbeat (DB) theory is proposed in the natural reference frame to regulate the load voltages under coupled model. The proposed method offers simplicity, ease of digital implementation, and a fast dynamic response. Furthermore, a delay compensation procedure is also proposed to make the overall performance of the proposed DB controller better. Experimental tests based on a 3kW prototype are implemented to support the analytical analysis. Different tests under various single/three-phase, nonlinear/linear, and unbalanced/balanced load conditions were performed, which confirm the excellent performance of the proposed control system.

KEYWORDS

deadbeat (DB) controller, delay compensation procedure, four-leg inverter, renewable energy system

1 | INTRODUCTION

Because of the global concern about CO_2 emission and lack of fossil resources, renewable resources have attracted much attention nowadays. Most of renewable energy sources generate electrical power in two forms of DC or changing frequency AC. To feed AC loads high-quality clean sinusoidal voltages, a power electronic interface is essential to make use of this energy. The renewable energy system can be used in two different ways[1]: (1) stand-alone[2] or (2) grid-connected.[3,4] The main goal in stand-alone renewable energy systems is to supply AC loads with sinusoidal voltages having a stable and constant amplitude and frequency under all operating conditions.

List of symbols and abbreviations: U_{xf}, inverter voltages $a = A, B, C$; U_{xn}, load voltages $x = a, b, c$; i_{Lx}, inductor currents $x = a, b, c$; i_{ox}, load currents $x = a, b, c$; F_{sampling}, sampling frequency; $F_{\text{switching}}$, switching frequency; L, inductor filter of inverter output low-pass filter; C, capacitor filter of inverter output low-pass filter

[Correction added on 06 March 2019, after first online publication: the author's affiliation and e-mail address in Correspondence section have been corrected.].

A typical stand-alone renewable energy feeder is depicted in Figure 1. According to Figure 1, converter (A) usually performs either the maximum power point tracking (MPPT) or AC to DC conversion. One of the differences between stand-alone and grid-connected renewable energy systems is the DC-DC converter (B) and the battery. For the stand-alone case, to ensure the continuous supply of the load, battery storage is essential.

For off-grid operations, mixed nonlinear/linear, unbalanced/balanced, and three/single-phase loads are possible. As a result, the inverter must feed unbalanced loads in which the fourth wire must be provided. To realize it, several configurations have been proposed such as connecting a zigzag or Δ/Y transformer at three-leg inverter outputs[5] and connecting the fourth wire to midpoint of the DC link.[6] However, because of several advantages offered by the four-leg inverter like lower voltage ripple of DC-link, better DC-link utilization, and lower cost and size, it may be considered as the preferred solution in most applications.[7] The schematic of the four-leg inverter is depicted in Figure 2.

As depicted in Figure 2, the three-phase legs are supplied loads using LC filters while just an inductor is used between the fourth leg and load neutral point. This inductor reduces the switching current ripples of the neutral leg, and therefore, the peak current of the power switches. Also, it can reduce the current of phase to neutral short circuit conditions. Having considered the advantages, it concluded that the presence of the fourth leg inductor is practically essential.

The four-leg inverter must prepare sinusoidal three-phase balanced voltages under all circumstances. To this end, several control methods are already proposed in the synchronous reference frame (SRF) with good steady-state performance.[8-12] Among available control techniques in the SRF, the double-loop control offers the best performance by regulating the output voltage d, q, and 0 components via inner current control loops.[8] The inherent d and q components coupling in the SRF make the controller design complicated.[9,10] Besides, the performance of the SRF controller considerably degrades under unbalanced or nonlinear loads.[11]

The model predictive control (MPC) is another control method.[13-15] In this method, the switching frequency is variable, which makes the filter design less effective and more complicated. In addition, the available switching conditions of the four-leg inverter are equal to $2^4 = 16$, so the cost function must be evaluated 16 times within a sampling period,

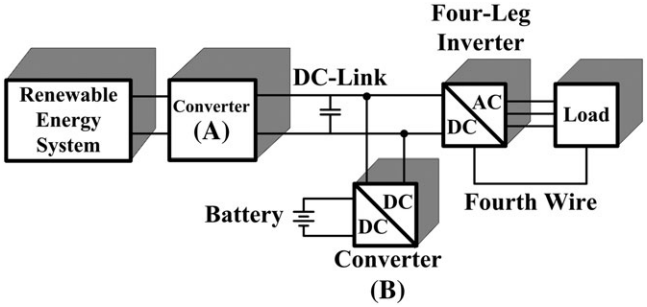


FIGURE 1 The typical stand-alone photovoltaic (PV) generator

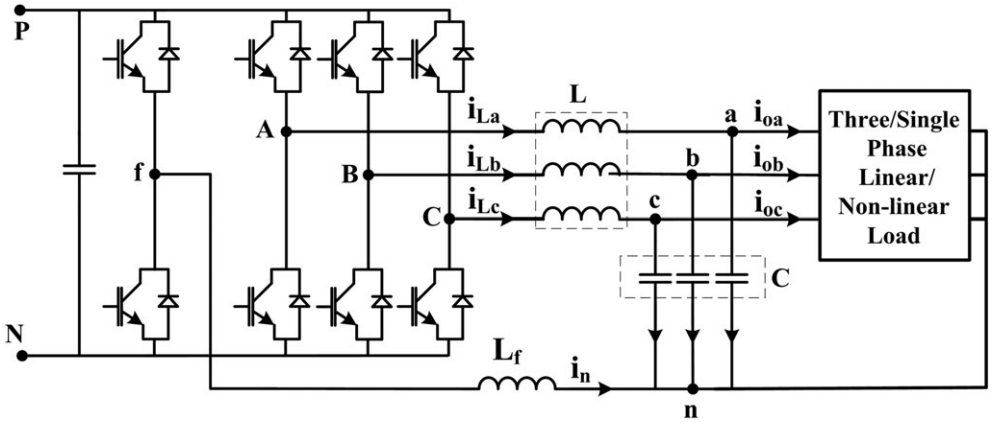


FIGURE 2 The schematic of the four-leg stand-alone inverter

which may not be possible in some applications. Moreover, MPC performance is highly model dependent, which may not be possible because of various practical nonidealities, drifts, and uncertainties of component values.

Control methods in the nonlinear methods classification involve pole-placement method,[16] variable structure method,[17] and sliding mode control (SMC) methods.[18-22] The first two methods provide benefits such as fast transient response, but they suffer from hard parameters tuning, variable switching frequency, sensitivity to model parameters, and nonzero steady-state error. The SMC methods mainly suffer from complexity, changing switching frequency, and chattering issue. Smoothing the control law, constant switching frequency, and lower chattering is achieved in Abrishamifar et al.[18] However, the voltage error especially under nonlinear loads is increased, and the robustness is also decreased. In another solution, three-level hysteresis approach is adopted to decrease the chattering issue,[20] but high-frequency voltage ripple is still evident besides changing switching frequency. In addition, controller design is a hard task in this method where the total harmonic distortion (THD) of the load voltages is also high.

Resonant and repetitive control methods[23,24] can guarantee zero steady-state error. But these methods usually impose high computation burden and memory usage and slow transient response.

The deadbeat (DB) is another model-based control method that is simple and fully compatible with digital platforms and also provides the fastest possible dynamic response.[25-28] However, the inherent delay of digital control systems highly degrades the DB performance. Besides the control strategy, the modeling of the four-leg inverter is important such that it determines the validity and effectiveness of the designed controller parameters. For example, in Yaramasu et al,[13] the fourth leg inductor is not considered, dividing the four-leg converter to three single-phase converters. On the other hand, the fourth leg inductor is almost essential to limit the current rating of switches and reduce harmonics and the electromagnetic interference (EMI).

In this paper, as a base to develop the controller equations, the four-leg inverter is modeled accurately considering the effect of the fourth wire inductor in the natural reference frame. The derived model introduces high coupling among control variables that increases the complexity of the controller design. Therefore, a simple digital controller with low computational burden based on the DB theory is developed under coupled model for the stand-alone four-leg inverter. Unlike conventional methods, the proposed controller considers the mentioned coupling simply with ease of digital implementation and considerably low computational burden. In addition, adopting the natural reference frame for the controller implementation brings the privilege of avoiding multiple transformations among different reference frames and alleviates the need for a phase-locked loop (PLL) in the control system. Furthermore, to overcome the inherent delay of the control method and consequently to improve the control response, a delay compensation algorithm is proposed. The solution improves the quality of the load voltages evidently to meet the international standards without any complex mathematics calculations and operators.

2 | MODEL DESCRIPTION

The averaged switching model of the four-leg inverter in the natural reference frame is depicted as Figure 3.[8]

Based on Figure 3 and using Kirchhoff's voltage law (KVL) in equivalent circuit, the voltage equations can be written as follows[8]:

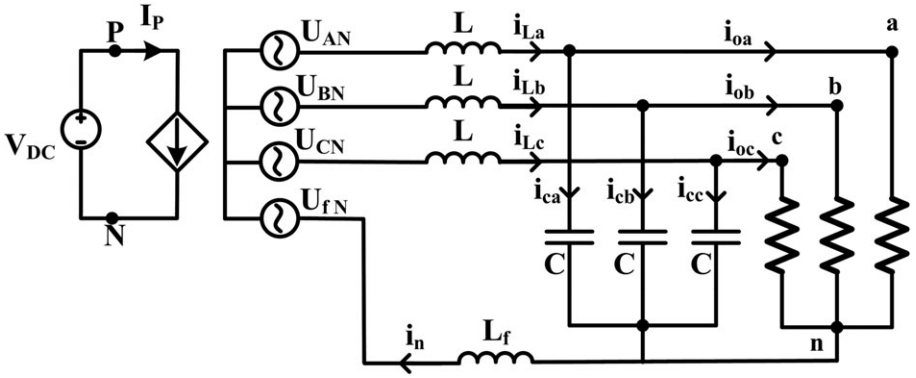


FIGURE 3 The averaged switching model of the four-leg inverter in the natural reference frame

$$\frac{d}{dt}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \frac{L_f}{L}\frac{d}{dt}\begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix} + \frac{1}{L}\begin{bmatrix} U_{Af} \\ U_{Bf} \\ U_{Cf} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix}, \tag{1}$$

where U_{an}, U_{bn}, and U_{cn} are the load voltages; U_{Af}, U_{Bf}, and U_{Cf} are the inverter voltages; and i_{La}, i_{Lb}, and i_{Lc} are the inductors currents. On the other hand, by using the Kirchhoff's current law (KCL) in the load neutral point n, the existing relation between the currents can be expressed as (2).

$$i_{La} + i_{Lb} + i_{Lc} - i_n = 0. \tag{2}$$

Substituting (2) in (1) results in (3), which can be readily rearranged as standard state equation format, shown in (4).

$$\begin{aligned} A\frac{d}{dt}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} &= \frac{1}{L}\begin{bmatrix} U_{Af} \\ U_{Bf} \\ U_{Cf} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} \\ A &= \begin{bmatrix} 1+\frac{L_f}{L} & \frac{L_f}{L} & \frac{L_f}{L} \\ \frac{L_f}{L} & 1+\frac{L_f}{L} & \frac{L_f}{L} \\ \frac{L_f}{L} & \frac{L_f}{L} & 1+\frac{L_f}{L} \end{bmatrix}, \end{aligned} \tag{3}$$

$$\frac{d}{dt}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \frac{1}{L+3L_f}\underbrace{\begin{bmatrix} 1+2\frac{L_f}{L} & -\frac{L_f}{L} & -\frac{L_f}{L} \\ -\frac{L_f}{L} & 1+2\frac{L_f}{L} & -\frac{L_f}{L} \\ -\frac{L_f}{L} & -\frac{L_f}{L} & 1+2\frac{L_f}{L} \end{bmatrix}}_{B}\begin{bmatrix} U_{Af}-U_{an} \\ U_{Bf}-U_{bn} \\ U_{Cf}-U_{cn} \end{bmatrix}. \tag{4}$$

In addition, the output voltage state equations are again obtained by applying the KCL to nodes a, b, and c as

$$\frac{d}{dt}\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix}. \tag{5}$$

Based on (4), since the nondiagonal elements of the matrix B are not zero, the inductor currents are coupled to each other. The nondiagonal elements are proportional to L_f, so the L_f is the reason of the current coupling.

3 | THE PROPOSED DB CONTROLLER

The four-leg inverter model from AC side point of view is depicted as Figure 4.

According to Figure 4, the voltage equation of phase a is given in (6).

$$U_{Af} = L\frac{di_{La}}{dt} + U_{an} + L_f\frac{di_n}{dt}. \tag{6}$$

Applying the KCL to the output and neutral point nodes results in (7) and (8).

$$i_{Ca} = C\frac{dU_{an}}{dt} = i_{La} - i_{Oa}, \tag{7}$$

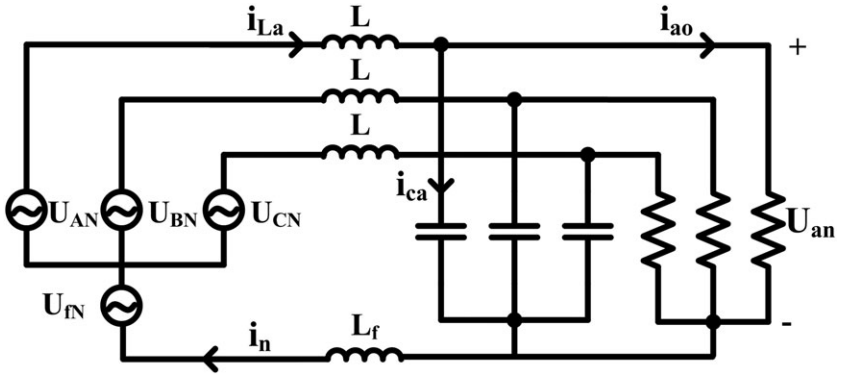


FIGURE 4 The four-leg inverter model from AC side point of view

$$i_n = i_{La} + i_{Lb} + i_{Lc}. \tag{8}$$

These equations form the basic of the proposed DB law. Substituting (8) in (6) results in

$$(L + L_f)\frac{di_{La}}{dt} = U_{Af} - U_{an} - L_f\left(\frac{di_{Lb}}{dt} + \frac{di_{Lc}}{dt}\right). \tag{9}$$

According to (9), time derivatives of the three-phase inductor currents are related to each other. So the equations for each phase cannot be solved independently. However, Equation 7 can be solved for any of the three phases independently.

By rewriting (9) for two other phases, a system of three equations with three unknown parameters is achieved where the unknown parameters are time derivatives of inductors currents:

$$\begin{aligned} W\begin{bmatrix} \frac{di_{La}}{dt} \\ \frac{di_{Lb}}{dt} \\ \frac{di_{Lc}}{dt} \end{bmatrix} &= \frac{1}{L + L_f}\begin{bmatrix} U_{Af} - U_{an} \\ U_{Bf} - U_{bn} \\ U_{Cf} - U_{cn} \end{bmatrix} \\ W &= \begin{bmatrix} 1 & \frac{L_f}{L + L_f} & \frac{L_f}{L + L_f} \\ \frac{L_f}{L + L_f} & 1 & \frac{L_f}{L + L_f} \\ \frac{L_f}{L + L_f} & \frac{L_f}{L + L_f} & 1 \end{bmatrix}. \end{aligned} \tag{10}$$

Assuming the sampling time to be very small and using the backward Euler discretization method, the time derivative can be simply estimated by the difference between two consecutive samples (at instants k and $k + 1$). Hence, (10) can be discretized as follows, in which T_s is the sampling interval:

$$W\begin{bmatrix} i_{La}(k+1) \\ i_{Lb}(k+1) \\ i_{Lc}(k+1) \end{bmatrix} = X\begin{bmatrix} i_{La}(k) \\ i_{Lb}(k) \\ i_{Lc}(k) \end{bmatrix} + \frac{T_s}{L + L_f}\begin{bmatrix} U_{Af}(k) - U_{an}(k) \\ U_{Bf}(k) - U_{bn}(k) \\ V_{Cf}(k) - U_{cn}(k) \end{bmatrix}. \tag{11}$$

In DB with two-sample delay, the target is to calculate the actuating signal at instant $k + 1$ based on the measured variables at instant k. Therefore, the control variables are expected to reach their reference values at the end of $k + 1$ (or equivalently at instant $k + 2$). At this condition and at moment k, all the $k + 1$ values are considered as the reference values. In the four-leg stand-alone inverter, the output or load voltages are the control variables while the inverter voltages are actuating signals. As a result, the final DB control law at instant k has to provide the inverter voltages at instant $k + 1$. To do this, the converter currents at instant $k + 1$ can be estimated from (11) by using a linear approximation ($i_{Lx}(k + 2) = i_{Lx}(k + 1) + [i_{Lx}(k + 1) - i_{Lx}(k)]$), as

$$W\begin{bmatrix} i_{La}(k+1)+(i_{La}(k+1)-i_{La}(k)) \\ i_{Lb}(k+1)+(i_{Lb}(k+1)-i_{Lb}(k)) \\ i_{Lc}(k+1)+(i_{Lc}(k+1)-i_{Lc}(k)) \end{bmatrix} = W\begin{bmatrix} i_{La}(k+1) \\ i_{Lb}(k+1) \\ i_{Lc}(k+1) \end{bmatrix} + \frac{T_s}{L+L_f}\begin{bmatrix} U_{Af}(k+1)-U_{an}(k+1) \\ U_{Bf}(k+1)-U_{bn}(k+1) \\ U_{Cf}(k+1)-U_{cn}(k+1) \end{bmatrix}, \tag{12}$$

which can be simply solved for $U_{xf}(k+1)$:

$$\begin{bmatrix} U_{Af}(k+1) \\ U_{Bf}(k+1) \\ U_{Cf}(k+1) \end{bmatrix} = \begin{bmatrix} U_{an}(k+1) \\ U_{bn}(k+1) \\ U_{cn}(k+1) \end{bmatrix} + \frac{L+L_f}{T_s}X\begin{bmatrix} i_{La}(k+1)-i_{La}(k) \\ i_{Lb}(k+1)-i_{Lb}(k) \\ i_{Lc}(k+1)-i_{Lc}(k) \end{bmatrix}. \tag{13}$$

Putting values at moment $k+1$ with their references at current moment k, Equation 13 becomes

$$\begin{bmatrix} U^*_{Af}(k) \\ U^*_{Bf}(k) \\ U^*_{Cf}(k) \end{bmatrix} = \begin{bmatrix} U^*_{an}(k) \\ U^*_{bn}(k) \\ U^*_{cn}(k) \end{bmatrix} + \frac{1}{T_s}\begin{bmatrix} L+L_f & L_f & L_f \\ L_f & L+L_f & L_f \\ L_f & L_f & L+L_f \end{bmatrix}\begin{bmatrix} i^*_{La}(k)-i_{La}(k) \\ i^*_{Lb}(k)-i_{Lb}(k) \\ i^*_{Lc}(k)-i_{Lc}(k) \end{bmatrix}. \tag{14}$$

Evidently, to compute the reference voltages of the inverter, the load voltages and the inductor currents' references are required. Although voltage reference values of the load are already decided with human operator, reference values of the inductors' currents are not determined yet. The currents can be calculated from the other state equation set of (7). It should be noted that (7) is written for phase a, but since it is decoupled for each phase, the same procedure can be employed for two other phases. So (7) can be converted to discrete form as follows:

$$\frac{U_{an}(k+1)-U_{an}(k)}{T_s} = \frac{1}{C}(i_{La}(k)-i_{Oa}(k)). \tag{15}$$

Based on (15), $i_{La}(k)$ is calculated as

$$i_{La}(k) = i_{Oa}(k) + \frac{C_a}{T_s}[U_{an}(k+1)-U_{an}(k)]. \tag{16}$$

As mentioned before, in DB with two-sample delay, the $k+1$ samples are considered as references. Therefore, to calculate the inductor current reference values, (16) must be updated for the next sample as follows:

$$i_{La}(k+1) = i_{Oa}(k+1) + \frac{C_a}{T_s}[U_{an}(k+2)-U_{an}(k+1)]. \tag{17}$$

Because of small sampling time, again, the linear approximation can be used for $U_{an}(k+2)$. Also, the load current variation can be neglected at this condition, and consequently, two consecutive samples can be assumed the same as given in (18).

$$i_{La}(k+1) = i_{Oa}(k) + \frac{C_a}{T_s}[(U_{an}(k+1) \quad + [U_{an}(k+1) - U_{an}(k)]) - U_{an}(k+1)]. \tag{18}$$

Consequently, doing some simplifications and replacing the $k + 1$ samples with reference ones result in (19).

$$i^*_{La}(k) = i_{Oa}(k) + \frac{C}{T_s}\left(U^*_{an}(k) - U_{an}(k)\right). \tag{19}$$

Reference inductor currents are given in (20), which are then replaced in (14) to give the final inverter reference voltages.

$$\begin{bmatrix} i^*_{La}(k) \\ i^*_{Lb}(k) \\ i^*_{Lc}(k) \end{bmatrix} = \begin{bmatrix} i_{Oa}(k) \\ i_{Ob}(k) \\ i_{Oc}(k) \end{bmatrix} + \frac{C}{T_s}\begin{bmatrix} U^*_{an}(k) - U_{an}(k) \\ U^*_{bn}(k) - U_{bn}(k) \\ U^*_{cn}(k) - U_{cn}(k) \end{bmatrix}. \tag{20}$$

As previously discussed, the fourth leg inductor creates a coupling among inductor currents, which is clear in (14). Since the proposed controller equations include only some basic algebraic operations, it offers considerable simplicity compared with other methods. In addition, it does not need several transformations among reference frames, which results in very low computational burden as well as ease of digital implementation. Also, it is not required to optimize any cost functions as the MPC technique. Compared with SRF control methods, the proposed DB controller does not need any PLL or transformations among reference frames.

It is worth mentioning that the DB controller dynamics can be considered as only two pure sampling period delays. In other words, the DB controller places all the closed-loop system poles at the origin of the z-plane and consequently inside the unit circle, which ensures the stability of the control scheme. In the real condition, if the model of the system is accurate, the stability of the whole system will be guaranteed. In practice, the main issues that challenge the stability are model mismatches and parameter uncertainties. The effect of these two problems, under severe conditions, will be investigated in Section 4 to confirm the stability over a wide range of possible mismatches and uncertainties.

4 | DELAY COMPENSATION PROCEDURE

There are several delays relevant to the digital implementation of the control systems mainly originated from the analog to digital conversion, algorithm execution, and the pulse-width modulation (PWM) update time. In most cases, the overall delay time equals to a sampling period. This delay may highly deteriorate the dynamic stability and the control performance. To avoid these problems, some kind of delay compensation should be employed.[29-31] In the proposed DB controller, the measured and reference values at instant k are used to generate the actuating or switching signals, which are applied at instant $k + 1$. If the inputs to the control equations at instant $k + 1$ are available at instant k, then the switching signals can be calculated and prepared for the instant $k + 1$. Consequently, the whole delay time of the DB controller decreases from two to one sampling period. This reduction not only improves the control performance but also increases the stability margin of the control system.

According to (14) and (20), the measured and reference load voltages as well as the load and inductor currents are used in the DB controller. Hence, to compensate the delay time, these values should be predicted one sample ahead.

According to (11), the inductor currents can be predicted for instant $k + 1$ according to the current values. Also, using (16), the load voltages can be predicted for instant $k + 1$. It is worth mentioning that these two equations are based on the system equations that guarantee the prediction accuracy.

However, still, load currents as well as reference load voltages at instant $k + 1$ are required, for which the prediction can be done based on the present and previous values using the fourth-order Lagrange extrapolation.[32-34] This extrapolation is valid for an extend frequency domain of the reference load voltages and currents and is given in (21) and (22) for phase a.

$$\begin{aligned} U^*_{an}(k+1) = {} & 4U^*_{an}(k) - 6U^*_{an}(k-1) + 4U^*_{an}(k-2) \\ & - U^*_{an}(k-3), \end{aligned} \tag{21}$$

$$i_{Oa}(k+1) = 4i_{Oa}(k) - 6i_{Oa}(k-1) + 4i_{Oa}(k-2) - i_{Oa}(k-3). \quad (22)$$

The complete schematic of the proposed DB controller with the delay compensation procedure is depicted in Figure 5.

5 | SIMULATION AND EXPERIMENTAL RESULTS

To validate the excellent performance of the proposed controller, an experimental test bench as Figure 2 is implemented as shown in Figure 6. The inverter is fed from constant DC voltage obtaining from diode rectifier fed from an autotransformer. Hall effect current and voltage sensors are utilized to sample the control input variables. The control system is implemented using a TMS320f28335 digital signal processor from Texas Instruments. The system parameters are summarized in Table 1.

Usually, three kinds of filters including L, LC, and LCL filters are used to damp and remove the high-frequency voltage and current harmonics in power converters. The L filter is more common for grid-connected converters in which the injected current harmonics must be mitigated.[35] On the other hand, LCL filters can be used for both grid-connected and stand-alone converters, but this filter is commonly used for high power application to reduce the size of the filter inductor.[35] Therefore, for low and medium stand-alone converters, an LC filter is commonly used to attenuate both high-frequency voltage and current ripples. To make the switching ripples lower than 1%, the cutoff frequency of the

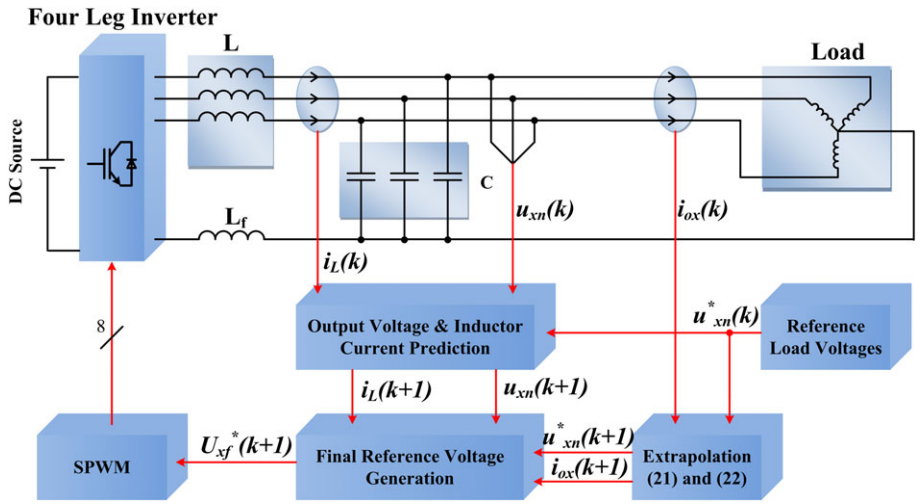


FIGURE 5 The schematic of the proposed control system. SPWM, sinusoidal pulse-width modulation

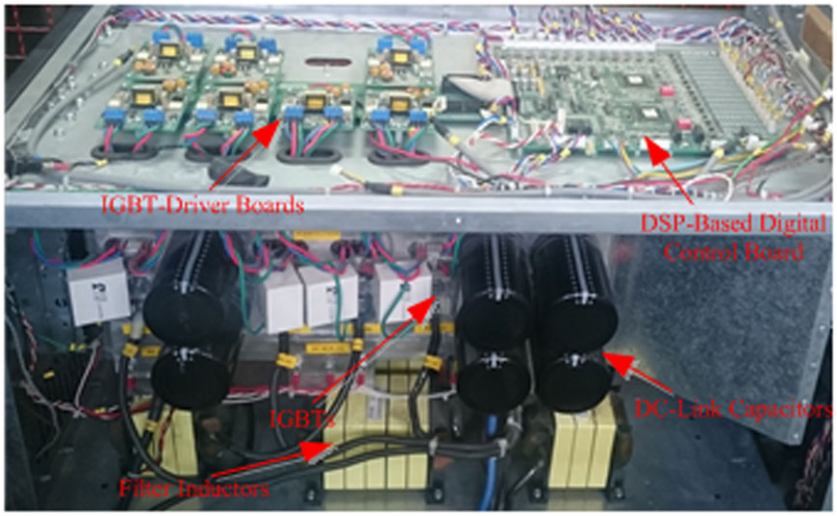


FIGURE 6 The photograph of the experimental setup

TABLE 1 The parameters of the experimental setup

Rated power	P_o	3 kVA
Output voltage (phase to neutral)	V_{xn}	110 V (rms)
Frequency	f_0	60 Hz
Filter inductor	L	880 μH
Fourth leg inductor	L_f	440 μH
Filter capacitor	C	33 μF
Sampling frequency	F_{sampling}	12 kHz
Switching frequency	$F_{\text{switching}}$	12 kHz
DC-link voltage	V_{DC}	390

LC filter is set to 10% of the switching frequency.[36,37] Besides, the current ripple of the each phase inductor at the worst case is determined as follows:

$$Inductor \quad Current \quad Ripple = \frac{VDC}{2*L*F_{sw}}|D|*(1-|D|). \tag{23}$$

In (23), D is the line to neutral duty ratio. According to the maximum allowable current ripple, the value of L is selected from (23). Afterward, based on the reactive power limit (about 5% of the rated converter power) and the

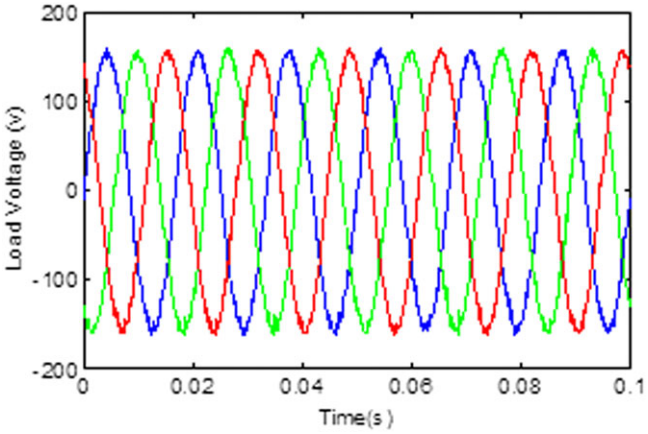


FIGURE 7 Simulation results under no-load condition

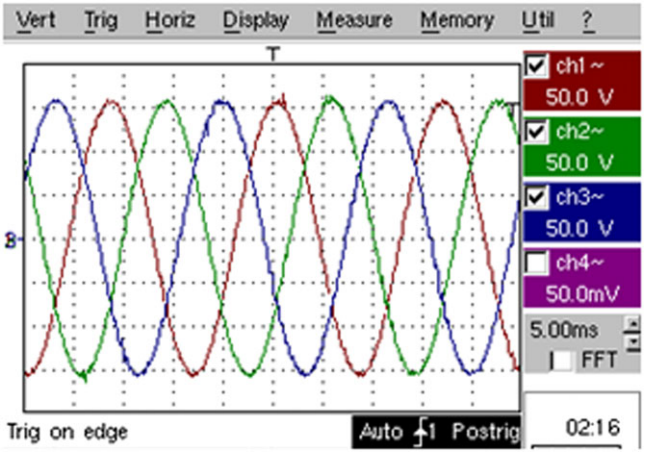
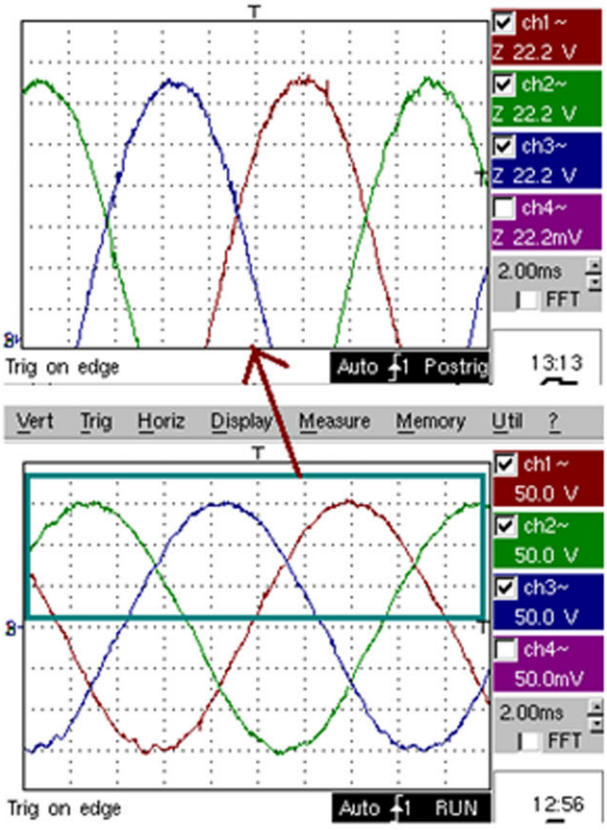
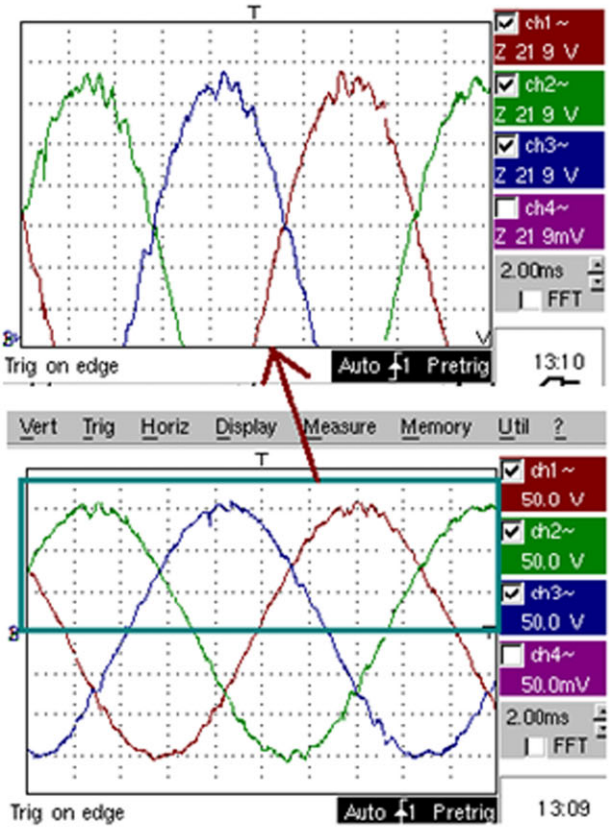


FIGURE 8 No-load experimental results: ch1-ch3, output voltages (50 V/div)



(A)



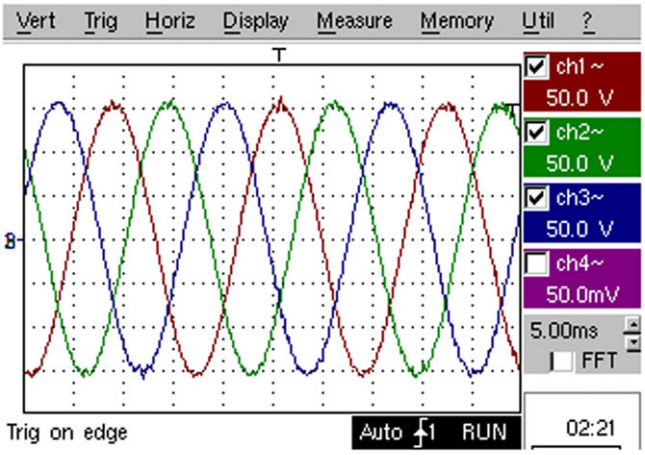
(B)

FIGURE 9 The effect of delay compensation: A, with and B, without delay compensation

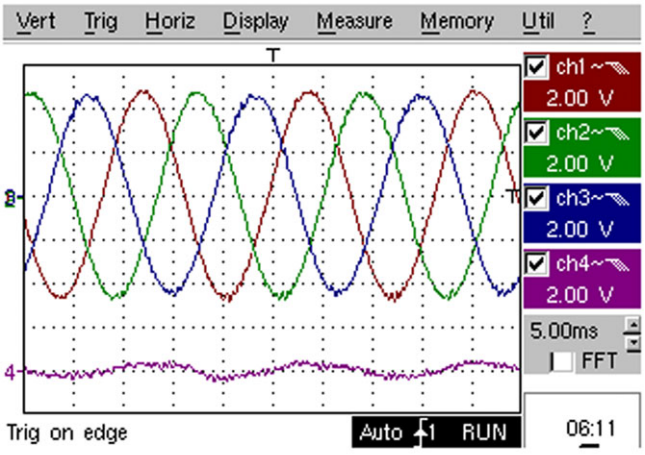
resonant frequency, the proper value of C will be calculated. To have the lowest THD for the load voltages, the neutral inductor (L_n) is selected as half of the three-phase inductors (L).[38]

It is beneficial that the sampling process should proceed at a very high frequency, so high that the spectrum of the sampled signal might be considered negligible at the Nyquist frequency, even if a significant ripple is observable. However, hardware limitation related to the digital signal processor (DSPs) or microcontrollers-based implementations with limited sampling frequency do not allow the sampling frequency too high. In addition, in single update mode of operation of the digital PWM, the sampling frequency is beneficial to be equal to the switching frequency. Otherwise, the sampled inputs do not affect the actuators (duty cycle of PWMs). In addition, according to the Nyquist theorem, the sampling rate must be at least $2f_{\max}$ or twice the highest analog frequency component.[39] So, in the tested stand-alone inverter with proposed controllers, the maximum analog frequency is 60 Hz. Therefore, the Nyquist frequency limitation is 120 Hz where the sampling frequency is far from this value (12 kHz). It is worth to be mentioned that sinusoidal PWM (SPWM) is adopted to generate the switching signals since it offers a simple structure as well as low harmonic profile of the load voltage.[40] First, no load simulation and experimental results are presented in Figures 7 and 8, respectively. Clearly, inverter provides three-phase balanced sinusoidal voltages for the load where the THD% of the load voltages is about 1% and 1.1% in simulation and experimental results, respectively. Thus, the simulation results are validated by the experimental results.

The delay compensation improves the output voltage quality, especially at peak and valley of voltage waveforms.[14] The zoomed peak voltages with and without the delay compensation are shown in Figure 9.



(A)



(B)

FIGURE 10 Experimental results of inverter loading with balanced linear three-phase load: A, ch1-ch3, load voltages (50 V/div) and B, ch1-ch3, load currents, and ch4, neutral current (6 A/div)

It is evident that the voltage ripple is more without the delay compensation, which increases the THD% of the load voltage to 2.2%.

In another study, the inverter is loaded with linear three-phase load with the results shown in Figure 10. The THD of the output voltage is 1.4% at this condition. It is worth mentioning that according to the IEC62040-3, which is an international standard related to stand-alone inverters, the maximum permitted THD% is 5% under linear load. Thus, it is evident that the proposed method not only satisfies an international standard but also, the THD value is far from standard limitation. Because of balanced load, the current of the fourth wire is close to zero; however, a small ripple current is still present. This is mainly because of the low percentage of the unbalanced load, which is evident in three-phase load currents.

A four-leg inverter should be able to handle unbalanced loads. To examine the converter performance under this condition, a single-phase linear load is supplied with experimental results shown in Figure 11. Evidently, the phase and neutral currents are the same (just phase shifted by 180°), and the inverter supplies the single-phase load with fully balanced voltages with a THD% less than 1.5%. This confirms that highly unbalanced loading does not affect the four-leg inverter performance.

The converter performance under a highly nonlinear load is also examined. Accordingly, three bridge diode rectifiers feeding parallel RC loads are connected to each output phase. The load parameters are selected to supply 70% of the rated apparent power. The load current and voltage waveforms are given in Figure 12. While the THD and crest factor (CF) of the load current are 124.5% and 3:1, the THD of the load voltage is 3.6%. Based on IEC62040-3 international standard, the THD% of the load voltages is not allowed to exceed 8% under nonlinear load. Also, the third, fifth,

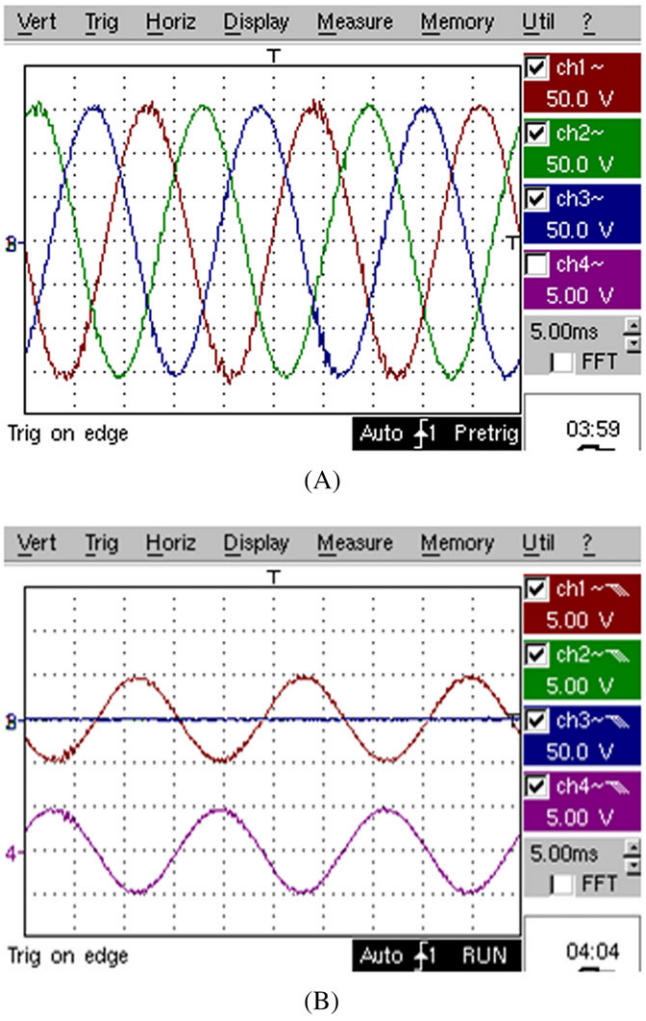
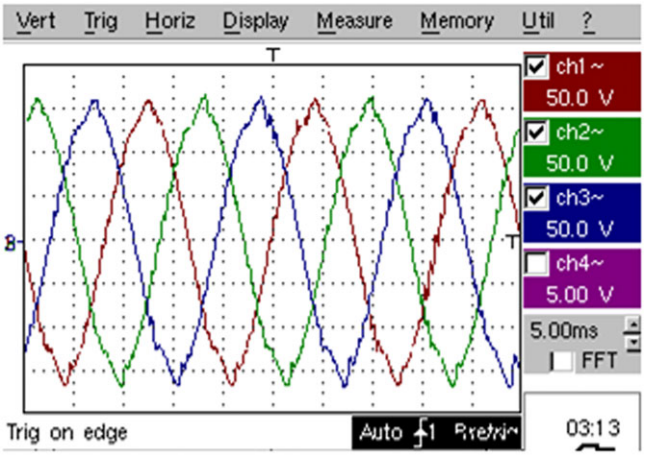
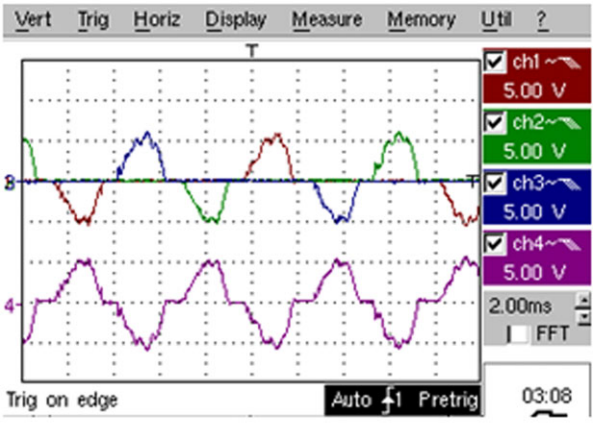


FIGURE 11 Experimental results of inverter loading with linear single-phase load: A, ch1-ch3, load voltages (50 V/div) and B, ch1-ch3, load currents, and ch4, neutral current (14 A/div)



(A)



(B)

FIGURE 12 Experimental results of inverter loading with nonlinear loads: A, ch1-ch3, load voltages (50 V/div) and B, ch1-ch3, load currents, and ch4, neutral current (14 A/div)

and seventh harmonics components are not permitted to be higher than 5%, 6%, and 5%, respectively. Again, the proposed method satisfies international standard limitation under nonlinear loads. According to Figure 12, the current of the fourth wire is not zero, which implies that the load current involves zero sequence components.

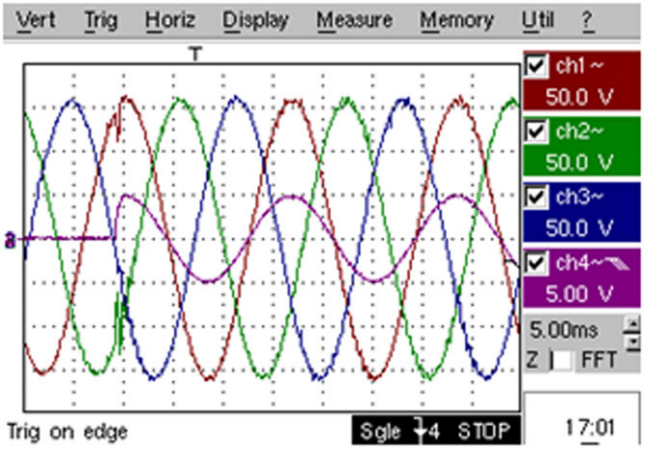


FIGURE 13 Experimental results of the inverter under 100% step load variation: ch1-ch3, load voltages (50 V/div) and ch4, load current "phase *a*" (14 A/div)

For the next test, inverter is tested under 100% step load variations where the results are presented in Figure 13. Evidently, the controller shows a fast and smooth dynamic response, where the load voltage experiences a 15% dip with negligible oscillations, which is eliminated in less than 1.5 milliseconds.

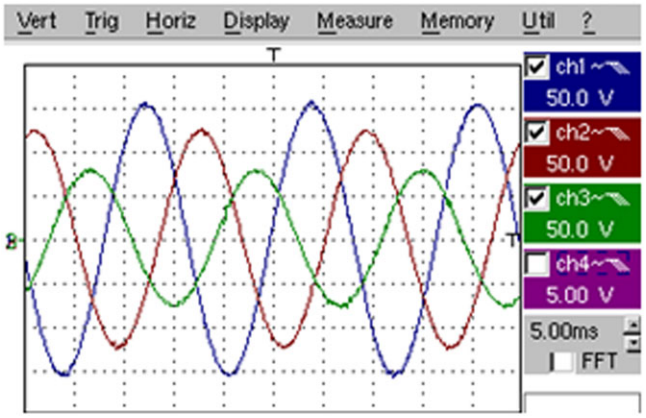
As already stated, the controller equations are dependent to the model of the system, so the performance is inherently affected by the model and parameter mismatches. Usually, filter elements may be susceptible to mismatches because of uncertainties and parameters drift. Hence, the performance of the control system from steady-state amplitude error (e_v) and THD% of the load voltage is investigated in response to filter parameter mismatches. The results are presented in Table 2. Accordingly, it is confirmed that the controller is robust against parameter mismatches in which large deviations from real values do not affect the controller performance considerably.

Voltage stabilizer (VS) or, in other words, dynamic voltage restorer (DVR) is one of the best customer power devices to reduce or eliminate voltage variation in power distribution network and consequently improves the power quality. For this purpose, the VS is used in series connection with the network using a boost transformer. The VS must generate

TABLE 2 Analysis of the proposed method robustness against model mismatches via experimental results

		ΔC, μF							ΔL_f, μH						
		−18	−13	−8	−3	0	+2	+4	−240	−140	−40	0	+60	+160	+260
THD, %	No load	1.8	1.4	1.3	1.15	1.1	1.1	1.2	1	1	1.1	1.1	1.1	1.2	1.3
	Full load	2.1	1.9	1.6	1.5	1.4	1.6	1.8	1.4	1.4	1.4	1.4	1.5	1.5	1.6
e_v, %	No load	1.1	0.7	0.4	0.1	0	0	0.3	0	0	0	0	0	0	0
	Full load	3.5	2.5	2.1	2.2	2	2	2	1.8	1.8	1.85	2	2.1	2.2	2.4

Abbreviation: THD, total harmonic distortion.



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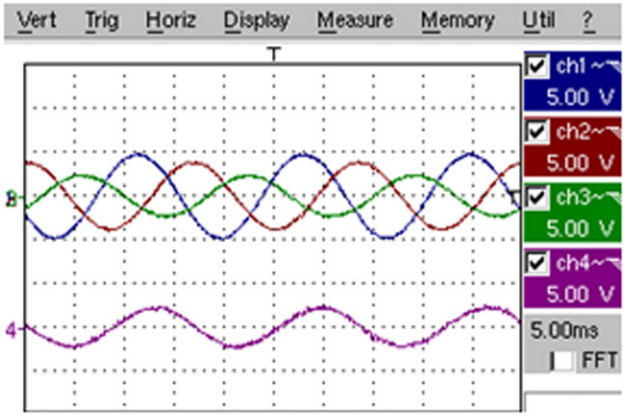
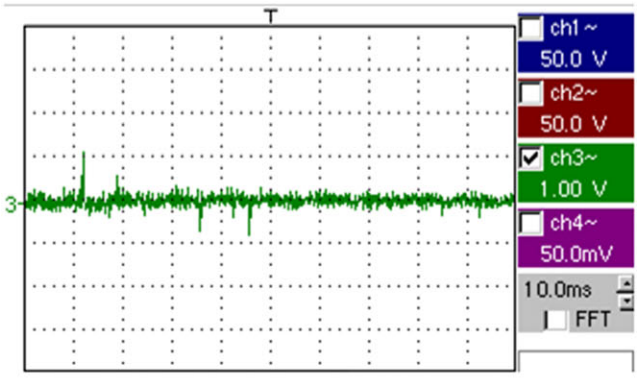


(B)

FIGURE 14 The experimental results of the inverter under unbalanced reference voltages: A, load voltages, ch1-ch3 (50 V/div) and B, load currents, ch1-ch4 (13 A/div)



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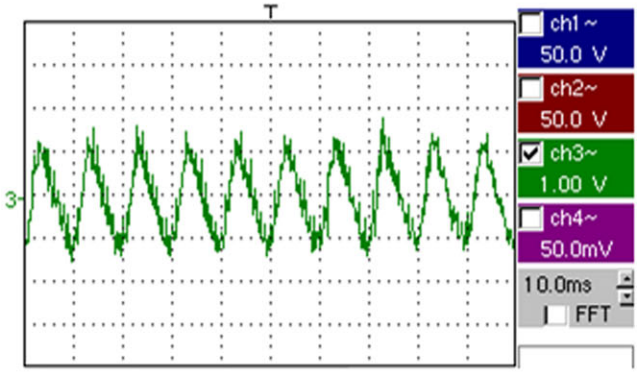

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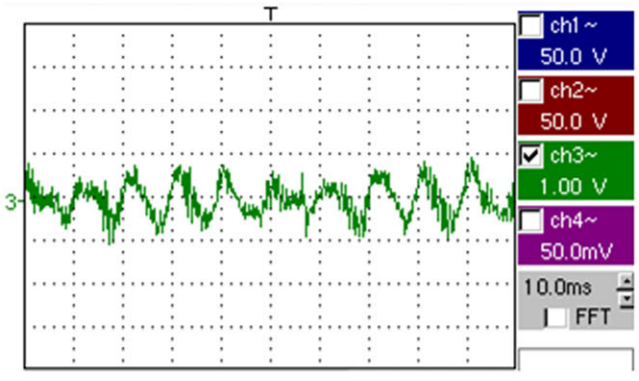
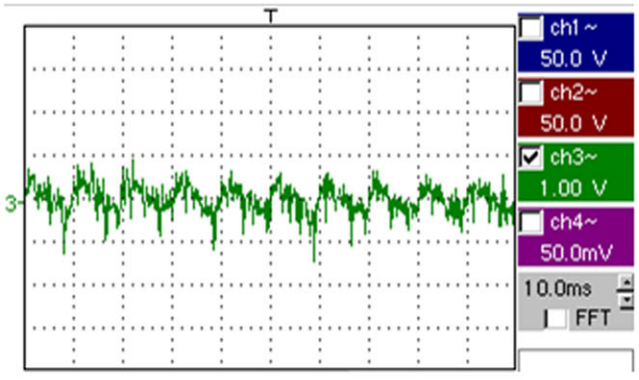


(C)



(D)

FIGURE 15 The ripple of the input DC-link voltage for A, no load, B, full linear load, C, single-phase linear load, and D, nonlinear load

a controlled voltage in order to supply the load with fixed voltages. The most important task is the injection task when the voltage sag happens and the VS is responsible to minimize the voltage sag. Usually, balanced voltage sag happens in three-phase systems, which means equal voltage sag for all three phases. However, for three-phase VS applications, sometimes, because of unbalanced loading or other conditions, unbalanced voltage sag happens. As a result, the VS must generate controlled unbalanced voltages to supply loads with fixed and equal voltage amplitudes. In addition, in stand-alone renewable energy–based distributed generation, sometimes, different loads may need different voltages. All of these verify the need of generating three-phase voltages without balanced values. Four-leg inverter can handle this condition precisely and simply, which verifies one of the excellent advantages of this inverter. As a result, the experimental results of proposed method with different reference voltages are shown in Figure 14. As evidently shown, it confirms that the three-phase unbalanced voltages can be generated, which makes the four-leg inverter as a proper solution for VS applications.

As mentioned before, in split DC-link four-wire inverter, the fourth wire is connected to the midpoint of the DC link to provide a path for neutral current. Since the neutral current flows through DC-link capacitors especially under unbalanced and nonlinear loading conditions, not only high capacitance values are needed to maintain the voltage ripple in standard range but also, the voltage balancing algorithm must be added to the control system to balance the DC voltage, which imposes two additional voltage sensors itself. However, in the four-leg inverter, the fourth wire is connected to the fourth leg, which decouples the neutral current from DC link. Accordingly, the neutral current flows through the phase's leg and fourth leg without any effect on the DC-link capacitors. Therefore, it can be concluded that the required DC-link capacitance is significantly lower than the split DC-link structure. To verify this, the ripple of the input DC-link voltage for four different conditions is shown in Figure 15.

As evidently appeared, the voltage ripple is too small in all conditions. For the unbalanced condition (even single-phase loading), since the fourth leg provides a path for the neutral current flow, the DC-link voltage ripple does not alter considerably. It is one of the advantages of the four-leg inverter compared with the conventional split DC-link four-wire inverter.

To make a good comparison, the proposed method is compared with three other methods through different parameters as tabulated in Table 3. As already evident in Table 3, the proposed method provides lower or equal steady-state amplitude error (e_v) compared with other methods. Besides, although the performance under nonlinear loads is equal or a little lower, the sampling and switching frequency of the proposed method are much lower than other methods. It is worth mentioning that the performance of the controller is highly related to the sampling and switching frequency. To sum up, the proposed method provides equal or higher performance compared with other methods even under lower sampling and switching frequency.

TABLE 3 The experimental performance investigation under model parameter mismatches

Reference	Proposed Method	Yaramasu et al[14]	Abrishamifar et al[18]	Darvishzadeh et al[41]
V_{DC}	390	350	350	275
V_0(rms)	110	120	220	120
S_{out}, kVA	3	-	6	-
Number of phases	3	3	1	1
Filter inductor, μH	880	2.5	357	250
Filter capacitor, μF	33	60	9.4	100
$F_{switching}$, kHz	12	Variable	15	13.42 (average)
$F_{sampling}$, kHz	12	20	15	-
THD% (nonlinear load)	3.6	3.5	1.7	3.4
THD% (linear load)	1.4	2.8	1.1	-
e_v%	2	5.4	-	2
Robustness	Very high	High	High	Very high
Transient response	Very fast	Fast	Very fast	Very fast

Abbreviation: THD, total harmonic distortion.

6 | CONCLUSION

The four-leg inverter is modeled in the natural reference frame considering that the inductor of the fourth wire was presented. It was confirmed that this inductor imposes an inductor current coupling in different phases. The mathematical model was discretized, and the proposed DB control law was derived. The DB equations consist of some simple algebraic operations. By predicting converter variables for the next sampling period, time delay of the proposed DB control decreased from two to one sampling period, which improves the overall control performance. At linear single/three-phase load conditions, the controller guarantees the THD value under 1.5%. Also, the performance under a highly nonlinear load is far from international standards limitations where THD% is about 3.7%. Besides, in response to a wide range of uncertainties for the output filter parameters, the controller maintained its normal performance.

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How to cite this article: Pichan M, Rastegar H, Monfared M. A new digital control of four-leg inverters in the natural reference frame for renewable energy–based distributed generation. *Int Trans Electr Energ Syst*. 2019;29: e2836. https://doi.org/10.1002/2050-7038.2836