Ferdowsi Rectifiers—Single-Phase Buck-Boost Bridgeless PFC Rectifiers With Low Semiconductor Count

Saeed Sharifi, Mohammad Monfared, *Senior Member, IEEE*, and Mohammad Babaei

***Abstract*—Two new power factor correction (PFC) rectifiers with the voltage buck-boost capability are proposed in this article, called as Ferdowsi rectifiers (FRs). The proposed rectifiers employ a reduced number of semiconductors compared to the competitors. Also, since the reverse recovery problem of antiparallel diodes of transistor switches is avoided, then MOSFETs can be readily utilized, which lets much higher switching frequencies and lower size of passive components. In addition, two parallel capacitors provide a path for the input current during the discharge mode of the buck-boost inductors to improve the current quality. The discontinuous conduction mode operation of the proposed rectifiers guarantees a high quality input current with a low total harmonic distortion. All aforementioned features offer a highly efficient operation and at the same time a purely sinusoidal current drawn from the ac source compared to the previous well-developed competitors. The validation of the theoretical achievements is performed by extensive tests on a laboratory test rig.**

***Index Terms*—Buck-boost, Ferdowsi rectifier (FR), high efficiency, power factor correction (PFC).**

I. Introduction

THE rectifiers are widely utilized from home appliances to industrial facilities, such as telecom and uninterruptable power supplies, adaptors, light-emitting diodes (LEDs) and motor drivers [1]–[5]. The conventional diode-bridge rectifier is usually followed by a dc–dc stage to shape the input current waveform, known as the power factor correction (PFC) circuit. The most well-known bridge-based PFC rectifier is formed from the boost-type dc–dc circuit [5]. However, this type of PFC rectifier lacks to provide a dc voltage lower than the source peak voltage, which is required in many applications [1], [6]. In contrast, the buck-type PFC rectifier offers the possibility of voltage step-down. It lacks a pure sinusoidal input current due to appearance of the dead zones within its waveform when the instantaneous input voltage is below the output dc voltage [7]–[9]. As a following approach to improve the input current quality of the buck-type PFC rectifiers, some other researches tried to employ an auxiliary converter, which operates during the dead zones of the input current instead of the main converter. These auxiliary converters are mainly based on the buck-boost and flyback converters, which successfully improve the power factor [9], [10]. However, the aforementioned techniques incur a recognizable distortion on the input current waveform at the instant of changing the operating converter. In addition, many components are needed for these rectifiers leading to a low efficiency and a high cost. Therefore, these rectifiers cannot be applicable in those applications, where the buck-boost capability and the high-quality input current are of main interest. Unfortunately, the buck-boost-type rectifiers also need an additional input *LC* filter to reduce the total harmonic distortion (THD) and improve the PF of the current drawn from the input ac source [11]–[14]. In addition to these circuits, the application of the well-known Cuk and Sepic converters are widely discussed as the PFC rectifiers, which inherently offer voltage buck-boost capability and a continuous input current waveform [15]–[20] at the cost of a high number of passive components. As an overall conclusion, the aforementioned topologies mainly suffer from a high number of components, comparably high power losses and a low input current quality, which higher costs and increased converter volume are incurred to solve these issues, respectively.

In this article, two types of novel bridgeless PFC buck-boost rectifiers are introduced, called as Ferdowsi rectifiers (FRs), which offer high quality sinusoidal ac input current with a close-to-unity PF. The proposed FRs employ a low number of semiconductors and integrate the magnetic elements to reduce the total size and volume of the converter. Also, they operate under discontinuous conduction mode (DCM) to benefit from the reduced power loss at the switch turn ON and the diode turn-OFF transitions and at the same time, the simple single-loop output voltage control plant without the need for additional sensors [9], [15]. In addition, utilizing the MOSFETs lets increase the switching frequency to reduce the passive components size. Moreover, the continuous half cycle conduction of its inherent body diode provides a continuous low frequency (LF) current path between the input source and the output load without any concern of abrupt current changes and the reverse recovery problem. Considering the aforementioned features along with the ability to operate with the maximum of two semiconductors conducting during any operation mode, the highly efficient

Manuscript received August 4, 2019; revised October 8, 2019; accepted November 4, 2019. Date of publication December 5, 2019; date of current version July 14, 2020. *(Corresponding author: Mohammad Monfared.)*

The authors are with the Department of Electrical Engineering Faculty of Engineering, Ferdowsi University of Mashhad, Mashhad 91779-48974, Iran (e-mail: saeed.sharifi@mail.um.ac.ir; m.monfared@um.ac.ir; mohammad.babaei@mail.um.ac.ir).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2019.2955430

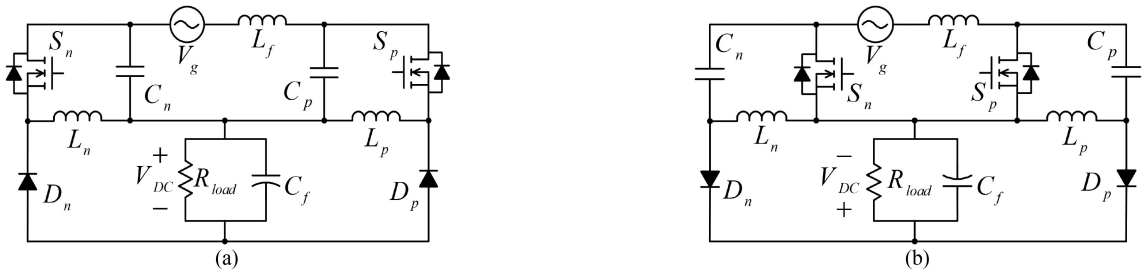

Fig. 1. Proposed FRs. (a) Type I. (b) Type II.

operation of the proposed FRs is guaranteed. As a clear contribution, it can be claimed that the proposed FRs offer highly sinusoidal input current with a low THD and a close-to-unity PF compared to the Cuk and the Sepic-based rectifiers of [15]–[20] while they can also provide higher efficiencies than the buck-boost-type rectifiers of [13], [14]. Moreover, the buck-boost-type rectifiers of [11]–[14] need an ac input filter capacitor unlike the proposed ones, which does not require any extra input filter capacitors. Therefore, both proposed FRs can be employed instead of the conventional PFC rectifiers in a variety of applications, such as LED drives, lamp ballasts, motor drives, telecom power supplies, battery chargers, and wind energy systems. In order to verify the aforementioned theoretical advantages of the proposed FRs, a 300 W buck-operated prototype setup is implemented in the laboratory to feed a dc load with 48 $V_{\rm dc}$ from an input ac source of 110 $V_{\rm rms}$/60 Hz. All discussed features of the proposed rectifiers are confirmed by extensive experiments on this prototype. It is worth mentioning that both proposed FRs offer superior performance when higher output voltages are of interest. Since most papers in the filed mainly focused on the buck operation rather than the boost, then only the buck operation with output voltage of 48 $V_{\rm dc}$ is investigated in this article.

II. Proposed FRs

A. Circuit Configuration

The circuit configurations of the proposed FRs types I and II, are depicted in Fig. 1, which are mainly inspired from the well-known converters of [21], [22]. As seen from this figure, both types benefit from two high frequency (HF) switched MOSFETs, S_p and S_n, two HF diodes, D_p and D_n, two inductors, L_p and L_n, and two capacitors, C_p and C_n. In addition, one input inductor and one output capacitor are also required for current and voltage smoothing, respectively. The elements with a p (n) subscript operate only during the positive (negative) ac half cycle. The same happens for L_p and L_n, thus, they can readily share a common magnetic core to reduce the overall size and cost as in [23]–[25]. Both proposed FRs produce a highly sinusoidal input current waveform with the help of two capacitors C_p and C_n, which provide a path for the input current to flow through during the discharge mode of the inductors. Therefore, one can employ a small input filter inductor, which is more evident for the FR type I. It is worth mentioning that a LF current path is always available between the load and the source by the body diodes of the MOSFETs S_p and S_n for both FR types. For both circuits and during the positive (negative) half cycle a continuous half cycle current flows through the body diode of MOSFET S_n (S_p) that means no reverse recovery problem. Moreover, employing MOSFET switches lets highly increase the switching frequency to reduce the components size without the concern of high power losses. Also, the MOSFETs common source configuration connected to the output negative-polarity is provided by the FR type II, which highly simplifies the control and gating of the MOSFETs. Finally, the common cathode or anode connection of the diodes D_p and D_n lets employ dual diode packages to reduce the size of both FRs.

B. Performance

The performance principles of both FRs are presented in the following, according to the equivalent circuits during the positive half cycle of the input voltage shown in Fig. 2 and the expected current waveforms presented in Fig. 3. The operation modes are analyzed with assuming a same pulsewidth modulated gating signal goes to both MOSFETs S_p and S_n simultaneously, which simplifies the control and means that there is no need to determine the zero crossings of the input voltage waveform.

1) Mode I (0∼DTs):

a) Proposed FR Type I: The equivalent circuit of mode I of the FR type I is depicted in Fig. 2(a) in which the MOSFET S_p turns ON to charge L_p from the input voltage and the capacitor C_p. According to Figs. 2(a) and (3), with assuming the peak values, one can write

$$\begin{cases} V_{Lp}^{\text{type}-I} = V_{Cp}^{\max} = V_{g-(pk)} \\ I_{Lp(\text{type}-I)}^{\max} = I_{Cp} + I_{g-(pk)} \end{cases} \tag{1}$$

where $V_{g-(pk)}$, $I_{g-(pk)}$ and I_{Cp} are the maximum values of input voltage, input current and the capacitor C_p current, respectively.

b) Proposed FR Type II: The operation mode I of the proposed FR type II is also depicted in Fig. 2(d). The voltage across L_p is the same as (1) while its current must be rewritten as

$$I_{Lp(\text{type}-II)}^{\max} = I_{Cp}. \tag{2}$$

Comparing Fig. 2(a) and (d), the input current of the proposed FR type II only flows through the body diode of S_n while it goes through L_n of the proposed FR type I as well.

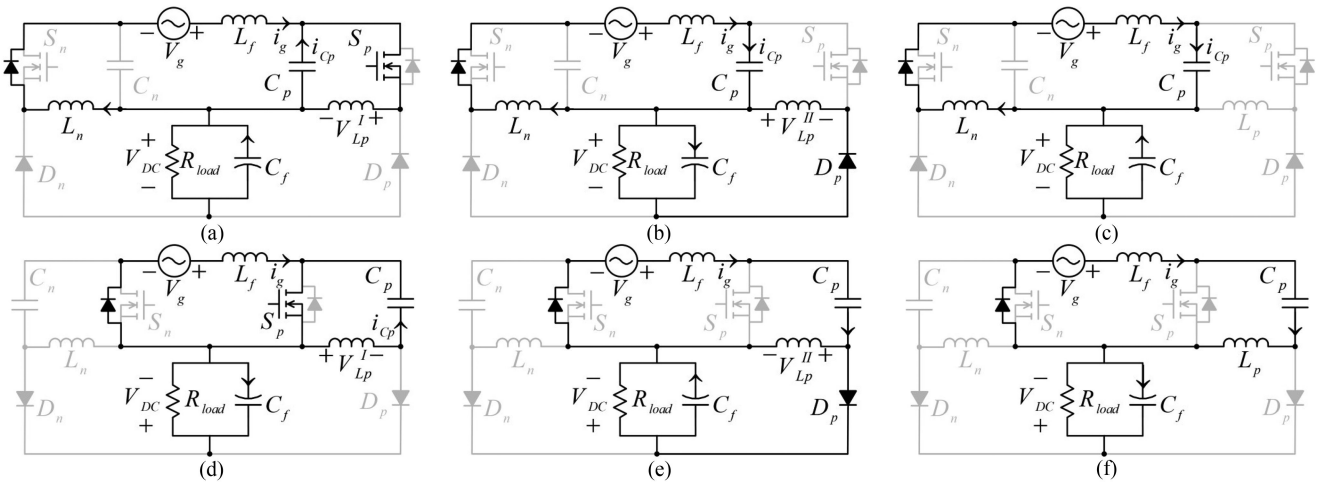

Fig. 2. Operation mode. (a) I. (b) II. (c) III of FR type I, and mode. (d) I. (e) II. (f) III of FR type II, during positive input voltage half cycle.

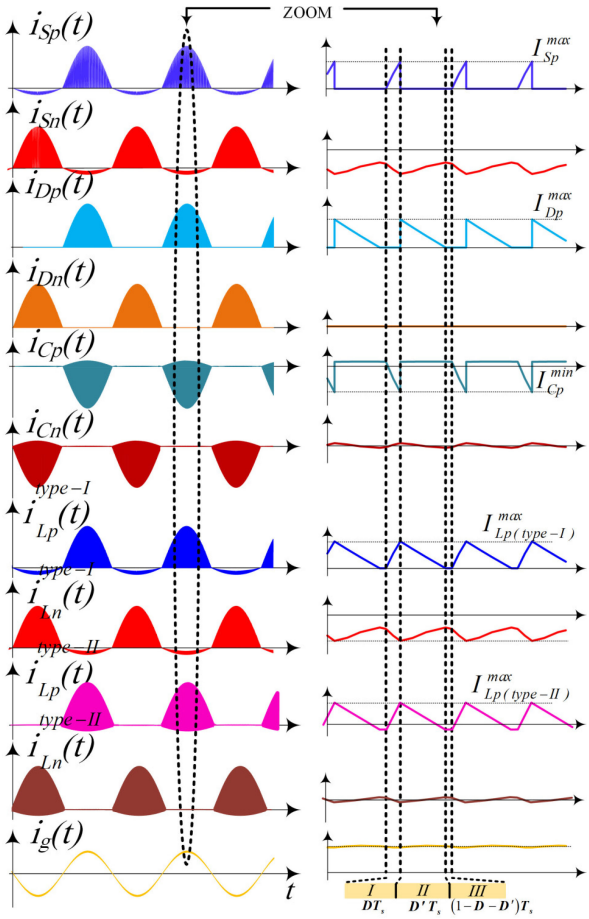

Fig. 3. Current waveforms of FRs.

2) Mode II ($D'T_s$):

a) Proposed FR Type I: As obvious from Figs. 2(b) and 3, the stored energy in L_p discharges to the output load through the HF diode D_p. At the same time, the input current flows through the capacitor C_p to charge it. On contrary to the previous mode of operation, the input current of the proposed FR type I does not flow through L_p. The equations during this mode of operation are

$$\begin{cases} V_{Lp}^{\text{type}-I} = V_{\text{DC}} \\ I_{g-(pk)} = I_{Cp} \end{cases} \tag{3}$$

and its inductor current decreases to zero.

b) Proposed FR Type II: The performance of the proposed FR type II is the same as its type I counterpart during mode II with a different input current path, which is conducted from L_p back to the input, as shown in Figs. 2(e). While (3) still holds for type II, the current of its inductor L_p becomes negative at the end of mode II. From (2) and (3), one can conclude that the current of the inductor within the FR type II has a lower peak value compared to the type I. This reduces the required size of the magnetic core for the inductors of the FR type II than its type I. This mode ends when the diode D_p current reaches to zero. By applying the volt-second balance on the voltage across each inductor and considering the duty cycle D, one can obtain D', called the DCM duty cycle, as

$$\begin{cases} D' = \dfrac{D}{M}\sin(\omega t) \\ M = \dfrac{V_{\text{DC}}}{\sqrt{2}V_{g-(\text{rms})}} \end{cases}. \tag{4}$$

3) Mode III ($(D + D')T_s \sim T_s$):

From the end of the previous mode to the end of mode III, the voltage across the inductor L_p becomes zero. The input current flows through the capacitor C_p of the type I while it also passes through L_p of the type II, as seen from Fig. 3. The capacitor C_p keeps being charged in both types during this mode and the output load is fed from the output filter capacitor. As seen from all three operation modes shown in Fig. 2, the body diode of the MOSFET S_n is always conducting the input current during the whole positive half cycle of the input voltage, which is evident from its corresponding switch current waveform given in Fig. 3. Thus, any reverse recovery problem

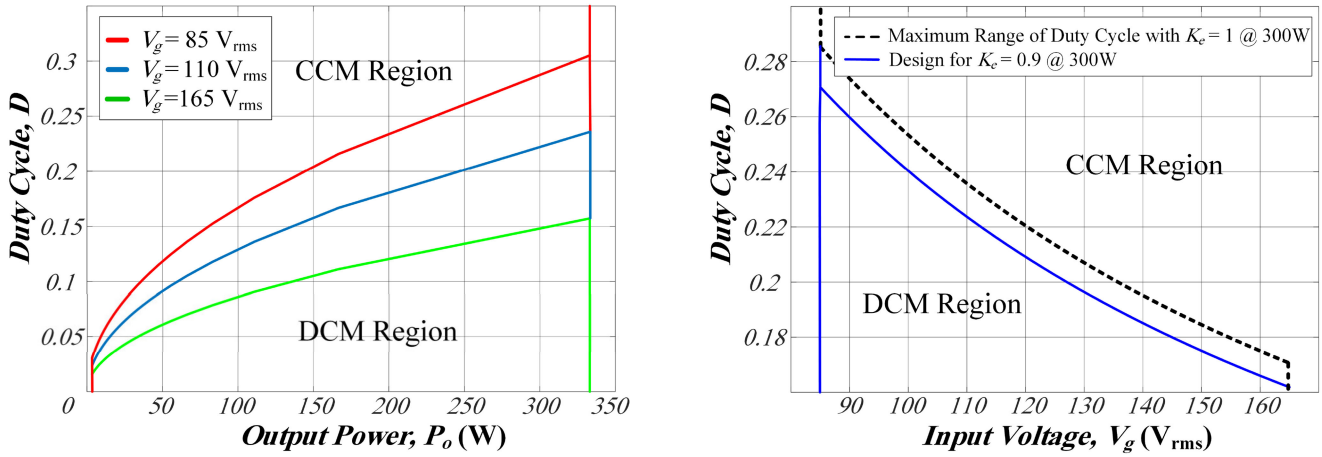

Fig. 4. Maximum duty cycle values for various (a) output powers, and (b) input voltages, assuming $V_{DC} = 48\ V_{dc}$.

and its related power losses is not concerned, since the body diode does not turn-OFF during the whole half cycle.

The operation principles of the FRs during the negative half cycle of the input voltage are the same as that analyzed above for the positive one.

From (4), one can conclude that both FRs can operate with buck-boost capability offering a wide range of the output voltage gain. Also, unlike the conventional buck-boost rectifiers, the FRs can provide a pure sinusoidal input current waveform to easily meet the power quality standards, such as IEC 61000-3-2 [26] without the need for additional ac filter components. Moreover, the components count, especially semiconductors, are lower compared to all well-known competitors.

III. Parameters Design and Comparison

A. Parameter Design

Following a similar approach as in [15], by assuming the proposed rectifiers operate in DCM, one can readily conclude that

$$D' < 1 - D. \tag{5}$$

Thus, in order to obtain the DCM duty cycle in terms of the circuit parameters, the average output diodes current is calculated according to Fig. 3 as

$$i_{Dp,n}^{\text{avg}} = \frac{V_{g-(\text{rms})}^2 D^2}{4 f_s L_e V_{DC}} = \frac{V_{g-(\text{rms})}^2}{2 R_e V_{DC}} \tag{6}$$

where $V_{g-(\text{rms})}$ is the rms value of the input voltage, f_s is the switching frequency and

$$\begin{cases} \dfrac{1}{L_e^{\text{type}-I}} = \dfrac{1}{L_{p,n}^{\text{type}-I}} \\ \dfrac{1}{L_e^{\text{type}-II}} = \dfrac{1}{L_{p,n}^{\text{type}-II}} + \dfrac{1}{L_f} \end{cases} \quad ; \quad R_e = \frac{2 f_s L_e}{D^2}. \tag{7}$$

Besides, one can also show that the average current of the output diodes during a half cycle of the input voltage is the same as the output dc load current, i.e.,

$$i_{Dp,n}^{\text{avg}} = I_{\text{load}} = \frac{V_{DC}}{R_{\text{load}}} \tag{8}$$

and if substituted from (6) in (8), one yields

$$\begin{cases} M = \sqrt{\dfrac{R_{\text{load}}}{2R_e}} = \dfrac{D}{\sqrt{2K_e}} \\ K_e = \dfrac{2 f_s L_e}{R_{\text{load}}}. \end{cases} \tag{9}$$

Considering (4), (5), and (9)

$$K_e < K_{e,crit} = \frac{1}{2(M + \sin(\omega t))^2}. \tag{10}$$

In order to ensure the DCM operation during entire line cycle, one can conclude that the designed K_e for the rectifiers must be satisfied as

$$\begin{cases} K_e < K_{e,crit\_\min} = \dfrac{1}{2(M+1)^2} \\ K_{e,\text{Ratio}} = \dfrac{K_e}{K_{e,crit\_\min}}. \end{cases} \tag{11}$$

As evident from the above calculations, two parameters of the input voltage and the output power can affect the maximum duty cycle value, which ensures the DCM operation for any specific output voltage. Therefore, the maximum duty cycle versus the output power and the input voltage is plotted in Fig. 4(a) and (b), respectively, when the proposed FRs are assumed to provide the same output voltage of $V_{DC} = 48\ V_{dc}$.

As obvious from this figure, the lower side of each curve is the DCM region while its upper side is the continuous conduction mode, i.e., the CCM region. With any variations of the output power and the input voltage, both proposed FRs guarantee their good performance by keeping their duty cycles lower than the boundaries plotted in Fig. 4.

The input filter inductor is designed according to the voltage applied across this inductor as

$$\begin{cases} L_f^{\text{type}-I} = \dfrac{\alpha\, V_{g-(\text{rms})}^2}{\Delta I_{Lf}\, f_s P_o} \\ L_f^{\text{type}-II} = \dfrac{D V_{g-(\text{rms})}^2}{\Delta I_{Lf}\, f_s P_o} \end{cases} \tag{12}$$

where α is the voltage ripple ratio of the C_p and C_n of the FR type I, ΔI_{Lf} is the desired input current ripple for the FR type II, and P_o is the output power.

The maximum currents through inductors L_p and L_n are also obtained as

$$\begin{cases} I_{Lp,n\,(\text{type}-I)}^{\max} = \dfrac{\sqrt{2}\, V_{g-(\text{rms})} D}{f_s L_{p,n\,(\text{type}-I)}} \\ I_{Lp,n\,(\text{type}-II)}^{\max} = \dfrac{\sqrt{2}\, V_{g-(\text{rms})} D}{f_s L_{p,n\,(\text{type}-II)}} - \sqrt{2} I_{g-(\text{rms})} \end{cases} \tag{13}$$

where $I_{g-(\text{rms})}$ is the rms of the input current for the nominal loading condition.

With regarding that the peak voltage across the capacitors of both proposed rectifiers is the same as the peak input voltage, one can design their capacitances by assuming β as their voltage ripple ratio using

$$C_{p,n} = (1-D)\,\frac{P_o}{\beta f_s V_{g-(\text{rms})}^2}. \tag{14}$$

As seen from Fig. 2, the *LC* networks are appeared across the input source constructed from the capacitors C_p and C_n, and the input and the output inductors L_f, L_p, and L_n. These *LC* networks cause resonances, which may appear in the input current waveform and drastically degrade its quality. Therefore, this situation must be avoided [27]. Following the same guidelines as [27], the capacitors C_p and C_n of the FRs are designed as

$$C_{p,n} = \frac{1}{(2\pi f_{res})^2 \times (L_f + L_{p/n})} \tag{15}$$

in which the resonance frequency f_{res} must be chosen within the range defined as

$$f_g < f_{res} < f_s \tag{16}$$

where f_g is the AC frequency.

In addition, the output filter capacitor is designed based on the rated output power and the tolerable voltage ripple at the dc side

$$C_f = \frac{P_o}{2\pi f_g \delta\, V_{\text{DC}}^2} \tag{17}$$

where δ is the acceptable output voltage ripple ratio.

The semiconductors ratings of the proposed rectifiers are obtained as in (18) to select the proper switches and diodes

$$\begin{cases} V_{Sp,n}^{\max} = V_{Dp,n}^{\max} = \sqrt{2}\, V_{g-(rms)} + V_{\text{DC}} \\ I_{Sp,n}^{\max} = I_{Dp,n}^{\max} = I_{Lp,n}^{\max}. \end{cases} \tag{18}$$

In addition to (18), the body diodes of the MOSFETs S_p and S_n must have the capability to conduct the input current, which is much lower than the output inductors L_p and L_n currents.

B. Comparison

The numerical comparison among various PFC rectifiers is performed and the results are given in Table I. The number of components and the semiconductors conducting simultaneously during each mode of operation are compared in this table. Both proposed rectifiers employ the lowest number of semiconductors. Also, the number of conducting semiconductors within the proposed rectifiers is comparably low. Moreover, the number of inductive elements is relatively lower for the proposed rectifiers than that for the competitors and at the same time they do not need any input filter capacitor unlike the rectifiers of [15]–[20]. Evidently, the aforementioned properties directly translate to a low total power loss and small converter size, as discussed in Section II. In addition, the presence of an LF (HF) current path between the input and the output, which affects the common mode noise of the rectifiers is also given in Table I based on the directions discussed in [3]. According to this table and the operation principles discussed in Section II, both proposed FRs benefit from an LF current path between the source and the output to avoid common mode noise. Moreover, the total voltage and current stresses of the semiconductors are calculated for $M = 0.3$ and given in Table I for each circuit after normalization based on those derived values for the proposed FRs. It is obvious from Table I that the total voltage and current stresses of the semiconductors of both proposed FRs are lower than most of their competitors.

According to Table I, it must be noted that the rectifiers of [12]–[15] employ a high number of HF diodes. In addition, the number of semiconductors conducting in each mode of operation of the rectifier of [17] is higher than that of the proposed ones. Also, on contrary to the proposed rectifiers, a HF current flows through the body diodes of the MOSFETs of rectifiers of [18]–[20] from which the power losses increase due to their reverse recovery issue.

The most important features of any PFC rectifier are the power loss and the THD of the input current. Thus, as a comparative analysis, the FRs are designed according to the previous section procedure along with the other rectifiers with assuming a constant and same $K_{e,\text{Ratio}}$, given in (11), and the same output power and input and output voltages. By using the power loss calculation methods given in [28] and [29] and assuming the same semiconductors, the total power losses of all under study rectifiers are calculated and compared in Table I. Also, loss distribution among circuit components is compared in Fig. 5(a). Accordingly, the FR type II offers the lowest power loss compared to all other rectifiers. Also, the FR type I have a comparably low power loss, especially when compared to the rectifiers of [13] and [14].

In order to derive and compare the input currents THDs of the under-study rectifiers, they are simulated in PLECS software to generate 48 V_{dc} from 110 V_{rms}/60 Hz feeding a 300 W dc load. The results are reported in Table I and THD variations at different

TABLE I
COMPARISON AMONG VARIOUS RECTIFIERS

Feature		Proposed FRs		Pseudo Buck-Boost of [12]	Buck-Boost of [13]	Buck-Boost of [14]	Sepic of [15]	Cuk (Type III) of [16]	Cuk of [17]	Cuk/Sepic of [18]-[20]
No. of switches		2		2	2	2	2	2	1	2
No. of fast diodes		2		5	4	4	3	2	2	1
No. of slow diodes		---		---	---	---	2	2	4	2
No. of inductors		3		3	3	3	3	4	3	2
No. of magnetic cores		2		2	3	3	3	2	3	2
No. of capacitors		3		2	3	2	3	3	2	2
No. of isolated gate drivers		Type I: 2	Type II: 1	1	2	2	1	1	1	2
No. of semics. Conducting Current	Mode I	2		3	2	2	3	2	3	3
	Mode II	2		1	1	1	2	2	4	3
	Mode III	1		---	---	---	1	1	2	2
Need for AC input filter capacitor		No		Yes	Yes	Yes	No	No	No	No
Current path between input and output		LF		NA	NA	NA	LF	LF	HF	LF
Voltage gain in continuous conduction mode, (CCM)		$\frac{D}{1-D}$		$\frac{D}{2(1-D)}$	$\frac{2D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{2(1-D)}$	$\frac{D}{1-D}$
Ratio of total voltage stress of semics. at $M = 0.3$, $\sum V_s / \sum V_{s\_FRs}$		Type I: 1	Type II: 1	1.54	1.39	1.5	1.31	1.39	1.39	1.25
Ratio of total current stress of semics. at $M = 0.3$, $\sum I_s / \sum I_{s\_FRs}$		1	1	1.78	2.56	1.47	1.3	1.05	0.6	0.92
Calculated efficiency @ $48V_{dc}$ & 300W		95.7%	96.3%	94.2%	92.4%	95.5%	95.2%	96%	95.85%	95%
Input current *THD* @ $48V_{dc}$ & 300W		2%/	9.6%	2.4%	1.9%	1.5%	9.7%	9.7%	15.8%	9.7%

NA – Not Available

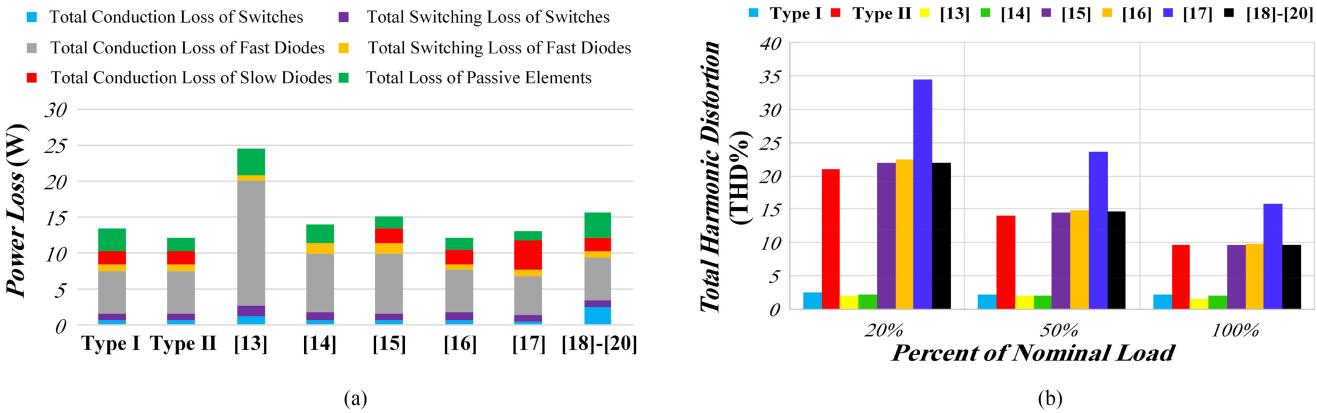

Fig. 5. Comparison of (a) power loss, and (b) input current THDs among various PFC rectifiers.

power levels are shown in Fig. 5(b). Obviously, the input current THD of the FR type I is as low as that of the rectifiers of [13] and [14], while it is higher for the FR type II similar to the rectifiers in [15], [16], and [18]–[20]. One can conclude that both proposed FRs offer low power losses (especially for type II) and comparably low input current THDs (especially for type I), with the lowest number of semiconductors compared to the competitors.

Overall, the proposed FR type II offers a slightly lower total power loss at the cost of a higher input current THD. On the

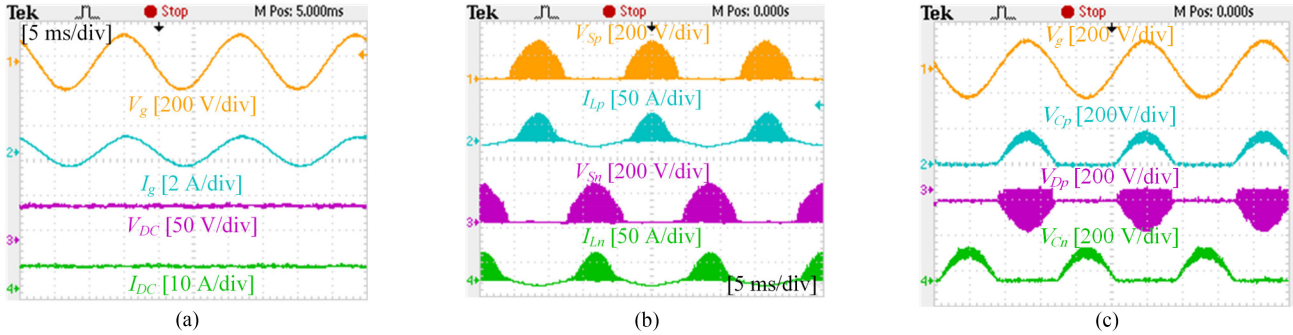

Fig. 6. Experimental results of (a) input and output voltages and currents, (b) switches S_p and S_n voltages and inductors L_p and L_n currents, and (c) capacitors and diode D_p voltages of FR type I at rated power.

TABLE II
EXPERIMENTAL TESTS CONDITIONS AND PARAMETERS

Description	Values
Rated power, P_o	300W
Input source, $V_{g\text{-}(rms)}/f_g$	110V_{rms}/60Hz
Output DC voltage, V_{DC}	48V_{dc}
Switching frequency, f_s	60kHz
Capacitors, $C_p = C_n$, C_f	1µF/250V, 6800µF/63V
Inductors, $L_p = L_n$, L_f	16µH, 450µH
Switches, S_p & S_n	IXFH80N25X3
Diodes, D_p & D_n	VS-60EPU04PbF

other hand, the proposed FR type I requires two isolated gate driver circuits instead of only one of the type II and some other competitors.

IV. EXPERIMENTAL CONFIRMATION

According to the guidelines given in Section III, a test rig for both proposed FRs is implemented in the laboratory to feed a 300 W, 48 $V_{\rm dc}$ load from 110 $V_{\rm rms}$/60 Hz AC source. The components and the test conditions are given in Table II. The switching frequency is 60 kHz. The inductors L_p and L_n are 16 μH, which ensures the DCM operation at the rated power. Moreover, they are symmetrically wound on each side-limb of a common magnetic core to even more reduce the size and cost of the core. The capacitors C_p and C_n are selected so as to avoid any resonance within the input current waveform as already designed as (15). The output capacitor is also designed to keep the output voltage ripple as low as 5% of 48 $V_{\rm dc}$ when the proposed FRs operate at the rated power.

The experimental input and output voltage and current waveforms are presented in Figs. 6(a) and 7(a) for types I and II, respectively. As seen from these figures, the output voltage is fixed to 48 $V_{\rm dc}$ with a ripple ratio of $\delta = 0.06$ by manually adjusting the duty cycle while a purely sinusoidal current is drawn from the input ac source. The same experiments are performed at 50% and 20% of the rated power and the input current quality factors are then measured by FLUKE-435 power analyzer and plotted in Fig. 8. According to Fig. 8(a), the PF of the input current is close-to-unity for both FRs. Also, the THDs shown in Fig. 8(b) are lower than 5% for the FR type I while they are higher for the FR type II, which is due to employing the same input inductor L_f for both types during the tests. By properly designing the input inductor for the FR type II, the same or even better THDs than those reported in [15]–[20] can be readily achieved.

The voltage waveforms across the positive and the negative switches S_p and S_n along with their corresponding inductor currents are measured and depicted in Figs. 6(b) and 7(b). As obvious from these measurements, the voltages across the switches are almost zero during their non-operating half cycle of the input voltage, which confirms a half cycle conduction of the MOSFETs body diodes. Moreover, the inductors currents of the FR type I shown in Fig. 6(b) provide the input current path during their nonoperating half cycle while those of the FR type II do not, as shown in Fig. 7(b). According to Fig. 3, these results were already expected. The capacitors voltages V_{Cp} and V_{Cn} are also presented in Figs. 6(c) and 7(c) for the FR types I and II, respectively, where the peak of the input ac voltage equals to the maximum capacitors voltages.

As a general conclusion, one can easily say that the experimental results truly verify the operation principles and the theoretical claimed properties of the proposed FRs.

Finally, the efficiency values of both proposed FRs measured from the tests at 20%, 50%, and 100% of the rated power are plotted in Fig. 9. As seen from this figure, the peak efficiencies of 93.26% and 93.87% are read for the FR types I and II, respectively, at the rated output power. The FR type II offers a bit higher efficiency than its counterpart, which is a result of its lower inductors and capacitors currents, as discussed in Section II.

Following previous analyses, one can conclude that the FR type II offers a little higher efficiency than its type I counterpart at the cost of a slightly higher THD value. Both proposed FRs ensure the input current with close-to-unity PFs and acceptable THDs without the need for any extra input ac filter capacitor and by employing the lowest number of semiconductors. Despite a subtle difference between the topologies, both FRs have the same components with nearly the same ratings. Also, both benefit from an LF current path between the input and the load to mitigate the common mode noise. So, based on the main priority

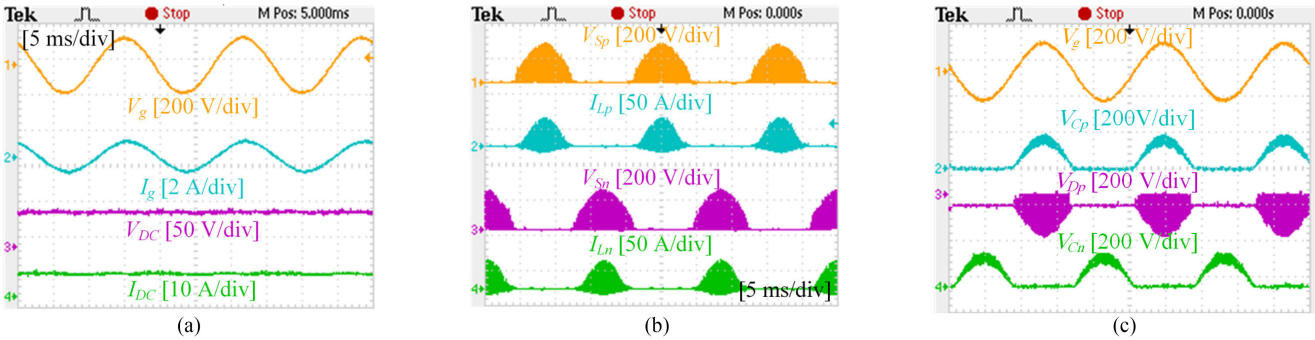

Fig. 7. Experimental results of (a) input and output voltages and currents, (b) switches S_p and S_n voltages and inductors L_p and L_n currents, and (c) capacitors and diode D_p voltages of FR type II at rated power.

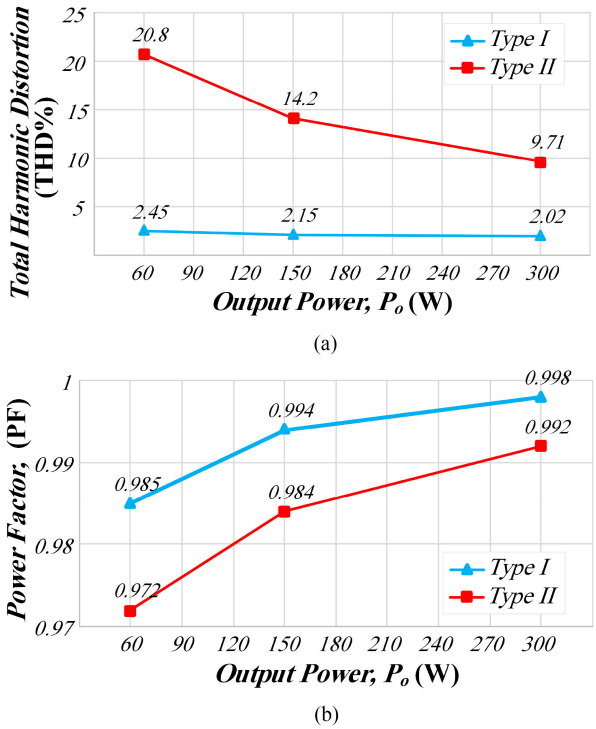

Fig. 8. Measured (a) power factor, and (b) total harmonic distortion.

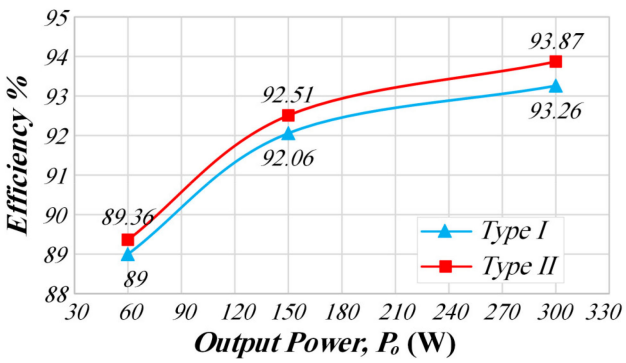

Fig. 9. Efficiency curves of proposed FRs.

of any specific application (efficiency or THD), one may decide to choose between them.

V. Conclusion

This article introduced two new single-phase buck-boost bridgeless PFC rectifiers, called the FRs. Both proposed rectifiers employ the lowest number of semiconductors with two integrated inductors on a common magnetic core. The proposed rectifiers utilize only two MOSFET switches without the reverse recovery problem of their body diodes. In addition, the proposed rectifiers employed two parallel capacitors to provide a current path for the input current during the discharge mode of the inductors to improve the power quality factors, known as PF and THD. The aforementioned features along with benefiting from the DCM operation of the inductors result in a low power loss and improved THD of the input current for both proposed rectifiers. Also, they benefit from a LF current path between the input and the load to mitigate the common mode noise. The theoretical achievements and the operation principles were all validated through experimental tests on a test rig of 300 W.

References

[1] J. Il Baek, J. K. Kim, J. B. Lee, H. S. Youn, and G. W. Moon, "A boost PFC stage utilized as half-bridge converter for high-efficiency dc-dc stage in power supply unit," *IEEE Trans. Power Electron.*, vol. 32, no. 10. pp. 7449–7457, Oct. 2017.

[2] Y. Wang, J. M. Alonso, and X. Ruan, "A review of LED drivers and related technologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5754–5765, Jul. 2017.

[3] L. Huber, Y. Jang, and M. M. Jovanović, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[4] A. M. Al Gabri, A. A. Fardoun, and E. H. Ismail, "Bridgeless PFC-Modified sepic rectifier with extended gain for universal input voltage applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4272–4282, Aug. 2015.

[5] Y.-S. Kim, W.-Y. Sung, and B.-K. Lee, "Comparative performance analysis of high density and efficiency PFC topologies," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2666–2679, Jun. 2014.

[6] M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Design of a highly efficient (97.7%) and very compact (2.2 kW/dm^3) isolated AC–DC telecom power supply module based on the multicell ISOP converter approach," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7750–7769, Oct. 2017.

[7] Y. Jang and M. M. Jovanović, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.
[8] S. Sharifi, M. Babaee, and M. Monfared, "A high gain buck PFC synchronous rectifier," in *Proc. Iranian Conf. Elect. Eng.*, 2018, pp. 1185–1190.
[9] X. Lin and F. Wang, "New bridgeless buck PFC converter with improved input current and power factor," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7730–7740, Oct. 2018.
[10] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A family of single-phase hybrid step-down PFC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5271–5281, Jul. 2017.
[11] S. Singh, B. Singh, G. Bhuvaneswari, and V. Bist, "Improved power quality switched-mode power supply using buck-boost converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 5194–5202, Nov./Dec. 2016.
[12] B. Zhao, A. Abramovitz, and K. Smedley, "Family of bridgeless buck-boost PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6524–6527, Dec. 2015.
[13] Z. Chen, B. Liu, P. Davari, and H. Wang, "Efficiency enhancement of bridgeless buck-boost PFC converter with unity PF and DC split to reduce voltage stresses," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, 2018, vol. 1, pp. 1187–1192.
[14] V. Bist and B. Singh, "An adjustable-speed PFC bridgeless buck–boost converter-Fed BLDC motor drive," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2665–2677, Jun. 2014.
[15] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New bridgeless DCM sepic and Cuk PFC rectifiers with low conduction and switching losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, Mar./Apr. 2011.
[16] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless cuk rectifiers for PFC applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3292–3301, Jul. 2012.
[17] B. R. Ananthapadmanabha, R. Maurya, and S. R. Arya, "Improved power quality switched inductor Cuk converter for battery charging application," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9412–9423, Nov. 2018.
[18] H. Farzaneh-Fard and M. Mahdavi, "Bridgeless CUK power factor correction rectifier with reduced conduction losses," *IET Power Electron.*, vol. 5, no. 9, pp. 1733–1740, 2012.
[19] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.
[20] Y. Liu, Y. Sun, and M. Su, "A control method for bridgeless Cuk/Sepic PFC Rectifier to achieve power decoupling," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7272–7276, Sep. 2017.
[21] S. Sharifi, F. Jahani, and M. Monfared, "Direct single-phase AC–AC converters based on series impedance networks," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10380–10389, Dec. 2018.
[22] S. Sharifi, M. Monfared, M. Babaei, and A. Pourfaraj, "Highly efficient single-phase buck-boost variable-frequency AC-AC converter with inherent commutation capability," *IEEE Trans. Ind. Electron.*, May 16, 2019.
[23] S. Sharifi and M. Monfared, "Series and tapped switched-coupled-inductors impedance networks," *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9498–9508, Dec. 2018.
[24] S. Sharifi and M. Monfared, "Modified series and tapped switched-coupled-inductors quasi-Z-source networks," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5970–5978, Aug. 2019.
[25] A. H. Masoumi, S. Sharifi, M. Monfared, and S. Karbasforooshan, "Γ-Source magnetic integrated filter for single-phase grid tied voltage source converters," *IEEE Trans. Ind. Electron.*, Aug. 14, 2019.
[26] *Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input Current ≤16 A per phase)*, *IEC 61000-3-2*, Electromagnetic Compatibility, 2005.
[27] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power factor preregulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct. 1997.
[28] D. Graovac and M. Pürschel, "MOSFET power losses calculation using the Data - Sheet parameters," *Infineon Technol. AG*, 2006.
[29] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Boston, MA, USA: Springer, 2001.

Saeed Sharifi received the B.Sc. (Hons.) and M.Sc. (Hons.) degrees in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2015 and 2018, respectively.

His research interests include power electronic converters, especially impedance networks, high order passive filters, grid connected converters, ac–ac converters, and rectifiers.

Mohammad Monfared (S'07–M'10–SM'15) received the B.Sc. degree in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2004, and the M.Sc. (with Hons.) and Ph.D. (with Hons.) degrees in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2006 and 2010, respectively.

He is currently an Associate Professor of Electrical Engineering with the Ferdowsi University of Mashhad. His research interests include power electronics, renewable energy systems, and power quality.

Dr. Monfared was the recipient of the Best Researcher Award from the Ferdowsi University of Mashhad in 2015.

Mohammad Babaei received the B.Sc. and M.Sc. degrees in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2016 and 2019, respectively.

His research interests include power electronic converters, especially rectifiers, impedance networks, ac–ac converters, and renewable energy systems.