An Extendable Quadratic Bidirectional DC-DC Converter for V2G and G2V Applications

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Abstract- This paper proposes an extendable quadratic bidirectional DC-DC converter that has an improved voltage transfer ratio (VTR) with capability of redundancy and modularity for electric vehicle applications. As *n* modules are embedded, its VTR becomes *n* times higher for both directions of currents. Furthermore, the common electrical ground between input and output is preserved. This is a simple structure with the lowest rating of semiconductors in the family of quadratic bidirectional converters leading to ease of control ability. The proposed converter performance is evaluated in both power flow direction using the dead-beat controller which is smooth, accurate and fast response. Finally, the process of charging/discharging of a lithium-ion battery is controlled through the proposed converter. A 500 W experimental results are provided in both power flow directions in closed-loop system in the presence of the proposed controller. The obtained results verify the applicability of this structure.

Index Terms- Bidirectional dc-dc converter, high voltage gain, battery charge/discharge, non-isolated, semiconductors rating.

I. INTRODUCTION

VEHICLE to grid (V2G) and grid to vehicle (G2V) capabilities have increased much popularity of electric vehicle (EVs) due to recovering stored electrical energy and thus, reducing the imbalance of energy demand and supply [1]. EVs with V2G and G2V capabilities are provided by a DC-DC bidirectional boost-buck converter, in which both power flow directions are available [2]-[4], as shown in Fig. 1. Late at night, when the price of electricity is low, the vehicle's battery (mostly lithium-ion) is charged through DC-DC and AC/DC converters. In the daytime, the battery supplies the power grid through the opposite direction of both converters [5]. Such batteries require a constant voltage at their polarity. So, the proper selection of converters for them will strongly enhances battery life [6]. However, the conventional DC-DC converters are exposed to limited applications due to their low voltage transfer ratio (VTR) and restricted duty cycles [7]. Therefore, the problem of voltage gain enhancement is the first order of priority among other technical issues [4]-[5].

Increase/decrease of voltage by changing the ratio of transformers has already been accomplished in isolated bidirectional structures for both directions [8]. Nevertheless, owing to the leakage flux of their transformer, these structures are in danger of voltage overshoot across their semiconductors, which reveals itself as spikes in action. Therefore, auxiliary snubber circuits such as RCDs and active clamped etc. have offered to alleviate or recycle these fluxes [6], [8]. Evidently, the costs rise due to the extra employed components. Moreover, researchers now believe that non-isolated structures can constitute the basic circuit for most of the renewable energy converters [9]. In this respect, many works have been devoted to non-isolated high VTR topologies. For instance, high VTR boost-buck ones have devised in [10]-[11], also quadratic ones in [12]-[14]. Switched capacitor architectures have given in [15]-[17] all for wide VTRs. Three level one has given in [18], but without high VTR. Common ground switched-quasi-Z-source converter has presented in [19]. Moreover, significant VTR has achieved in [20] with soft switching feature. Admittedly, the configurations such as in [10], [16]-[17] have designed without the common electrical ground. So, their applications are confined due to the serious electromagnetic interference (EMI). In this regard, extra devices such as EMI filters are required so; the costs and weight are increased in their circuit [19]. Into the bargain, multi-stage converters have adapted owing to their high VTRs in bidirectional structures. They have utilized sub-modules in series or parallels, which all have been cascaded or interleaved to obtain higher VTRs [21]. Their common advantages are redundancy and modularity [22]-[23]. For example, switched-capacitor in [24], a multilevel boost-buck in [25], cascaded design in [26] all have offered high modular VTRs.

Single phase on-board EV charger in [27] and [28], coupled inductor (CI) converter in [29], interleaved CI converter in [30] and [31] suffered from high number of elements.

Since the remarkable problem of isolation for isolated converters such as in [8] can put the performance of the battery in jeopardy, so a non-isolated structure circuit would be a compromise to be utilized [32]. Hence, this work only focuses
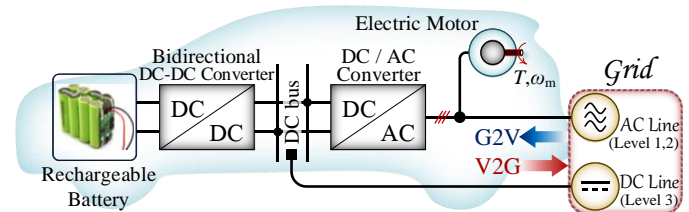

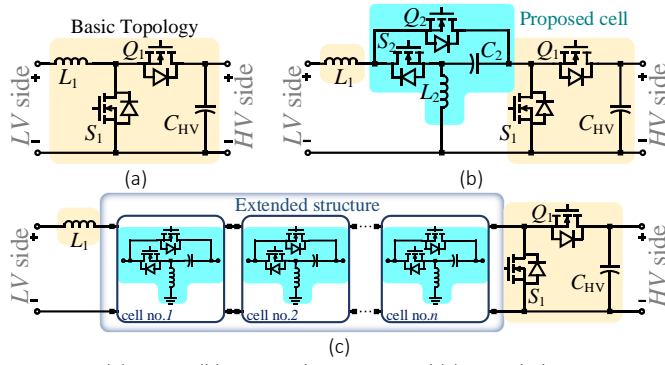Fig. 1. Energy system source of an EV.

Fig. 2. (a) FBBBC, (b) proposed converter and (c) extended structure.

on the bidirectional DC-DC converter of the G2V and V2G systems. In this paper, a non-isolated extendable bidirectional DC-DC is engaged to a lithium-ion battery. Furthermore, the dead-beat current controller is adapted for indirect current control of the step-up chopper and direct current control of the step-down chopper, which offers accurate, fast, and smooth control performance under different working conditions. The common electrical ground between input and output is preserved. Each stage comprises two alternative power switches, an inductor and a capacitor, which gives rise to VTR of $1/(1-D)$ and D for boost and buck modes of operation. Stage 1 is a fundamental bidirectional boost/buck converter. By applying n stages, the VTR also increases for both directions. This converter is characterized by being extendable, simple in structure and ease of controlling ability.

The paper is organized as follows. The multi-stage structure is presented in section II. Section III is devoted to steady state calculation. Practical considerations and comparisons in IV, the indirect and direct dead-beat controller illustration in section V, grid connected system is presented in section VI and experimental verification in section VII have all given. Finally, section VIII concludes the paper.

II. MULTI-STAGE STRUCTURE

Fig. 2 shows how the proposed converter topology is developed. Fig. 2(a) is the fundamental bidirectional boost-buck converter (FBBBC), V_{LV} and V_{HV} denote the low voltage and the high voltage sides, respectively. It consists of an inductor L_1, a capacitor C_1, and switches S_1 and Q_1. The switches conduct alternatively during a complete switching period. When a DC source is applied on the low voltage side, the output power at the high voltage side experiences the DC transfer ratio of $1/(1-D)$. Similarly, by applying the DC source on the high side, the output power at the low voltage experiences the DC transfer ratio of D. To magnify the VTR, FBBBC structure splits at the junction of L_1, S_1 and Q_1 as shown in Fig. 2(b). Now, the proposed cell is applied. Hence, S_1 and S_2 are both switching simultaneously, yet, Q_1 and Q_2 both performing alternate to S_1 and S_2. This structure can be extended by inserting further modules in series. By inserting n modules, the VTR of the obtained topology increased by amount equal to FBBBC of fundamental topology to the power of $(n + 1)$ in both step-up and step-down modes of operation, which is shown in Fig. 2(c).
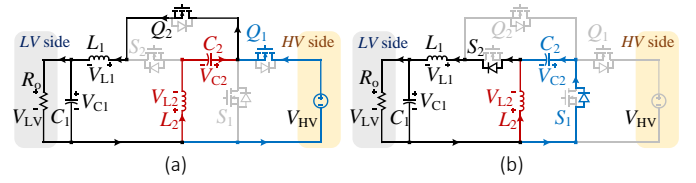

Fig. 3. Equivalent circuit of the proposed converter in step-down mode:
(a) state 1 and (b) state 2.

III. STEADY STATE CALCULATIONS

For the sake of simplicity, steady state calculations are made for this converter having one module or stage in its configuration. The step-up and the step-down modes, in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) can be defined as follows.

A. Step-down mode

A DC source is connected to the high side and a resistive load R_o to the low side. Two states for CCM (three states for DCM) operation are defined as:

State 1 (CCM and DCM) [0 - t_1]: According to Fig. 3(a), Q_1 and Q_2 are both conducting while S_1 and S_2 are blocked. In this period, L_1 is charged by the input DC source and released energy from L_2 and C_2. Thus, the current through L_1 increases, whereas it decreases for L_2 all linearly.

State 2 (CCM) [t_1 - T_s]: as shown in Fig. 3(b), during this time interval, Q_1 and Q_2 are both blocked whereas body diodes of S_1 and S_2 are conducting. The inductor L_1 releases its energy into the circuit to charge both L_2 and C_2 along with the output load. So, current through L_1 decreases, while for L_2. The relevant typical time-domain waveforms are shown in Fig. 4(a).

By applying volt-second balance on L_1 and L_2, we have

$$\begin{cases} \langle V_{L1} \rangle = DT_s(V_{HV} - V_{C1}) + (1-D)T_s(-V_{C1} - V_{C2}) = 0 \\ \langle V_{L2} \rangle = DT_s(V_{C2} - V_{HV}) + (1-D)T_s V_{C2} = 0 \end{cases} \tag{1}$$
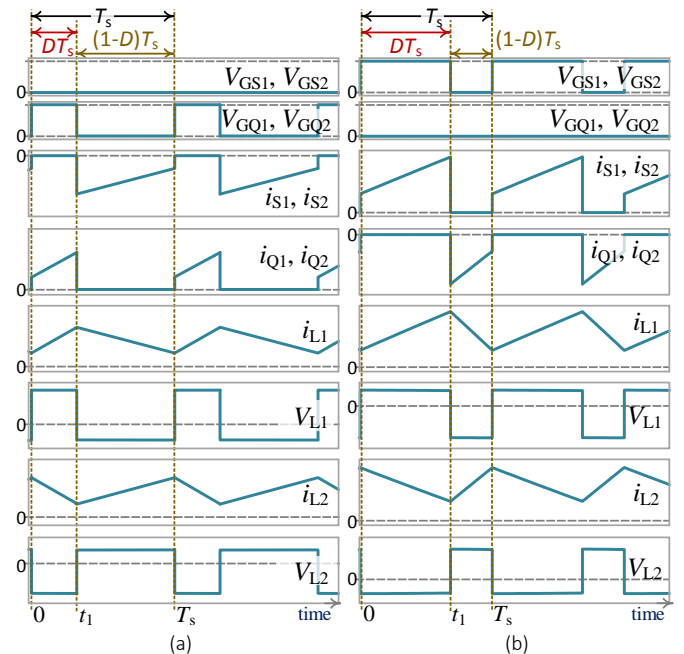

Fig. 4. Typical time-domain waveforms in CCM for:
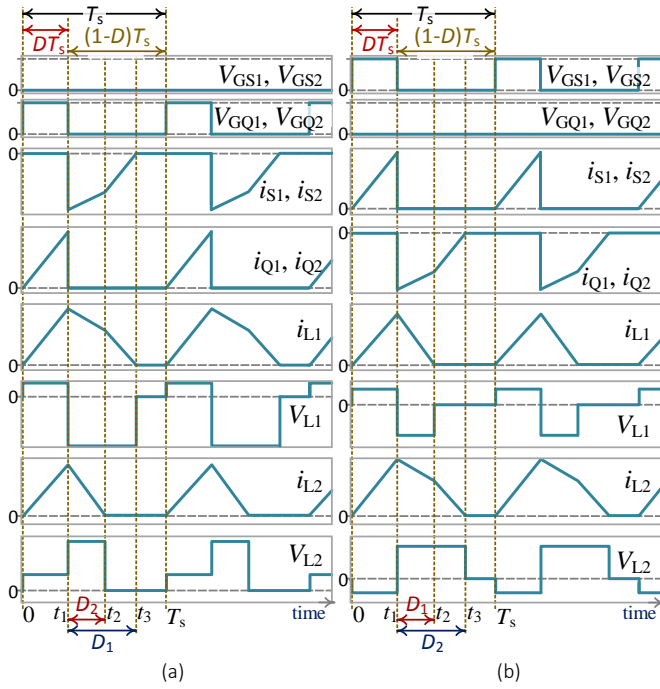(a) step-down mode and (b) step-up mode.

Fig. 5. Typical time-domain waveforms in DCM for:
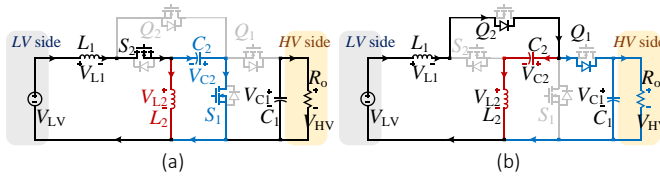(a) step-down mode and (b) step-up mode.

Fig. 6. Equivalent circuit of the proposed converter in step-up mode:
(a) state 1 and (b) state 2.

where D represents the duty cycle and T_s is switching period.

By solving (1), both capacitor voltages can be determined as

$$V_{C1} = D^2 V_{HV}, V_{C2} = D V_{HV} \qquad (2)$$

Clearly, the voltage across C_1 represents the DC VTR in CCM operation for step-down mode. Thereby, we have

$$M_{CC(Step-down)} = V_{LV}/V_{HV} = D^2 \qquad (3)$$

When n similar stages having the same switching operations and topology are inserted, the VTR of the obtained topology can be magnified by

$$M_{n-stage(Step-down)} = V_{LV}/V_{HV} = D^{n+1} \qquad (4)$$

The ampere-second balance equation is applied on capacitors C_1 and C_2, by which the following equations are derived.

$$\begin{cases} \langle I_{C1} \rangle = DT_s (i_{L1} - i_o) + (1-D)T_s (i_{L1} - i_o) = 0 \\ \langle I_{C2} \rangle = DT_s (-i_{L2}) + (1-D)T_s (i_{L1} - i_{L2}) = 0 \end{cases} \qquad (5)$$

Therefore, inductor currents I_{L1} and I_{L2} are acquired as

$$I_{L1} = I_o, I_{L2} = (1-D)I_o \qquad (6)$$

State 2 (DCM) [t_1 - t_2]: As shown in Fig. 5(a), Q_1 and Q_2 are turned off while body diodes of S_1 and S_2 are conducted.

State 3 (DCM) [t_2 - t_3]: According to Fig. 5(a), in this mode, the current through inductor L_2 meets zero.

State 4 (DCM) [t_3 - T_s]: In this mode, all of switches are

turned off. The current through inductors meets zero. At the end of this interval, a complete period T_s has been passed.

Considering these intervals, one can define D_1 and D_2 as duty cycles, at where the current of L_1 and L_2 becomes zero, respectively. In this regard, following equations can define as the voltage across inductors

$$V_{L1} = \begin{cases} +V_{HV} - V_{LV} & 0 \le t < DT_s \\ -V_{C2} - V_{LV} & DT_s \le t < (D+D_1)T_s \\ 0 & (D+D_1)T_s \le t < DT_s \end{cases} \qquad (7)$$

$$V_{L2} = \begin{cases} -V_{HV} + V_{C2} & 0 \le t < DT_s \\ +V_{C2} & DT_s \le t < (D+D_2)T_s \\ 0 & (D+D_2)T_s \le t < DT_s \end{cases} \qquad (8)$$

Now the volt-second balance is applied on both inductors. So, the voltage of capacitor is

$$V_{C2} = DV_{HV}/(D+D_2) \qquad (9)$$

As a result, the DCM voltage gain transferred ratio during the step-down mode can be obtained as:

$$M_{DCM(Step-down)} = \frac{V_{LV}}{V_{HV}} = \frac{D(D-D_1+D_2)}{(D+D_1)(D+D_2)} \qquad (10)$$

The current ripple of inductors L_1 and L_2 can be obtained as

$$\Delta i_{L1} = \frac{D(V_{HV} - V_{LV})}{L_1 f_s}, \Delta i_{L2} = \frac{D(-V_{HV} + V_{C2})}{L_2 f_s} \qquad (11)$$

where f_s is switching frequency.

By ignoring power losses and considering (6) the average current of L_1 and L_2 and duty cycles can be obtained as

$$I_{L1} = 0.5 \Delta i_{L1}(D+D_1), I_{L2} = 0.5 \Delta i_{L2}(D+D_2) \qquad (12)$$

$$D_1 = \frac{2V_{LV} f_s L_1}{R_o D(V_{HV} - V_{LV})} - D, D_2 = \frac{2V_{LV} f_s L_2(1-D)}{R_o D(-V_{HV} + V_{C2})} - D \qquad (13)$$

B. Step-up mode

In this mode, a DC source is connected to the low side and a resistive load R_o is connected to the high side. The relevant typical time-domain waveforms for this mode are given in Fig. 4(b). Two states for CCM (three states for DCM) operation can be defined as follows:

State 1 (CCM and DCM) [0 - t_1]: During this time interval, S_1 and S_2 are both on while Q_1 and Q_2 are off. In this state, the input DC source magnetizes L_1. Meanwhile, L_2 and C_2 release their energy into circuit. On the other side, C_1 delivers its energy to R_o. Thereby, the current through L_1 rises while that of L_2 decays. Relevant circuit and the power flow direction for this mode of operation is shown in Fig. 6(a).

State 2 (CCM) [t_1 - T_s]: As shown in Fig. 6(b), during this time, S_1 and S_2 are both blocked while body diodes of Q_1 and Q_2 are conducted. Meanwhile, the DC source and the released energy of L_1 tend to supply L_2, C_1 and the output load R_o. The current through L_1 decreases while through L_2 increases.

By applying volt-second balance on L_1 and L_2, we have

$$\begin{cases} \langle V_{L1} \rangle = DT_s (V_{LV} + V_{C2}) + (1-D)T_s (V_{LV} - V_{C1}) = 0 \\ \langle V_{L2} \rangle = DT_s (-V_{C2}) + (1-D)T_s (V_{C1} - V_{C2}) = 0 \end{cases} \qquad (14)$$

By solving (14) the voltage across both capacitors can be derived as follows

$$V_{C1} = V_{LV} / (1-D)^2, V_{C2} = V_{LV} / (1-D) \qquad (15)$$

It can be seen that V_{C1} indicates the DC VTR in CCM operation for step-up mode, which is given by

$$M_{CC(Step-up)} = V_{HV} / V_{LV} = 1 / (1-D)^2 \qquad (16)$$

When n similar stages are embedded, the VTR becomes

$$M_{n-stage(Step-up)} = V_{HV} / V_{LV} = 1 / (1-D)^{n+1} \qquad (17)$$

Now the ampere-second balance equation is applied on C_1 and C_2, by which the following equations can be attained.

$$\begin{cases} \langle I_{C1} \rangle = DT_s(-i_o) + (1-D)T_s(i_{L1} - i_{L2} - i_o) = 0 \\ \langle I_{C2} \rangle = DT_s(i_{L2} - i_{L1}) + (1-D)T_s i_{L2} = 0 \end{cases} \qquad (18)$$

Therein, inductor currents I_{L1} and I_{L2} are determined as:

$$I_{L1} = I_o / (1-D)^2, I_{L2} = I_o D / (1-D)^2 \qquad (19)$$

State 2 (DCM) [t_1 - t_2]: As shown in Fig. 5(b), S_1 and S_2 are turned off while body diodes of Q_1 and Q_2 are conducted.

State 3 (DCM) [t_2 - t_3]: According to Fig. 5(b), the current through inductor L_1 meets zero.

State 4 (DCM) [t_3 - T_s]: In this mode, all of the power switches are turned off. The current through inductors meets zero. At the end of this interval, a complete period T_s has been passed.

In this regard, following equations can define as the voltage across inductors

$$V_{L1} = \begin{cases} +V_{LV} + V_{C2} & 0 \le t < DT_s \\ +V_{LV} - V_{HV} & DT_s \le t < (D+D_1)T_s \\ 0 & (D+D_1)T_s \le t < DT_s \end{cases} \qquad (20)$$

$$V_{L2} = \begin{cases} -V_{C2} & 0 \le t < DT_s \\ -V_{C2} + V_{HV} & DT_s \le t < (D+D_2)T_s \\ 0 & (D+D_2)T_s \le t < DT_s \end{cases} \qquad (21)$$

Now the volt-second balance is applied on both inductors. So, the voltage of capacitor is

$$V_{C2} = D_2 V_{HV} / (D + D_2) \qquad (22)$$

As a result, the DCM voltage gain transferred ratio in the step-up mode can be obtained as:

$$M_{DCM(Step-up)} = \frac{V_{HV}}{V_{LV}} = \frac{(D+D_1)(D+D_2)}{DD_1 - DD_2 + D_1 D_2} \qquad (23)$$

The current ripple of inductors L_1 and L_2 can be obtained as

$$\Delta i_{L1} = D(V_{LV} - V_{C2}) / L_1 f_s, \Delta i_{L2} = -DV_{C2} / L_2 f_s \qquad (24)$$

By ignoring power losses and considering (12)

$$D_1 = \frac{2V_{HV} f_s L_1}{R_o D(1-D)^2 (V_{LV} - V_{C2})} - D, D_2 = \frac{2V_{HV} f_s L_2 D}{R_o D(1-D)^2 (-V_{C2})} - D \quad (25)$$

IV. PRACTICAL CONSIDERATIONS AND COMPARISON

A. Voltage and current stress

By applying KVL and KCL in Figs. 3 and 6, the voltage (V_{S1}, V_{S2}, V_{Q1}, V_{Q2}) and current stress (I_{S1}, I_{S2}, I_{Q1}, I_{Q2}) of each power switch in both modes can be attained as

$$S_1 : \begin{cases} step-down: V_{S1} = V_{HV}, I_{S1} = DI_o \\ step-up: V_{S1} = V_{HV}, I_{S1} = I_o / (1-D) \end{cases} \qquad (26)$$

$$S_2 : \begin{cases} step-down: V_{S2} = DV_{HV}, I_{S2} = I_o \\ step-up: V_{S2} = (1-D)V_{HV}, I_{S2} = I_o / (1-D)^2 \end{cases} \qquad (27)$$

$$Q_1 : \begin{cases} step-down: V_{Q1} = V_{HV}, I_{Q1} = DI_o \\ step-up: V_{Q1} = V_{HV}, I_{Q1} = I_o / (1-D) \end{cases} \qquad (28)$$

$$Q_2 : \begin{cases} step-down: V_{Q2} = DV_{HV}, I_{Q2} = I_o \\ step-up: V_{Q2} = (1-D)V_{HV}, I_{Q2} = I_o / (1-D)^2 \end{cases} \qquad (29)$$

B. Design of Components

Using (5) and (18), ripples of capacitors (Δv_{C1} and Δv_{C2}) can be earned for both step-down and step-up modes by

$$\begin{cases} \Delta v_{C1} = \dfrac{D_{Step-down}(i_{L1} - i_o)}{C_1 f_s} = \dfrac{D_{Step-up} i_o}{C_1 f_s} \\ \Delta v_{C2} = \dfrac{D_{Step-down}(1-D_{Step-down})i_o}{C_2 f_s} = \dfrac{D_{Step-up} i_o}{(1-D_{Step-up})C_2 f_s} \end{cases} \qquad (30)$$

Using (1) and (14), the inductor ripples (Δi_{L1} and Δi_{L2}) can be gained for both step-down and step-up modes by

$$\begin{cases} \Delta i_{L1} = \dfrac{D_{Step-down}(1-D_{Step-down}^2)V_{HV}}{L_1 f_s} = \dfrac{D_{Step-up}(2-D_{Step-up})V_{LV}}{(1-D_{Step-up})L_1 f_s} \\ \Delta i_{L2} = \dfrac{D_{Step-down}(1-D_{Step-down})V_{HV}}{L_2 f_s} = \dfrac{D_{Step-up}V_{LV}}{(1-D_{Step-up})L_2 f_s} \end{cases} \qquad (31)$$

Based on equations (30) and (31), the three-dimensional curves in both step-down and step-up modes are plotted in Fig. 7. The three axes denote the amount of required capacitor C_1 (or C_2), the percent of ripple Δv_{C1} (or Δv_{C2}) and D.

Similarly, to determine the values of inductors (L_1 and L_2) the three axes indicate the amount of required inductor L_1 (or L_2), the percent of ripple Δi_{L1} (or Δi_{L2}) and the duty cycle D.

Therefore, one can consider a constant value f_s and find the exact values of passive components based on the desired ripples and the duty cycle.

Considering 50 kHz as switching frequency, V_{LV} = 40 V, V_{HV} = 400 V, maximum current and voltage ripple is 1 A and 4 V, respectively, the critical passive components at the step-down mode are L_1 = 438 μH, L_2 = 346 μH, C_1 = 92 μF and C_2 = 52 μF. Similarly, at the step-up mode L_1 = 873 μH, L_2 = 848 μH, C_1 = 58 μF and C_2 = 19 μF.

C. Comparison

General information of the proposed converter and other leading competitors are provided in Table I. The proposed converter is compared with relevant structures that mostly have been used in battery charging, super capacitors and micro-grids, successfully. A voltage gain comparison is made between the proposed converter and the relevant bidirectional topologies. Fig. 8(a) displays the plotted VTRs in step-down mode. It is evident that as the duty cycle increases, the step-down capability for the proposed converter is much better than

FBBBC and converters in [17]-[19], and is approximately better than [10], [15] and [16], also in [22] and [26] for $n = 2$. Also, VTR in step-up mode is displayed in Fig. 8(b). The proposed converter offers higher VTR in compared with the mentioned cases. Moreover, the VTR of the proposed converter is much higher in comparison to extendable multi-stage cascaded structures, such as converter in [26]. Note that the proposed converter has fewer components than converter in [13] and [16]. Also, electrical common ground is maintained in the proposed converter, while those of [10], [16] and [17] do not.

Another comparison made between the proposed converter and quadratic ones. Their total voltage stresses of semiconductors (TVS) and total current stresses of semiconductors (TCS) are given in Table II and Fig. 9. According to this figure, the proposed converter offers a lower TCS in comparison to [12]. Also, TVS and TCS of the proposed converter are lower than [13]. Granted, the TCS of the proposed converter is lower than that of [14]; however, the proposed converter offers a much lower TVS in comparison to [14].

The main point in Fig. 9 curves is that the proposed converter offers the lowest maximum voltage and current for choosing the semiconductors in the family of quadratic bidirectional converter. As shown in Fig. 9, the maximum TVS of converters in [12], [13] and [14] is $2V_{HV}$, $2V_{HV}$ and $3V_{HV}$, respectively. Moreover, the maximum TVS of the proposed converter is $2V_{HV}$.

Similarly, the maximum TCS of converters in [12], [13] and [14] is $3I_{LV}$, $4I_{LV}$ and $2I_{LV}$, respectively. And the maximum TCS of the proposed converter is $2I_{LV}$.

Therefore, in the family of quadratic bidirectional converters, the proposed converter has the lowest TVS ($2V_{HV}$) and the lowest TCS ($2I_{LV}$).

V. DIRECT AND INDIRECT DEAD-BEAT CONTROLLER

As mentioned earlier, control of the proposed bidirectional converter includes two strategies: direct and indirect control of battery current. The overall proposed control system is shown in Fig. 10. By comparing the instantaneous value of source

Fig. 7. Components design: (a) C_1, (b) C_2, (c) L_1 and (d) L_2.
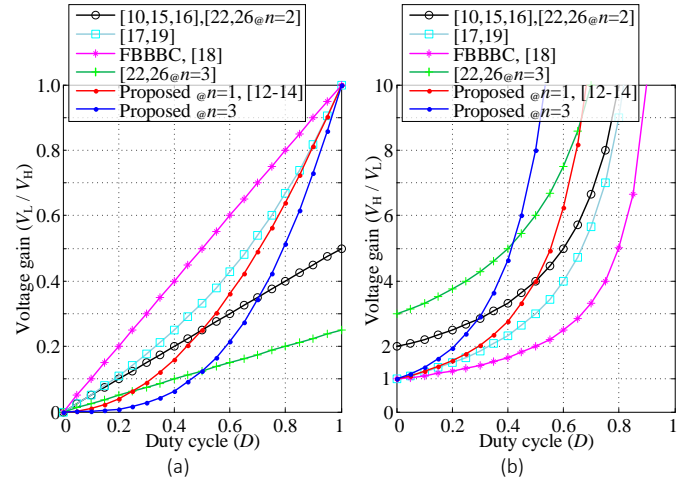

Fig. 8. Voltage gain curve during: (a) step-down and (b) step-up modes.

voltage and the load voltage, either step-down or step-up modes of operation are determined.

In this converter, a simple yet efficient digital dead-beat control concept is adopted for both current controllers. As will be shown, the dead-beat current controller can also simply determine the duty cycle, D, for the step-down stage directly from the measured source, load and C_1 voltages, measured and reference current with the L_1 inductance value as the only parameter to be known.

For the step-up mode, neglecting the losses, the following equation can be written:

$$V_{LV} i_{L1} = V_{HV}^2 / R_o \qquad (32)$$

The current i_{L1} can be regulated by directly calculating the optimal duty cycle for the next switching period by a dead-beat strategy. The simple yet efficient dead-beat indirect current control technique only requires the value of L_1 to directly calculate the switches duty cycle from the measured source and currents, measured inductor current and its reference.

As shown in Fig. 10(a), in the step-down mode, when Q_k is on, the voltage across the inductor L_1 can be determined as

$$V_{L1} = L_1 di_{L1} / dt = V_{HV} - V_{LV} \qquad (33)$$

The slope of the inductor current in Q_k on state ($\Delta_{on,step-down}$) can be determined as

$$\Delta_{on,step-down} = di_{L1}/dt = (V_{HV} - V_{LV})/L_1 \qquad (34)$$

Similarly, when the switch Q_k is off, the inductor voltage is

$$V_{L1} = L_1 di_{L1} / dt = -V_{C2} - V_{LV} \qquad (35)$$

The slope of inductor current in Q_k off state ($\Delta_{off,step-down}$) is

$$\Delta_{off,step-down} = di_{L1}/dt = (V_{C2} - V_{LV})/L_1 \qquad (36)$$

In the step-up operating mode, when S_k is on, the inductor voltage and the slope of the inductor current ($\Delta_{on,step-up}$) are

$$V_{L1} = L_1 di_{L1} / dt = V_{LV} + V_{C2} \qquad (37)$$

$$\Delta_{on,step-up} = di_{L1}/dt = (V_{LV} + V_{C2})/L_1 \qquad (38)$$

Similarly, when S_k is off, the inductor voltage and the slope of the inductor current ($\Delta_{off,step-up}$) are

$$V_{L1} = L_1 di_{L1} / dt = V_{LV} - V_{HV} \qquad (39)$$

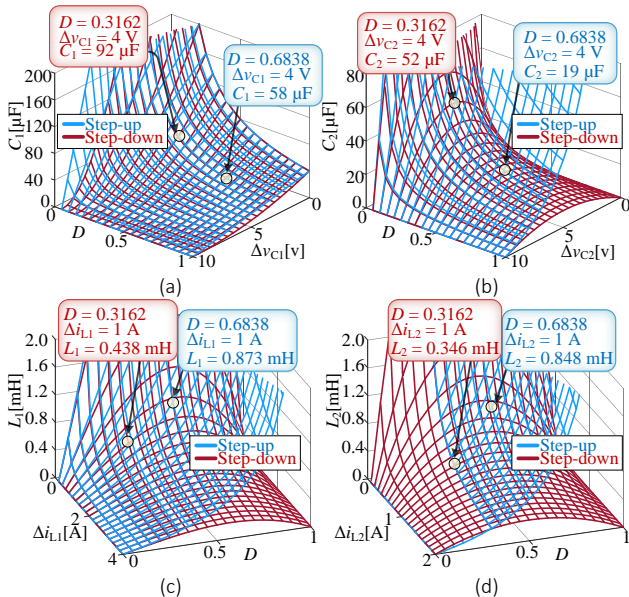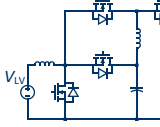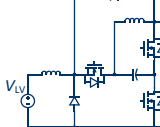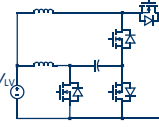$$\Delta_{off,step-up} = di_{L1}/dt = (V_{LV} - V_{HV})/L_1 \qquad (40)$$

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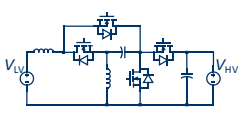
TABLE I
SUMMARIZED INFORMATION OF THE PROPOSED CONVERTER AND OTHER RELEVANT BIDIRECTIONAL STRUCTURES

Converter	No. of Elements	Voltage gain step-down mode	Voltage gain step-up mode	Electrical common ground	Rated power [W]	Switching Freq. [kHz]	Peak efficiency [%]
[10]	4 switches 3 capacitors 1 inductor	$D/2$	$2/(1-D)$	No	200	50	$< 95\%$
[15]	4 switches 3 capacitors 1 inductor	$D/2$	$2/(1-D)$	Yes	300	20	94.45%
[16]	5 switches 3 capacitors 2 inductors	$D/2$	$2/(1-D)$	No	1000	20	95.30%
[17]	3 switches 3 capacitors 2 inductors	$D/(2-D)$	$(1+D)/(1-D)$	No	2000	20	98.6%
[18]	4 switches 3 capacitors 1 inductor	D	$1/(1-D)$	Yes	1000	50	$< 97\%$
[19]	3 switches 3 capacitors 2 inductors	$D/(2-D)$	$(1+D)/(1-D)$	Yes	300	20	96.24%
[26]	6 switches 4 capacitors 2 inductors	$D/4$	$4/(1-D)$	Yes	500	100-400	97.1%
Proposed topology $n = 1$	4 switches 2 capacitors 2 inductors	D^{n+1}	$1/(1-D)^{n+1}$	Yes	500	50	97.1%

TABLE II
QUADRATIC GAIN BIDIRECTIONAL CONVERTERS ($V_{LV}/V_{HV} = D^2$; $V_{HV}/V_{LV} = 1/(1-D)^2$) COMPARISON

|		[12]	[13]	[14]	Proposed topology
Circuit diagram:					
No. of elements:		4 switches, 2 capacitors, 2 inductors	4 switches, 2 diodes, 2 capacitors, 2 inductors	4 switches, 2 capacitors, 2 inductors	4 switches, 2 capacitors, 2 inductors
Rated power: Peak efficiency: Switching frequency:		100 W 95.5 % 50 kHz	200 W 88.7 % 15 kHz	160 W ≈ 97 % 30 kHz	500 W 97.1 % 50 kHz
TVS step-down	$0 \le t < DT_s$:	V_{HV}	$2V_{HV}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$
	$DT_s \le t < T_s$:	$V_{HV} + \sqrt{V_{LV}V_{HV}}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$	$V_{HV} + 2\sqrt{V_{LV}V_{HV}}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$
TVS step-up	$0 \le t < DT_s$:	$V_{HV} + \sqrt{V_{LV}V_{HV}}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$	$V_{HV} + 2\sqrt{V_{LV}V_{HV}}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$
	$DT_s \le t < T_s$:	V_{HV}	$2V_{HV}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$	$V_{HV} + \sqrt{V_{LV}V_{HV}}$
TCS step-down	$0 \le t < DT_s$:	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$	$2I_o$	I_o	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$
	$DT_s \le t < T_s$:	$(1 + 2\sqrt{V_{LV}/V_{HV}})I_o$	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$
TCS step-up	$0 \le t < DT_s$:	$V_{HV}(1 + 2\sqrt{V_{LV}/V_{HV}})I_o/V_{LV}$	$V_{HV}(3 + \sqrt{V_{LV}/V_{HV}})I_o/V_{LV}$	$V_{HV}(1 + \sqrt{V_{LV}/V_{HV}})I_o/V_{LV}$	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$
	$DT_s \le t < T_s$:	$V_{HV}(1 + \sqrt{V_{LV}/V_{HV}})I_o/V_{LV}$	$2V_{HV}I_o/V_{LV}$	$V_{HV}I_o/V_{LV}$	$(1 + \sqrt{V_{LV}/V_{HV}})I_o$
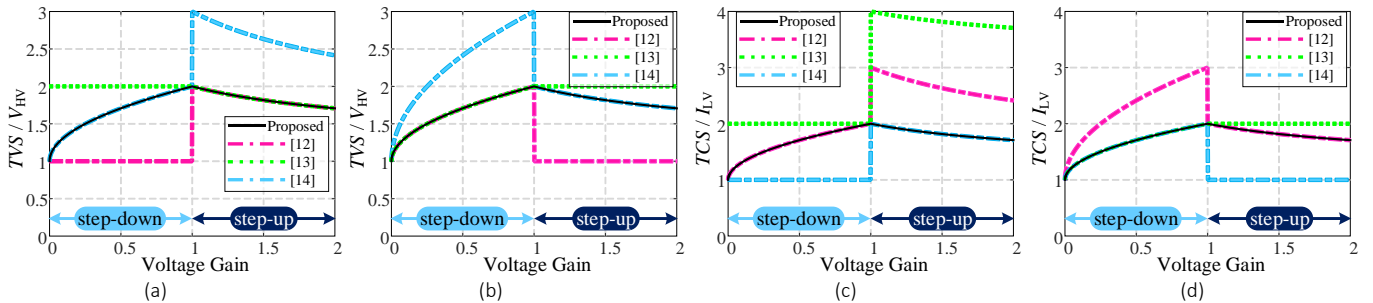
Fig. 9. TVS comparison during: (a) $0 \le t < DT_s$ and (b) $DT_s \le t < T_s$, TCS comparison during: (c) $0 \le t < DT_s$ and (d) $DT_s \le t < T_s$.
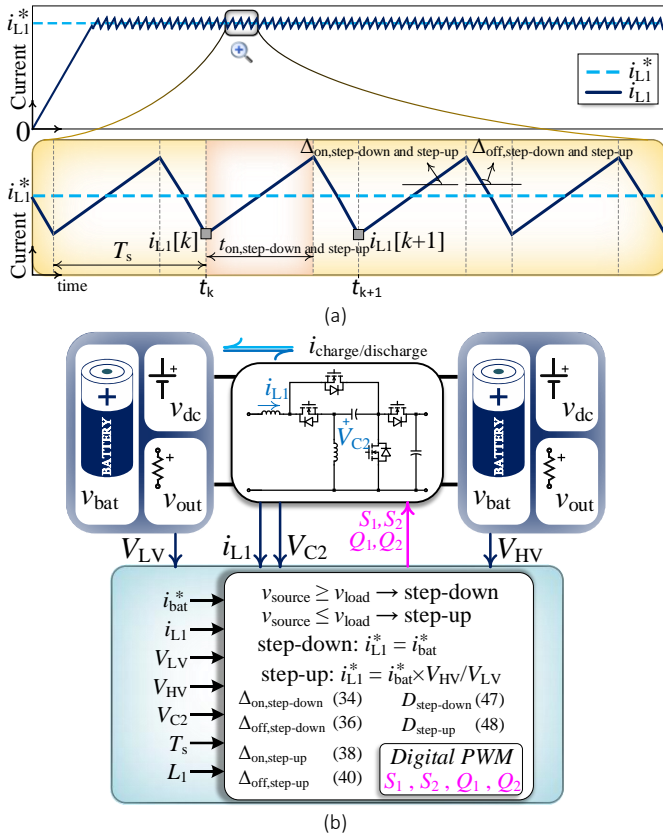
Fig. 10. (a) Working principle and (b) diagram of the control system.

Now one can predict the inductor current at the next sampling period ($i_{L1}[k+1]$) from its current value ($i_{L1}[k]$), by using the slopes already given by (34) and (36) for the step-down and by (38) and (40) for the step-up modes of operation, i.e.

$$i_{L1}[k+1] = i_{L1}[k] + \Delta_{\text{on,step-down}} t_{\text{on,step-down}} + \Delta_{\text{off,step-down}} t_{\text{off,step-down}} \quad (41)$$

$$i_{L1}[k+1] = i_{L1}[k] + \Delta_{\text{on,step-up}} t_{\text{on,step-up}} + \Delta_{\text{off,step-up}} t_{\text{off,step-up}} \quad (42)$$

where $t_{\text{on,step-down}}$ is the Q_k on state time, $t_{\text{off,step-down}}$ is the Q_k off state time during the step-down operation and $t_{\text{on,step-up}}$ is the S_k on state time, and $t_{\text{off,step-up}}$ is the S_k off state time during the step-up operation.

By forcing the error between the reference current (i_{L1}^*) and $i_{L1}[k+1]$, depicted as i_{err}, to be zero [33], [34], then

$$i_{err} = i_{L1}^* - i_{L1}[k+1] =$$
$$i_{L1}^* - i_{L1}[k] - \Delta_{\text{on,step-down}} t_{\text{on,step-down}} - \Delta_{\text{off,step-down}} t_{\text{off,step-down}} = 0 \quad (43)$$

$$i_{err} = i_{L1}^* - i_{L1}[k+1] =$$
$$i_{L1}^* - i_{L1}[k] - \Delta_{\text{on,step-up}} t_{\text{on,step-up}} - \Delta_{\text{off,step-up}} t_{\text{off,step-up}} = 0 \quad (44)$$

Therefore, $t_{\text{on,step-down}}$ and $t_{\text{on,step-up}}$ can be determined as

$$t_{\text{on,step-down}} = \frac{i_{L1}^* - i_{L1}[k] - (\Delta_{\text{off,step-down}} T_s)}{\Delta_{\text{on,step-down}} - \Delta_{\text{off,step-down}}} \quad (45)$$

$$t_{\text{on,step-up}} = \frac{i_{L1}^* - i_{L1}[k] - (\Delta_{\text{off,step-up}} T_s)}{\Delta_{\text{on,step-up}} - \Delta_{\text{off,step-up}}} \quad (46)$$

Using (45) and (46), the optimal duty cycles can be calculated as follows:

$$D_{\text{step-down}} = \frac{t_{\text{on,step-down}}}{T_s} = \frac{i_{L1}^* - i_{L1}[k] - (\Delta_{\text{off,step-down}} T_s)}{(\Delta_{\text{on,step-down}} - \Delta_{\text{off,step-down}}) T_s} \quad (47)$$

$$D_{\text{step-up}} = \frac{t_{\text{on,step-up}}}{T_s} = \frac{i_{L1}^* - i_{L1}[k] - (\Delta_{\text{off,step-up}} T_s)}{(\Delta_{\text{on,step-up}} - \Delta_{\text{off,step-up}}) T_s} \quad (48)$$

It must be mentioned that the average current through the inductor L_1 in each period is equal to the average current injected, since the average current of C_1 is zero at the steady state. Therefore, one can readily conclude that

$$i_{L1}^* = \begin{cases} |i_{\text{bat}}^*| & \text{step-down} \\ |i_{\text{bat}}^*| V_{HV}/V_{LV} & \text{step-up} \end{cases} \quad (49)$$

where i_{bat}^* is the reference battery current.

The simplified control diagram of proposed converter is shown in Fig. 10(b). By comparing the battery voltage and the source voltage, either in step-down or up modes of operation is determined and therefore the reference current i_{L1}^* is decided. This reference value and the measured current i_{L1} are then fed to the dead-beat algorithm, which directly and indirectly calculates the optimal duty cycles as already described above. The pulse width modulator (PWM) generates the switching pulses from the calculated duty cycles.

VI. PROPOSED CONTROL SYSTEM FOR V2G AND G2V

The proposed DC-DC converter is adopted as the pre-front stage for the bidirectional conventional DC-AC converter connected to the grid as shown in Fig. 11(a).

Fig. 11(b) shows the control diagram for the G2V and V2G operations of the proposed bidirectional EV charger. It consists of three control loops: an outer battery current control loop, a middle HV side control loop and an inner grid current, i_g control loop. When the grid voltage is normal, the charger is connected to the grid and can be operated in either G2V or V2G mode.

Based on [35], the battery voltage reference V_{LV}^* (or V_{bat}^*) is usually set as the full-charge voltage of the battery. When the battery is not fully charged, the output of the PI compensator in the constant power / constant voltage (CP/CV) control loop is saturated by the anti-windup mechanism limiter and LV side current reference i_{LV}^* (or i_{bat}^*) is determined by the upper limit value. P_{LV}^* is the desired amount of the power for either charging (G2V) or discharging (V2G).
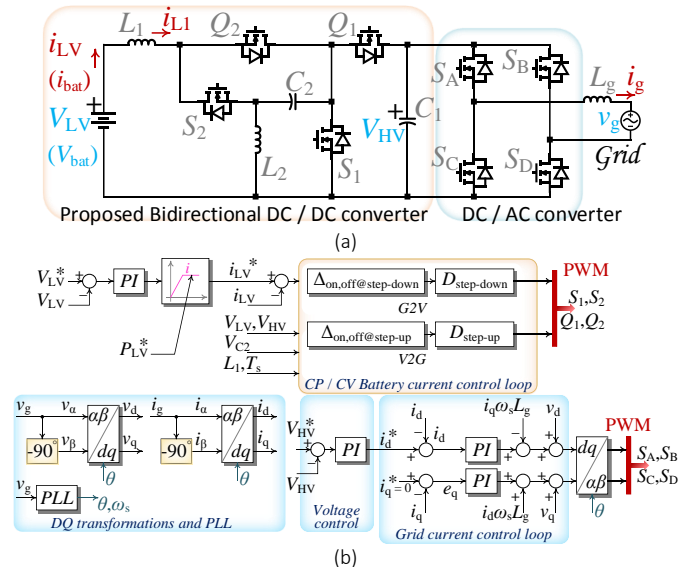

Fig. 11. Grid connected version of the proposed converter:
(a) Circuit and (b) control diagrams.

When V_{LV} reaches the full-charge voltage, the PI compensator in the CP/CV control loop is activated to regulate the battery voltage.

The outputs of the i_g control loop become the references of the grid current control loop. Therefore, the i_g is indirectly controlled by the magnitude V_{HV} and with respect to the phase of grid voltage, v_g.

VII. EXPERIMENTAL VERIFICATION

A 500 W laboratory prototype setup shown in Fig. 12, is provided with parameters listed in Table III. A STMicroelectronics STM32F303 floating point digital controller is used to implement the proposed control algorithm.

A. Proposed DC-DC converter operation

Fig. 13(a) demonstrates the step-down mode under steady state operation. It can be seen that the input DC source is 400 V and the voltage across the resistive load changes from 40 V up to 100 V with changing the reference voltage, stepwise. Subsequently, D varies stepwise from 0. 0.316 to 0.5. Assuming a constant value for load resistance, the load current varies with the change of current from HV side. Fig. 14(a) displays the gate signals, voltage and current of switches in step-down mode.

Fig. 13(b) shows the converter in step-up mode under steady state operation. In this case, the input DC voltage is 40 V and the output voltage is raised from 100 V up to 400 V as the reference voltage. Also, D is increased stepwise from 0.367 to 0.683. The proper performance of the proposed converter under the change of reference voltage contributes to appropriate and smooth behavior of the proposed control system. The voltage and current of switches are shown in Fig. 14(b).

DCM operation of the proposed converter during step-down and step-up modes are shown in Fig. 15(a) and (b), respectively. The values of V_{LV} and V_{HV} with respect to D, D_1 and D_2 confirm the DCM voltage gains.

B. Grid connected operation

The experimental results of the proposed control system for the grid connected converter G2V and V2G performances are shown in Fig. 16. The LV side current (or battery current i_b) reference and the HV side voltage reference is 15 A and 400 V, respectively. Battery voltage and grid voltage is 40 V and 110 V, respectively. The battery is charged (G2V) and discharged (V2G) with sinusoidal current, as shown in Fig. 16.

C. Proposed converter evaluation

Fig. 17(a) shows the measured efficiency curves under different strategies. The maximum efficiency in charging mode is 97.1 % while 96.9 % in discharging mode. A breakdown of the DC converter losses is presented in Fig. 17(b). It can be seen that a large portion of the loss is attributed to the conduction losses, which was calculated.
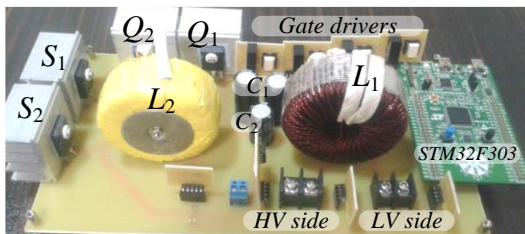

Fig. 12. Experimental prototype.

As mentioned earlier, the dead-beat current controller needs the value of L_1 to predict the optimal duty cycles. As a result, the performance of the dead-beat current controller, considering the L_1 mismatches, denoted by ΔL_1, in the term of output voltage is investigated and shown in Fig. 18. The stable operation of the proposed dead-beat current controller even with high mismatches is visible.

TABLE III
EXPERIMENTAL SETUP PARAMETERS

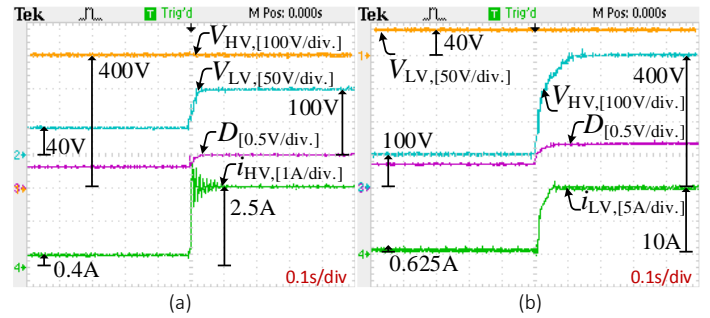| Parameter	Value
HV and LV side voltages	400 V and 40 V
Grid voltage	110 V, 50 Hz
Switching frequency	50 kHz
Output power	500 W
Inductor L_1 and L_2	1 mH
Capacitor C_1 and C_2	100 μF and 68 μF
MOSFETs	IPW60R099CPA

Fig. 13. Steady state operation of CCM in: (a) step-down and (b) step-up modes.
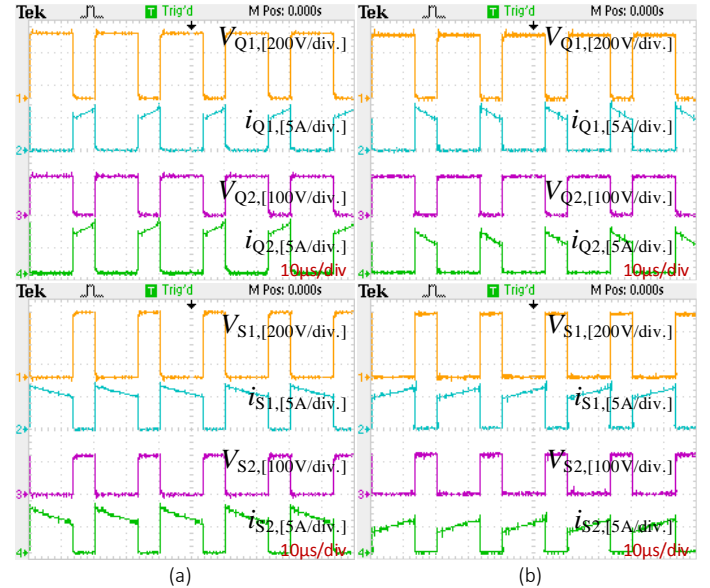
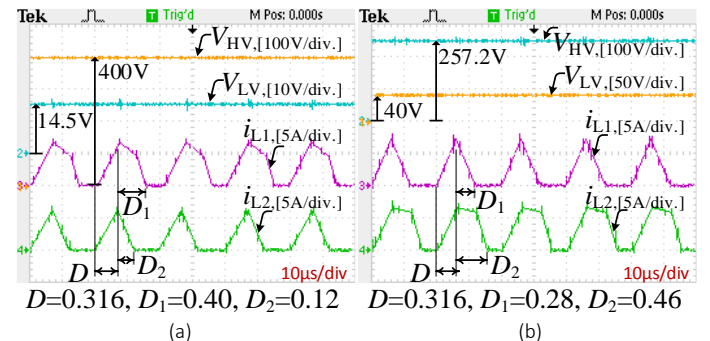Fig. 14. Voltage and current of switches: (a) step-down and (b) step-up modes.

D=0.316, D_1=0.40, D_2=0.12 D=0.316, D_1=0.28, D_2=0.46
(a)   (b)
Fig. 15. Steady state operation of DCM in: (a) step-down and (b) step-up modes.

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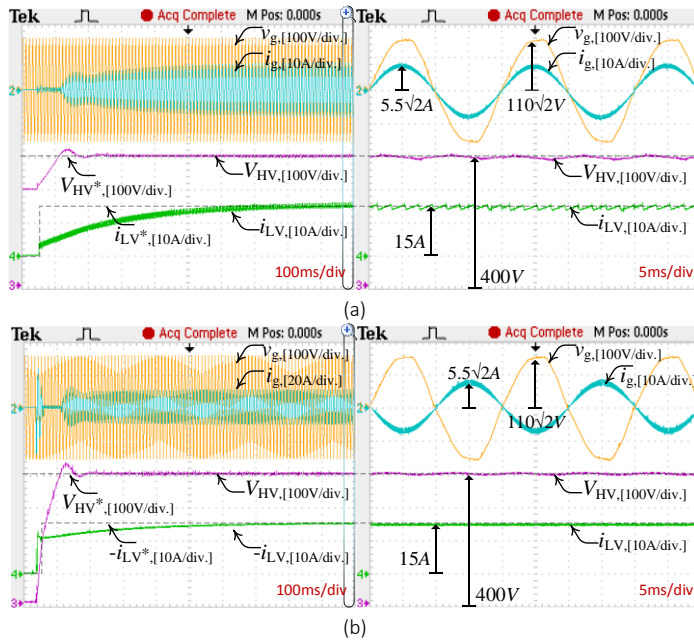IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS

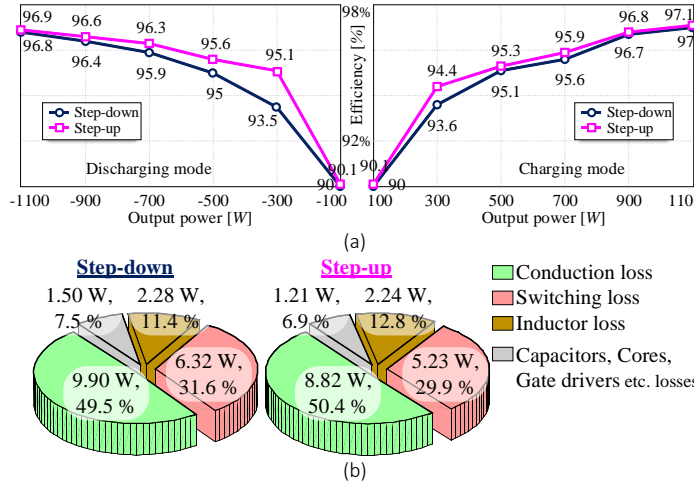Fig. 16. Grid connected operation during: (a) V2G and (b) G2V.

Fig. 17. Proposed converter:
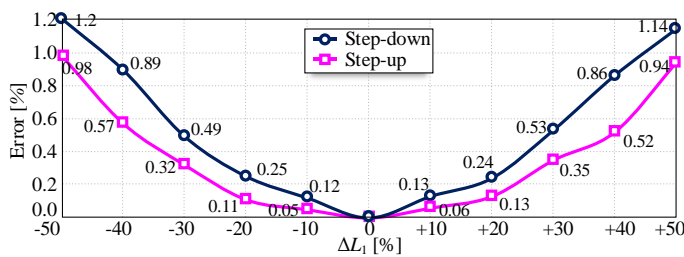(a) efficiency curve and (b) calculated loss breakdown at 500 W power.

Fig. 18. Error in output DC voltage versus L_1 mismatch under 500 W.

VIII. CONCLUSION

In this paper, an extendable bidirectional DC-DC converter for V2G and G2V applications has offered. This converter benefits from high step-down and high step-up voltage gains, extendibility, high efficiency, low rated switches, having common ground and bidirectional capability. The main disadvantages of the proposed converter are: complicated circuit diagram, complicated small signal model and highly sensitive voltage gain versus duty cycle. The proposed converter has married to rechargeable batteries under a smooth

and accurate dead-beat controller for both side of operation. Charge and discharge of the battery have successfully controlled through both directions of the proposed converter. The proposed converter has a maximum efficiency of 97.1 % at V_{LV} = 40 V, V_{HV} = 400 V, P_{out} = 500 W, and f_s = 50 kHz. Resultantly, the experimental waveforms are coincided with those expected from the proposed converter and make it a proper solution for on-grid EV applications.

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