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Comprehensive PowerLoss Analysis and Optimizing of FB PFC DAB DC/DC Battery Charger in Sinusoidal Charging

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Abstract— One of the most important restrictions of the double stage battery chargers is the capacity and size of the DC-link capacitors. In single-phase battery chargers, the input power is oscillating with double line frequency while the battery charged/discharged with DC power. The difference between these powers mostly stored in the DC-link. As a result, although the size of the passive component can be reduced by increasing switching frequency, the DC-link capacity is independent of the switching frequency. Sinusoidal charging is an innovative charging algorithm that leads to lower DC-link capacity and hence the charger requires less space. However, the effect of this charging method on the performance of the charger has not been investigated before. In this paper, a comprehensive power analysis of a FB PFC DAB DC/DC battery charger is performed. The results obtained from powerloss analysis show that sinusoidal charging reduces the efficiency of the system and also limits the range of the output power which further leads to lower efficiency. As the most of the powerloss related to the second stage, an optimizing TPS switching algorithm is selected to control the DAB DC/DC converter. Results show that the selected switching method well reduces the powerloss of the second stage and thereby the efficiency is increased.

Keywords—Battery charger, Electric vehicle, Powerloss, Sinusoidal charging.

I. INTRODUCTION

In recent years, concern over environmental pollution and its unfavorable effects on earth ecosystems such as global warming and climate changes is increased. Excessive emissions of greenhouse gases (GHGs) are the main reason for these harmful influences. The primary source of carbon dioxide emission is fossil fuel usage and transportation is one of the major sources of it [1, 2]. Adopting electric energy sources instead of fossil fuel allows EV to operate without emitting GHGs. Therefore, EVs are a promising solution for decreasing GHGs emissions in transportation. The quiet and audible noise-free operation, low maintenance, lower running cost, and better energy efficiency are the other advantages of EV over fossil fuel vehicles.

EV drive train can be divided into three main subsystems, i.e., electric propulsion subsystem, energy source subsystem, and auxiliary subsystem. The energy source subsystem consists of the energy management unit (EMU), energy source, and energy refueling unit [3]. The battery is the most adopted energy source in EVs which has high energy density, but low power density. Alongside new batteries that are often bulky and exorbitant, combining different energy sources, i.e., hybrid energy storage system

(HESS), such as the combination of battery and supercapacitor, which are presented to achieve high power and high energy density simultaneously [4-9].

The required power for charging the ESS is delivered through the energy refueling unit. Singh et al. [10] proposed a modified z-source PV grid-connected charger. However, the proposed structure added four more semiconductor devices which affect the overall efficiency of the system. In [11] design procedure of a compensative series LLC resonant network is proposed to realize ZVS for a wide range of loads. The Results show the improved efficiency at high loads but rather comparable at low loads. Zhang et al. [12] proposed an asymmetric center-tapped rectifier (ACTR) in order to decrease the intrinsic common-mode noise (CMN) of the half-bridge LLC converter. Dual active bridge (DAB) converter was first introduced by De doncker [13] in 1991. The DAB converter has many advantages such as electrical isolation, high reliability, less number of passive elements, high power density, the capability of soft switching and zero-voltage switching (ZVS) operation, and bidirectional power flow [13-15]. Therefore, the DAB topology is selected as the DC/DC converter of the second stage in this paper.

The battery chargers are categorized into off-board and on-board (OBC) chargers regarding their placement. OBC chargers have limited power rating (level 1 and level 2) which leads to lower cost and longer charging time. One-phase operation and simplified interconnection make them appropriate for house usage. One of the most important features of onboard chargers is the occupied space. Some literature integrates battery charger with an electric drive system to reduce the total weight and cost. Integrated chargers provide a low cost and high power OBC charger which are capable of fast charging [16, 19]. Double-stage OBC charger consists of two stages, i.e., AC/DC rectifier and DC/DC converter, which share a common DC-link capacitor. The first stage is a PFC structure which regulates the voltage of the DC-link, simultaneously and the second stage converts DC-link voltage to an appropriate voltage for the battery. The size of the passive components can be decreased by increasing the switching frequency, however; the DC-link capacitor size is independent of switching frequency. The input of the AC/DC rectifier is connected to the grid, so the input power oscillates with two times the line frequency. Most of this oscillating power is stored in the DC-link capacitor and the residual of it dissipates in other components in the form of the powerloss. Therefore,

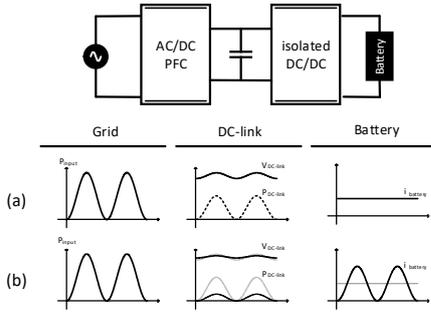


Fig. 1. The concept of sinusoidal charging. (a) constant current (CC) charging (b) sinusoidal charging

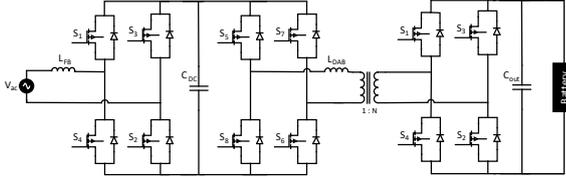


Fig. 2. The adopted FB PFC DAB DC/DC converter structure

the DC-link capacitor size is determined by the amplitude of the stored power having the two times line frequency. In general, the DC-link capacitor occupies most of the available space, particularly when the electrolytic capacitors are used. Ideally, the DC-link capacitor can be eliminated if the amplitude of this oscillating power decreased to zero. The principal of this concept firstly mentioned in [20-22] and further developed and named as sinusoidal charging by Xue [23, 24]. As shown in Fig. 1, if the battery is charged by an oscillating current with two times line frequency around its mean value the power and voltage ripple in the DC-link capacitor can be reduced. Another incentive for reducing DC-link capacitor size is the fact that electrolytic capacitors have a much lower lifetime than the film capacitors. At the moment, the film capacitors are only available at low sizes. Therefore, reducing the DC-link capacitor size lets designers to use film capacitors in chargers which increases the reliability and overall lifetime of the system.

Although the sinusoidal charging approaches render some interesting advantages but their effects on the powerloss of the system have not been studied properly. In this paper, a comprehensive analysis of the powerloss of a full-bridge (FB) PFC DAB DC/DC battery charger is performed. To do so, an accurate model of the powerloss of the system is presented. In addition, an optimal switching algorithm is provided to increase the system efficiency. The adopted structure and the modes of operation of each stage are described in the next section. The powerloss model of the system derived in section III. Simulation results in both CC and sinusoidal charging methods presented in section IV. Finally, section VI concludes the paper.

II. MODES OF OPERATION

Fig. 2 shows the battery charger studied in this paper which consists of FB PFC and DAB DC/DC converter. The input power transferred to the DC-link through the FB stage. The first stage controls the DC-link voltage and regulates the input current such that it would be in-phase with the grid voltage.

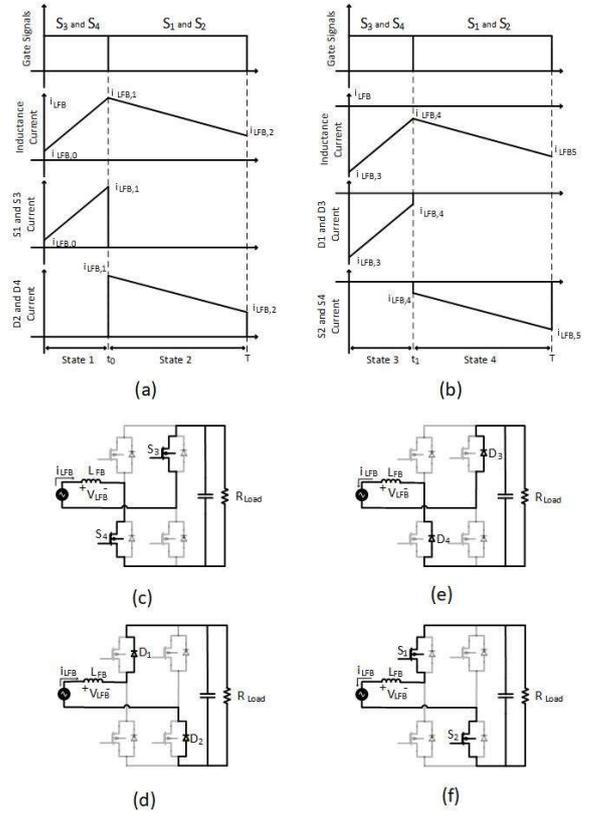


Fig. 3. Operational waveform at (a) positive (b) negative input current. (c) State 1 (d) State 2 (e) State 3 (f) State 4

A. Full-Bridge PFC

If we assumed that the input current in FB structure is in phase with voltage and the PFC is realized, then 4 modes of operation are possible based on the current direction. Fig. 3 shows all the possible operating modes and their corresponding waveforms.

B. Dual-Active Bridge Isolated DC/DC Converter

Based on the direction of the current and gate signals, eight operating states are possible. Fig. 4 shows the typical current waveforms and Fig. 5 the eight possible states and switches condition at each state.

In order to simulate the operation of the structure, the state-space equations of two stages are combined which leading to 32 possible states for the system operation. These are differential equations and can be solved by ode45 in MATLAB.

III. ANALYSIS

The powerloss of the system can be separated into FB stage powerloss and DAB stage powerloss. The PFC stage powerloss can be further divided into switching loss, conduction loss of switch and diode, inductance core and winding loss, and diode reverse recovery loss all indicated by $P_{PFC,sw}$, $P_{PFC,con}$, $P_{PFC,core}$, $P_{PFC,win}$, and $P_{PFC,rev}$, respectively. DAB stage powerloss consists of conduction loss, switching loss, inductance and transformer core and winding loss, and reverse recovery loss of diodes denoted by $P_{DAB,con}$, $P_{DAB,sw}$, $P_{DAB,core}$, $P_{DAB,win}$, respectively.

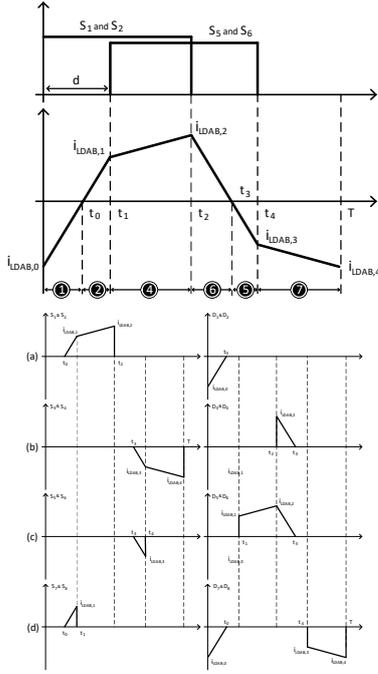


Fig. 4. Typical primary side inductance, switches, and diodes current waveforms in SPC control with CC charging

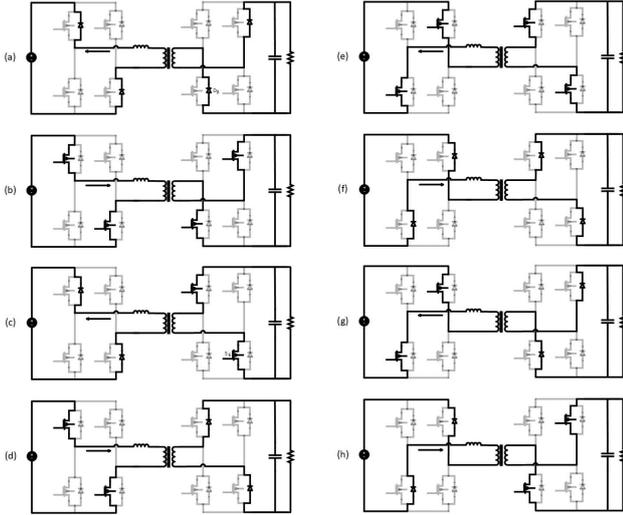


Fig. 5. DAB converter possible operating states. (a) state 1 (b) State 2 (c) State 3 (d) State 4 (e) State 5 (f) State 6 (g) state 7 (h) state 8

A. FB conduction and inductance winding powerloss

As the input current passes through the inductance, the winding loss can be calculated as

$$P_{PFC,con} = f_{line} \sum_{n=1}^{N1} \left(\int_0^{d(n)T_{S,FB}} R_{on}(n) i_{input}(t)^2 dt + \int_{d(n)T_{S,FB}}^{T_{S,FB}} R_{on}(n) i_{input}(t)^2 dt \right) \quad (7)$$

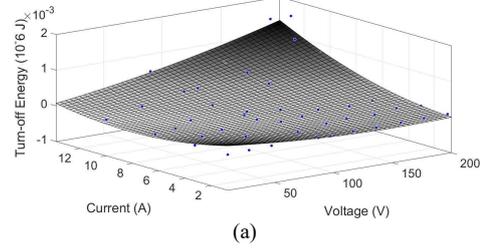
where N1 is the number of switching periods in one voltage cycle that is equal to $f_{S,FB}/f_{line}$ and n is the step index.

B. FB PFC switching powerloss

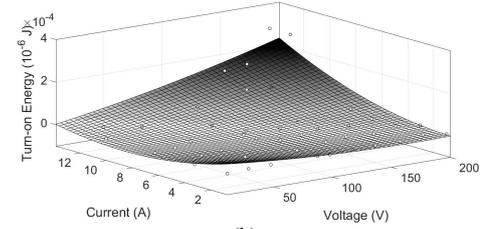
In order to provide an accurate switching powerloss, the dual-pulse test (DPT) to be employed. The DPT setup can be seen in Fig. 6. The test is utilized for BUP400D IGBT



Fig. 6. The DPT circuit



(a)



(b)

Fig. 7. Switching energy derived from DPT (a) Turn-on (b) Turn-off



Fig. 8. Reverse recovery SPT circuit

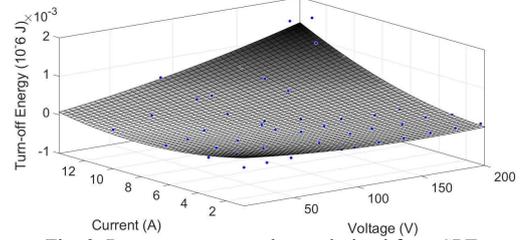


Fig. 9. Reverse recovery charge derived from SPT

in a wide range of voltages and currents in the interest of providing suitable data for adequate powerloss calculation. The switching energy can be described by (8) and (9) derived by second-order curve fitting. The results are shown in Fig. 7.

$$E_{on}(V_{ds}(t), i_{on}(t)) = p_{00} + p_{10}V_{ds}(t) + p_{01}i_{on}(t) + p_{20}V_{ds}(t)^2 + p_{11}V_{ds}(t)i_{on}(t) + p_{02}i_{on}(t)^2 \quad (8)$$

$$E_{on}(V_{ds}(t), i_{off}(t)) = p_{00} + p_{10}V_{ds}(t) + p_{01}i_{off}(t) + p_{20}V_{ds}(t)^2 + p_{11}V_{ds}(t)i_{off}(t) + p_{02}i_{off}(t)^2 \quad (9)$$

where V_{ds} is the switch voltage, $i_{on}(t)$ is the switch turn on current and $i_{off}(t)$ is the switch turn off current.

C. FB PFC inductance core powerloss

As the inductance current has a sinusoidal shape, the inductance core loss can be calculated by the Steinmetz equation. Based on Steinmetz approach the powerloss

density is equal to

$$P_{PFC,core} = k_h \left(\frac{f}{f_b} \right)^\alpha \left(\frac{B_{pk}}{B_b} \right)^\beta \quad (10)$$

where k_h , α , and β are the parameters obtained from curve fitting, f_b is base frequency, B_b is base flux density, and B_{pk} is the peak flux density, respectively. Basically, the base frequency and flux density in (10) assumed to be 1 Hz and 1 T, respectively.

D. FB PFC reverse recovery powerloss

The diode reverse recovery effect occurs at the turn off interval of a diode. After the diode forward current decreases to zero, it takes some time for stored charges in the depletion region and the semiconductor layers to be removed and this leads to a notable reverse charge that could last from few nanoseconds to some microsecond [24]. In order to calculate the reverse recovery powerloss of the diode, the single-pulse test (SPT) should be performed. Fig. 8 shows the PT test circuit and the experimental result. The curve fitting is also employed to develop a reverse recovery powerloss formula. The reverse recovery energy can be characterized by (11). The results are shown in Fig 9.

$$E_{rev,off}(V_{d,ak}(t), i_{d,on}(t)) = p_{00} + p_{10}V_{d,ak}(t) + p_{01}i_{d,on}(t) + p_{20}V_{d,ak}(t)^2 + p_{11}V_{d,ak}(t)i_{d,on}(t) + p_{02}i_{d,on}(t)^2 \quad (11)$$

where the amplitude of the reverse voltage and the forward current before the turn off interval are indicated by $V_{d,ak}$ and $i_{d,on}$, respectively.

E. DAB DC/DC converter winding powerloss

The DAB inductance current with the waveform of Fig. 4 passes through the transformer winding resistor on the primary, secondary side, and inductance. However, in battery chargers, the DC link capacitor voltage has a considerable ripple with double line frequency, especially in conventional charging methods such as CC charging. This leads to the periodic waveform with double line frequency. Hence, the conduction powerloss can be described by (12).

$$P_{DAB,win} = f_{2L} \times \sum_{n=1}^{N2} \int_0^{1/f_s} (R_{tran,p} + \left(\frac{1}{n}\right)R_{tran,s}) i_{L,DAB,n}(t)^2 dt \quad (12)$$

where the f_{2L} and $i_{L,DAB,n}$ are the double line frequency and relative DAB inductance current at step n.

F. DAB DC/DC converter conduction powerloss

In each DAB duty cycle, all the eighth switches and their body diodes are subjected to conduction powerloss. According to Fig. 4, the switch conduction loss can be calculated by (13).

$$P_{DAB,s_con} = f_s \left(\int_0^{t_1} (R_{on,S1} + R_{on,S2} + R_{on,S7} + R_{on,S8}) i_{L,DAB}(t)^2 dt + \int_{t_1}^{t_2} (R_{on,S1} + R_{on,S2}) i_{L,DAB}(t)^2 dt + \int_{t_2}^{t_3} (R_{on,S3} + R_{on,S4} + R_{on,S5} + R_{on,S6}) i_{L,DAB}(t)^2 dt + \int_{t_3}^{1/f_s} (R_{on,S5} + R_{on,S6}) i_{L,DAB}(t)^2 dt \right) \quad (13)$$

where $R_{on,Sn}$ is the on-resistor of switch number n. The body diode conduction loss can be calculated by the same approach as shown on (14).

$$P_{DAB,d_con} = f_s \left(\int_0^{t_0} (R_{on,D1} + R_{on,D2} + R_{on,D7} + R_{on,D8}) i_{L,DAB}(t)^2 dt + \int_{t_1}^{t_2} (R_{on,D5} + R_{on,D6}) i_{L,DAB}(t)^2 dt + \int_{t_2}^{t_3} (R_{on,D3} + R_{on,D4} + R_{on,D5} + R_{on,D6}) i_{L,DAB}(t)^2 dt + \int_{t_3}^{1/f_s} (R_{on,D7} + R_{on,D8}) i_{L,DAB}(t)^2 dt \right) \quad (14)$$

which $R_{on,Dn}$ is the on-resistor of the body diode of switch number n.

G. DAB DC/DC converter switching powerloss

According to Fig. 4, the DAB switches are subjected to zero current switching (ZCS) at turn on and hard switching at the turn off interval. For the same reason mentioned earlier, switching powerloss should be calculated with a double line frequency duty cycle and it is assumed that the same kind of switches used in this stage.

H. DAB DC/DC converter core powerloss

Unlike the PFC stage, the transformer inductance current does not has a sinusoidal waveform. Therefore, the Steinmetz equation can not be employed to calculate the core powerloss. In nonsinusoidal waveforms, the modified Steinmetz equation (MSE) should be used [26]. In fact, utilizing the Steinmetz equation in some cases would lead up to a 20 percent calculation error. Based on the MSE approach the core powerloss can be described by (15).

$$P_{core} = k_h \left(\frac{f_{eq}}{f_b} \right)^{\alpha-1} \left(\frac{\Delta B}{2B_b} \right)^\beta \frac{f}{f_b} \quad (15)$$

where f_{eq} is the equivalent frequency that is defined by (16) and ΔB is the average rate of charge. Identical to (10) the base frequency and flux density are assumed equal to 1 Hz and 1T.

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt} \right)^2 dt \quad (16)$$

IV. SWITCHING OPTIMIZATION

The operation of the system can be simulated with respect to space-state equations (Table 1). Fig. 10 shows the input current and voltage, DC-link voltage, DAB inductor current and output current of the system in the CC charging sinusoidal charging are shown in Fig. 11. Fig 10(a) and 11 (a) show the input current which indicates that the PFC application is realized in both charging methods. The DC-

TABLE 1
Battery Charger Specifications

Input Voltage	110 V	$F_{sw,FB}$	30 KHz
Nominal Power	1 Kw	$F_{sw,DAB}$	50 KHz
DC-link Voltage	200 V	$R_{s,on}$	0.1 Ω
R_{Load}	50 Ω	$R_{d,on}$	0.1 Ω
Switch	BUP400D	R_{tran}	10 m Ω
DAB inductance	100 μ H	$C_{DC-link}$	300 μ F
FB inductance	2 mH	L_m	200 μ H

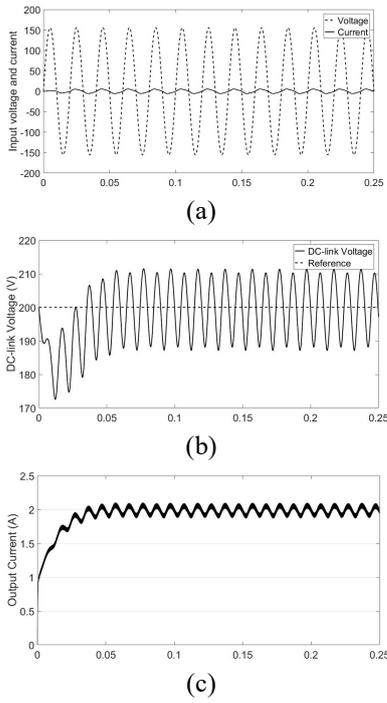


Fig. 10. Simulation results at CC mode (a) input current and voltage (b) DC-link voltage (c) output current

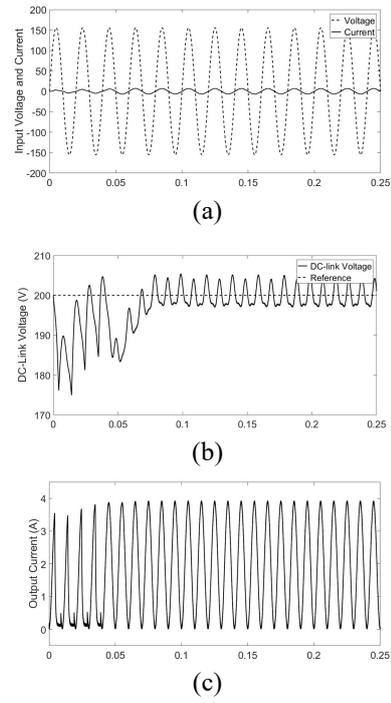


Fig. 11. Simulation results at sinusoidal mode (a) input current and voltage (b) DC-link voltage (c) output current

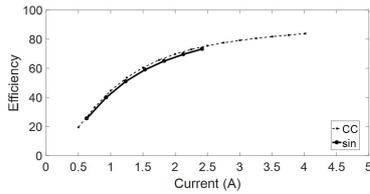


Fig. 12. Estimated efficiency of the battery charger in CC and sinusoidal charging

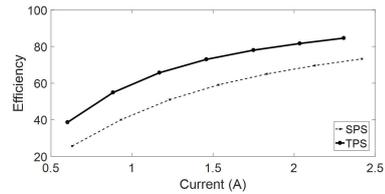


Fig. 14. Estimated efficiency of the battery charger in sinusoidal charging

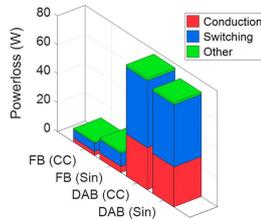


Fig. 13. The amount of powerloss of each section at each stage in CC and sinusoidal charging mode while the output current is 2A

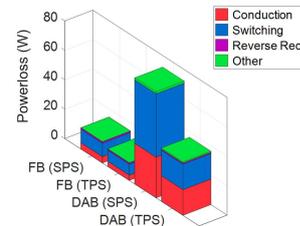


Fig. 15. The amount of powerloss of each section at each stage in sinusoidal charging SPS and TPS mode while the output current is 2A

link contains 25V voltage fluctuation in CC charging mode which is decreased to 8 V in sinusoidal charging. However, method. The simulation results for the same system at the mean of the output current is 2 A in both scenarios. As can be seen in Fig. 10(c) and 11(c), the DAB inductance current has a waveform similar to Fig. 4 and the waveform specifications are changing periodically over double line frequency duty cycle.

Fig. 12 shows the estimated efficiency of the system for a wide range of output current. As can be seen, not only sinusoidal charging results in a larger powerloss and lower efficiency, but also it comes with another vital restriction. As in the sinusoidal charging, the amplitude of the output current is two times the mean value, the charger can not operate at high output current. Consequently, in sinusoidal charging, the system operates at low output currents in which the converter has low efficiency even in the CC

charging method. In addition, the sinusoidal charging itself has a greater powerloss. The evidence of that can be found in Fig. 13 which shows the amount of powerloss of each section of each stage at 2A output current. As can be seen in Fig. 13, the majority part of the powerloss occurs in the DAB stage. Therefore, an optimizing triple phase shift (TPS) switching algorithm has been chosen to improve the efficiency of the system.

In [27] a comprehensive TPS switching algorithm for DAB converter is introduced. As the presented control algorithm doing well and covering all modes of operation of the DAB converter, this switching algorithm is selected as the optimizing switching method. Fig. 14 indicates the estimated efficiency of the system in sinusoidal charging with SPS and selected TPS mode. It can be seen that the selected optimizing algorithm shows better performance and enhances the efficiency of the system, especially at high

levels of output current. Fig. 15 shows the powerloss analysis of TPS switching comparing SPS mode. Regarding Fig. 15, the TPS algorithm decreases the DAB stage powerloss, especially the switching one. However, by utilizing this method the DAB stage will be subjected to reverse recovery loss (purple color in Fig. 15).

V. CONCLUSION

As the OBCs are installed inside the vehicle, the occupied space is an important feature. Most of the volume of the OBC relates to DC-link capacitors. As DC-link has to filter an oscillating power with double line frequency, it requires considerable capacity. Sinusoidal charging is a charging algorithm that reduces the required DC-link capacity and thereby the occupied space. However, the influences of this charging method on the performance of the charger especially on efficiency have not been analyzed before.

In this paper, the powerloss of a FB PFC DAB DC/DC battery charger analyzed comprehensively. Then, the performance of the system under sinusoidal charging investigated. Results show that the sinusoidal charging not only has higher powerloss, but also it limits the output power and pushes it toward lower output power which further results in lower efficiency. In addition, powerloss analysis indicates that the majority level of powerloss is related to the DAB stage. Therefore, an optimizing TPS switching algorithm for the DAB converter presented in recent literature is selected. By utilizing the selected TPS method the efficiency of the system is improved and the amount of the powerloss at the second stage reduced significantly.

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