Ripple-Free Input Current Flyback Converter Using a Simple Passive Circuit

Sobhan Sarani, Hossein Abootorabi Zarchi, and Hossein Delavaripour

***Abstract*—This paper proposes a new ripple canceling circuit (RCC) to eliminate the pulsating input current of the conventional flyback converter (CFC). The ripple canceling procedure occurs by two capacitors, one transformer, and a winding, which is added to the CFC transformer core. Besides, the proposed RCC acts as a passive snubber to reduce voltage spikes on the power switch of the converter. In comparison to the similar existing topologies, the proposed RCC does not employ additional semiconductors, and a lower number of magnetic components is used. The proposed RCC is verified by simulation and experimental results. The results show that using the proposed RCC, the input current ripple is reduced to 6% with the minimum power losses.**

***Index Terms*—DC-DC converter, flyback converter, ripple cancelation, semiconductors.**

I. INTRODUCTION

IN recent years, DC-DC converters have been developed significantly in many applications such as micro-inverters, battery chargers, power factor corrections (PFC), and light-emitting diode (LED) drivers, electric vehicles (EVs), etc. [1-5]. Among them, the flyback converter is very attractive because of its excellent features such as simple and compact structure, high efficiency and reliability, cost-effective, and adjustable conversion ratio [4, 5]. However, the conventional flyback converter (CFC) has some drawbacks, such as high voltage stress on the power switch and pulsating input current. These issues are the cause of the increased electromagnetic interference (EMI) and the decreased input source life span and the maximum power of the renewable sources [6, 7].

In order to compensate the input current ripple, bulky electrolyte capacitors or inductors are used as an input filter. However, these solutions induce phase shifting and have destructive effects on the efficiency, weight, volume, and dynamic of the converter [8, 9]. There is a control-based solution for compensating the mentioned phase shifting [10]. This method can improve the problem but does not entirely solve it. On the other hand, some valuable studies have been done to remove the bulky input filter and its undesirable effects. Generally, input current ripple cancelation methods are divided into two categories; techniques based on the interleaving branches and procedures based on the electromagnetic components. In the first approach, two or more branches are paralleled at the input port, and by applying a specific control strategy, the input current ripple will be eliminated [11-16]. In [14], a converter based on an interleaved boost converter is proposed. This converter provides a high voltage conversion ratio and has a low input current ripple. The input current ripple of the proposed converter is minimized by an asymmetric control strategy, and due to avoid a large surge at the input current, the duty cycle of the converter should exceed 0.5. Based on the number of interleaving branches, the input current ripple of the interleaved converter is canceled at a specific duty cycle. Hence, [15, 16] are proposed a design guide and control strategy for the interleaved branches to cancel the input current at an arbitrary duty cycle. However, the input current ripple will be increased by the variation of the duty cycle from the designed value. In order to remove the dependency of the input current ripple from the duty cycle and control strategy of the converter, the coupled inductor-based ripple cancelation techniques are proposed in the literatures. In these methods, the input current ripple is canceled by adding a network based on magnetic elements to the converter's topology [7, 17-27]. However, the input current ripple in these techniques is canceled by a particular design of the coupled inductors. In [24], a filter based on the coupled inductor is proposed to cancel the input current ripple of the DC converters. The proposed filter has a very simple structure, and it can be applied to the converters that have an input inductor. However, the ripple cancelation of this filter depends on the core geometry and designed parameters of the coupled inductor.

As mentioned above, the flyback converter has the pulsating input current, and despite the high performance of this converter, there has been less focused on the input current ripple cancelation. In [25, 26], the input current ripple of the flyback-type converters is reduced by locating an input inductor at a capacitive loop. Therefore, the input current ripple depends on the voltage ripple of the capacitors. On the other hand, galvanic isolation is eliminated in these studies. A passive pulsating ripple canceling circuit (PPRCC) is proposed in [27] to cancel the input current ripple along with maintaining the features and structure of the CFC. Two transformers and two capacitors with an additional diode

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comprise the PPRCC. This circuit has a modular structure and not only cancels the input current ripple but also reduces the voltage spikes on the power switch. Besides these significant benefits, there are some drawbacks such as complex structure, the high number of elements, and the PPRCC transformer parameters must be equal to the basic flyback transformer parameters. Therefore, the differences in the designed and implemented values of the parameters can be a challenge, which has adverse effects on the ripple cancelation methodology.

This paper proposes a circuit based on the PPRCC that saved all benefits and improved it. The proposed ripple canceling circuit (RCC) consists of a transformer, two capacitors, and an added winding to the main flyback transformer. Therefore, the proposed RCC does all the duty of the PPRCC with a lower number of elements. Nevertheless, the proposed RCC has higher efficiency and reliability.

The circuit configuration and operation principle of the proposed converter are detailed in the next section, steady-state and design of circuit parameters are analyzed in section III, and experimental results and conclusion are presented in sections IV and V, respectively.

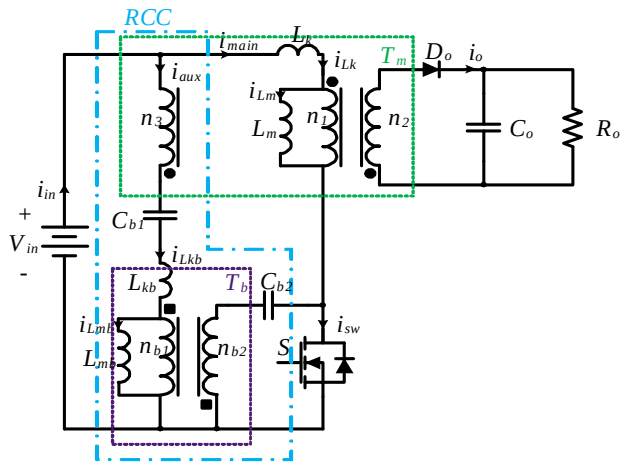

Fig. 1. Circuit configuration of proposed converter

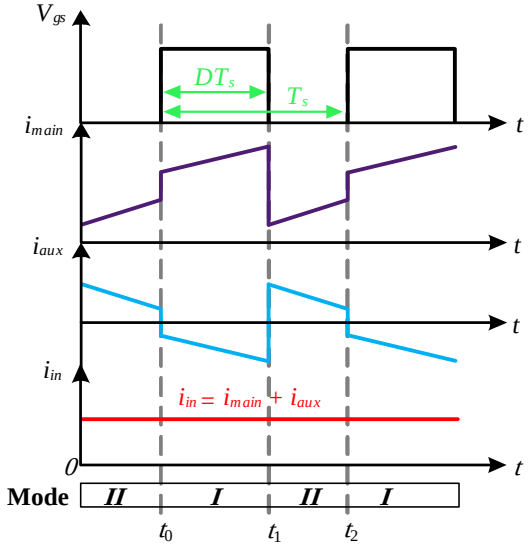

Fig. 2. Key waveform of proposed converter

II. Structure and Operation Principles

A. Circuit structure

The circuit schematic and key waveforms of the proposed converter are illustrated in Figs. 1 and 2, respectively. As shown in Fig. 1, the proposed converter consists of the CFC and auxiliary circuit that responsible for canceling the input current ripple. As mentioned in the previous section, the proposed RCC consists of two blocking capacitors (C_{b1} and C_{b2}) that block DC current, a transformer (T_b) to establish the voltage balance, and a third winding on the flyback transformer (T_m) core to reflect the current ripple of the T_m to the parallel branch of RCC. The pair of C_{b2} and T_b also operates as a passive snubber to decrease the voltage spikes on the switch S.

B. Operation of the converter

The following assumptions will be considered to simplify the description of the proposed converter operation principles.

- All semiconductors are ideal.
- All transformers modeled as a magnetizing inductor (L_m and L_{mb}) and a leakage inductance (L_k and L_{kb}) that connected series with an ideal transformer (with turns ratio n_1:n_2:n_3 and n_{b1}:n_{b2})
- All capacitors are large enough, and the voltage ripple across them is negligible.

Mode I [t_0 - t_1]: at the beginning of this mode, switch *S* is turned on. As shown in Fig. 3(a), the output diode (D_o) will be turned off, and the voltage across T_m will be equal to the input voltage source (V_{in}). Therefore, L_m and L_k will be charged, and their currents will be increased. As shown in Fig. 2, due to the existence of the blocking capacitors, only the ripple of i_{main} is mirrored to the RCC. Therefore, the auxiliary current (i_{aux}) would eliminate the ripple of i_{main}. During this mode, main circuit relationships are as follows:

$$V_{Lm} = \frac{L_m}{L_m + L_k} V_{in} \tag{1}$$

$$V_{Lk} = \frac{L_k}{L_m + L_k} V_{in} \tag{2}$$

$$V_{Lmb} = \frac{n_{b1}}{n_{b2}} V_{C_{b2}} \tag{3}$$

$$\frac{n_3}{n_1} V_{Lm} = V_{C_{b1}} + V_{Lmb} - V_{in} - V_{Lkb} \tag{4}$$

Mode II [t_1 - t_2]: In this mode, switch *S* is turned off, as shown in Fig. 3(b), the output diode is forward-biased, and the voltage across T_m is equal to the negative of the output voltage ($-V_o$). Therefore, L_m is discharged to the load, and the third winding mirrors the ripple of i_{main} to the RCC. Nevertheless, the input current will be pure DC, and input pulses will be gone. In this mode, the pair of C_{b2} and T_b provides a path to discharge the L_k. Therefore, the voltage spikes on the switch are reduced. By applying the Kirchhoff's voltage law (KVL), the following equations will be obtained:

$$V_{Lm} = -\frac{n_1}{n_2} V_o \tag{5}$$

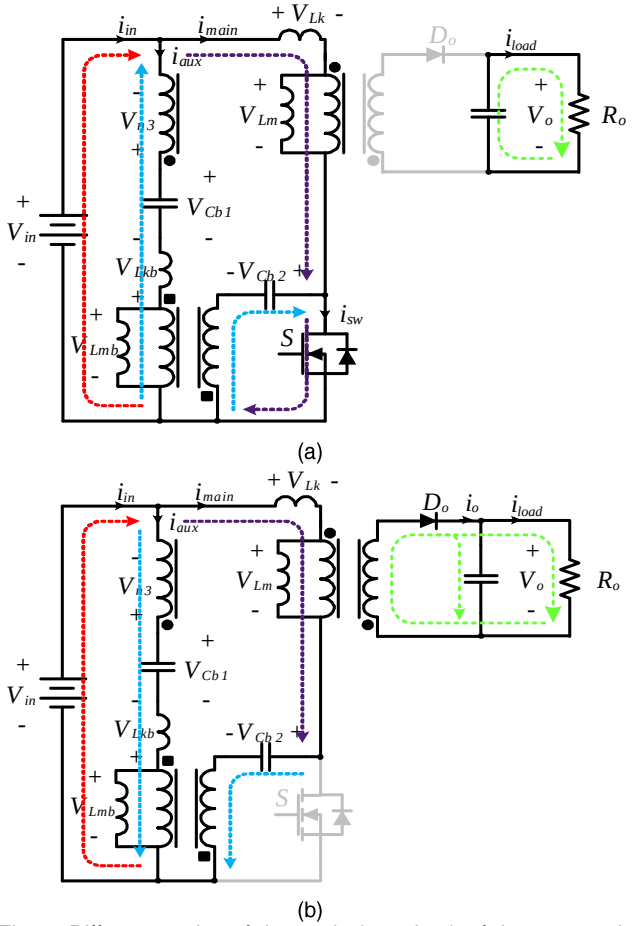

Fig. 3. Different modes of the equivalent circuit of the proposed converter. (a) mode I, (b) mode II.

$$V_{Lmb} = \frac{n_{b1}}{n_{b2}}\left(V_{C_{b2}} + V_{Lk} + V_{Lm} - V_{in}\right) \tag{6}$$

$$\frac{n_3}{n_1}V_{Lm} = V_{C_{b1}} + V_{Lmb} - V_{in} - V_{Lkb} \tag{7}$$

III. STEADY-STAT ANALYSIS

In this section, the voltage conversion ratio, the average voltage on blocking capacitors, the input current ripple cancelation requirements, and the current stress on semiconductor devices will be analyzed in detail.

A. Voltage conversion ratio

As voltage drop on leakage inductances is negligible, V_{Lk} and V_{Lkb} will be ignored. Therefore, the voltage conversion ratio can be obtained by applying the volt-second balance principle on L_m. According to (1) and (5):

$$M = \left(\frac{n_{21}D}{1-D}\right) \tag{8}$$

Where D is the duty ratio, and n_{21} represents n_2/n_1. From (8), it can be concluded that the voltage gain of the proposed converter is equal to the CFC, and the proposed RCC does not affect the voltage gain.

Considering the volt-second balance principle on L_{mb} and from (3), (5), (6), and (8), becomes:

$$V_{C_{b2}} = V_{in} \tag{9}$$

According to (3)-(9) and applying the volt-second balance principle on L_m, the average voltage on C_{b1} can be derived as

$$V_{C_{b1}} = V_{in} \tag{10}$$

B. Input current ripple cancellation requirements

For achieving ripple-free input current, the amplitude ripple of i_{main} and i_{aux} must be equal as follows.

$$\left|\frac{di_{main}}{dt}\right| = \left|\frac{di_{aux}}{dt}\right| \tag{11}$$

By considering (11) and transformer relationships on T_m, the current ripple on L_m can be defined as follows.

$$\frac{di_{Lm}}{dt} = \left(\frac{n_1+n_3}{n_1}\right)\frac{di_{main}}{dt} \tag{12}$$

From (1), (2), (11), and (12) in mode I, it can be obtained:

$$\left[L_k + L_m\left(\frac{n_1+n_3}{n_1}\right)\right]\frac{di_{main}}{dt} = V_{in} \tag{13}$$

Moreover, from (3), (4) and (9)-(12) in mode I, becomes:

$$\left(\frac{n_{b2}}{n_{b1}}\right)\left[L_{kb} + L_m\left(\frac{n_3}{n_1}\right)\left(\frac{n_1+n_3}{n_1}\right)\right]\frac{di_{main}}{dt} = V_{in} \tag{14}$$

Therefore, (13) and (14) will be equal if only if the proposed RCC satisfies the following conditions.

$$\begin{cases} n_3 = n_1 \\ n_{b1} = n_{b2} \\ L_k = L_{kb} \end{cases} \tag{15}$$

The same results will be similarly obtained in mode II.

From (15), it can be concluded that the input current ripple cancelation requirements do not depend on n_2, L_m, and L_{mb}. Therefore, in comparison with the PPRCC, the proposed RCC has a lower dependency on the flyback transformer parameters.

C. Inductor and semiconductor currents

As mentioned in the previous sections, the average current of the RCC is equal to zero because of the blocking capacitors. Therefore, the average current of i_{main} will be equal to I_{in}. Hence, from (1), the peak value of i_{main} can be calculated as (16).

$$I_{main}^{peak} = \frac{3I_{in}}{4D} + \frac{V_{in}DT_s}{2(L_m + L_k)} \tag{16}$$

The average value of the auxiliary current in each operation mode of the converter can be obtained by applying the Kirchhoff's Current law (KCL) in Fig. 3 and considering (15).

$$I_{aux}^{Mode\ I} = \frac{I_{in} - I_{Lm}}{2} \tag{17}$$

$$I_{aux}^{Mode\ II} = \frac{I_{in} - I_{Lm} + n_{21}I_o}{2} \tag{18}$$

By considering (17), (18), and applying the ampere-second balance law on C_{b1} the average magnetizing current of T_m is calculated as (19).

$$I_{Lm} = \frac{I_{in}}{D} \tag{19}$$

Therefore, the proposed RCC does not affect the average magnetizing current of the conventional flyback converter, but it reduces the peak current of the leakage inductance of T_m, which leads to reduce the stored energy on L_k and voltage spikes on the switch.

The current stress of semiconductor devices can be calculated from their current ripple and their average conductive current. Therefore, from (5), (11), and (15) in mode II, the current ripple on L_m can be defined as follows.

$$\frac{di_{Lm}}{dt} = \frac{di_o}{dt} = -\frac{V_o}{n_{21}L_m} \tag{20}$$

Therefore, the current stress on the output diode can be calculated from (20) and the average output current.

$$i_{o,\max} = \frac{P_o}{(1-D)V_o} + \frac{(1-D)V_o}{2n_{21}L_m}T_s \tag{21}$$

Where T_s represented the switching period.

In mode I, the ripple of the switch current is equal to (22).

$$\frac{di_{sw}}{dt} = \frac{n_{b2}}{n_{b1}}\left(\frac{di_{aux}}{dt} + \frac{di_{Lmb}}{dt}\right) + \frac{di_{main}}{dt} \tag{22}$$

Therefore, from (3), (9), (11), (12), (15), and (22), the switch current ripple can be summarized as (23).

$$\frac{di_{sw}}{dt} = V_{in}\left(\frac{1}{L_m} + \frac{1}{L_{mb}}\right) \tag{23}$$

As T_b is located between C_{b1} and C_{b2}, the current ripple of L_{mb} is negligible, and as mentioned before, the average of i_{aux} is almost zero. Therefore, the average of i_{sw} and i_{in} are equal. Accordingly, from (8) and (23), the current stress on S is calculated by (24).

$$i_{sw,\max} = \frac{n_{21}DP_o}{(1-D)V_o} + \frac{(1-D)V_o}{2n_{21}L_m}T_s \tag{24}$$

The total average and peak of switching device power (SDP_{avg} and SDP_{pk}) provide an appropriate comparison for the price and requirements of the converters semiconductors [28] that defined as (25).

$$\begin{cases} SDP_{pk} = \sum_{i=1}^{N} V_i^{pk} I_i^{pk} \\ SDP_{avg} = \sum_{i=1}^{N} V_i^{pk} I_i^{avg} \end{cases} \tag{25}$$

Where N represented the total number of semiconductor devices. From (25), the SDP of the proposed converter can be calculated as (26).

$$\begin{cases} SDP_{pk} = \frac{P_o}{n_{21}D} \times \left[1 + \frac{n_{21}}{1-D} + \frac{(1-D)\left(1-(1-0.5n_{21})D\right)}{n_{21}L_m R_o}T_s\right] \\ SDP_{avg} = \frac{P_o}{n_{21}D}\left[1-(1-2n_{21})D\right] \end{cases} \tag{26}$$

IV. Design Procedure

In this section, the design procedure of the passive components will be discussed. The magnetizing inductance of the coupled inductors are calculated based on their average current and considering an acceptable current ripple. Therefore, from (19) and considering the acceptable magnetizing current tolerant as β% of its average value, the magnetizing inductance of T_m is calculated as (27).

$$L_m = \frac{V_{in}D^2}{\beta\% I_{in}}T_s \tag{27}$$

As T_b is located in series with the blocking capacitors, its average magnetizing current and its stored energy are almost zero. Therefore, by considering (3), (9), and (15), the magnetizing inductance of T_b is calculated based on its current ripple.

$$L_{mb} = \frac{V_{in}D}{\Delta i_{Lmb}}T_s \tag{28}$$

Where, Δi_{Lmb} is the peak to peak magnetizing current of T_b.

From (17) to (19), the capacitance of the blocking and output capacitors are calculated by assuming their voltage ripple as γ% of the input voltage source.

$$C_{b1} = C_{b2} = \frac{(1-D)I_{in}}{2\gamma\% V_{in}}T_s \tag{29}$$

$$C_o = \frac{DI_{in}}{\gamma\% M^2 V_{in}}T_s. \tag{30}$$

V. Experimental Results and Comparison

A brief comparison between some ripple cancelation studies is reported in Table I. It can be concluded that the proposed converter cancels the input current ripple with a lower number of elements and design requirements, which leads the more accuracy in the implementation of the ripple cancelation methodology.

A laboratory-scale of the proposed RCC is built whose electrical parameters are reported in Table II. The laboratory prototype is shown in Fig. 4. The CFC and the PPRCC also are implemented with similar parameters to compare with the proposed RCC. The duty ratio of the converters is set to 0.5.

The waveform of the input current (i_{in}), main current (i_{main}), and auxiliary current (i_{aux}) are shown in Fig. 5. The figure confirms that i_{aux} can compensate the ripple of i_{main}, results in the input current of the converter becomes ripple-free. As shown in Fig. 6, the output voltage and the average voltage on blocking capacitors are equal to 30 V approximately, which confirm the theoretical analysis in (9) and (10).

The input current ripple and the voltage spikes on the switch of the converters are compared in Fig. 7. As can be seen, the voltage spikes in the RCC and PPRCC are the same approximately, and the input current ripple is decreased to 6% and 9% of the average input current, respectively. The remained ripple in the input currents is due to voltage ripple across the blocking capacitors and the mismatches between the implemented parameters and ripple cancelation requirements. On the other hand, the CFC has a pulsating input current with a ripple of 2.2 times of the average input current and high voltage spikes on the power MOSFET. Therefore, the proposed RCC reduces the input current ripple of the CFC more than two times of the average input current. The FFT analysis for the input current ripple of the proposed

TABLE I
COMPARISON AMONG SOME RIPPLE-FREE CONVERTERS

description	The proposed converter	Converter of [27]	Converter of [17]	Converter of [7]	Converter of [18]	Converter of [19]
Basic converter	Flyback	Flyback	Boost	CUK	Boost	Isolated SEPIC
No. of semiconductors	2	3	2	2	2	3
No. of magnetics components	2	3	3	4	2	3
No. of capacitors	3	3	2	4	2	3
Modular structure	No	Yes	Yes	Yes	No	No
Related parameters for ripple cancelation	Turns ratio, Leakage inductances	Turns ratio, Leakage inductances, Magnetizing inductances	Turns ratio, Leakage inductances, Magnetizing inductances	Turns ratio, Magnetizing inductances	Turns ratio, Magnetizing inductances	Turns ratio, Magnetizing inductances

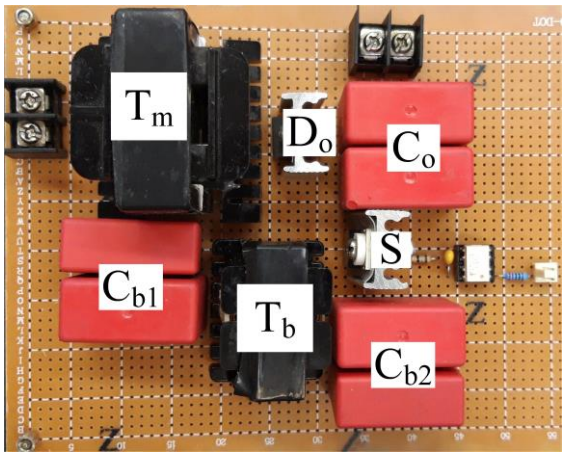

Fig. 4. Implemented flyback converter with the proposed RCC

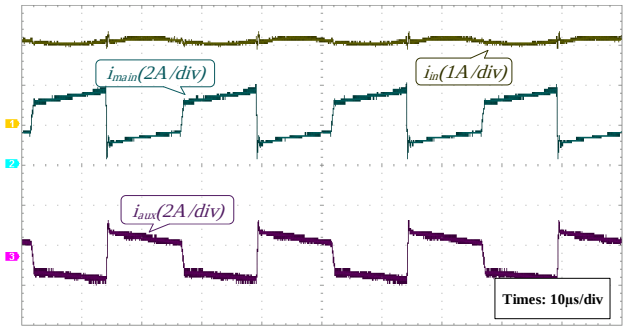

Fig. 5. Input current (i_{in}), main current (i_{main}) and auxiliary current (i_{aux}) waveforms.

converter and the conventional flyback converter are given in Fig. 8. As can be seen, the proposed converter approximately has a DC value, and the input current harmonics in the conventional flyback converter are reduced effectively with the help of the proposed RCC. Furthermore, a MOSFET with a lower voltage rating can be used as the switch of the proposed converter, due to voltage spike across the switch is reduced in the proposed converter.

The measured efficiencies of the converters are compared in Fig. 9. The proposed converter efficiency is about 84.2% at nominal output power, and the efficiency of the CFC and the PPRCC is 84.9% and 83.5%, respectively.

TABLE II
CIRCUIT PARAMETERS OF THE IMPLEMENTED CIRCUITS

	Parameters	RCC	PPRCC	CFC
	Output power (P_o)	65 W	65W	65W
	Input voltage source (V_{in})	30 V	30 V	30 V
	Switching frequency (f_s)	40 KHz	40 KHz	40 KHz
	Output voltage (V_o)	30 V	30 V	30 V
Flyback transformer (T_m)	Turn ratio	1:1:1	1:1	1:1
	Magnetizing inductance	431 µH	431 µH	431 µH
	Leakage inductance	15.04 µH	15.04 µH	15.04 µH
Balancing transformer (T_b)	Turn ratio	1:1	1:1	---
	Magnetizing inductance	3.26 mH	3.3 mH	---
	Leakage inductance	14.8 µH	1.2 µH	---
Auxiliary transformer	Turn ratio	---	1:1	---
	Magnetizing inductance	---	431.6 µH	---
	Leakage inductance	---	14.6 µH	---
	Blocking capacitors (C_{b1}, C_{b2})	37 µF	37 µF	---
	Output capacitor (C_o)	44 µF	44 µF	44 µF
	Switch	Spw20n60c3	Spw20n60c3	Spw20n60c3
	Output diode(s)	BYV32-200-D	BYV32-200-D	BYV32-200-D

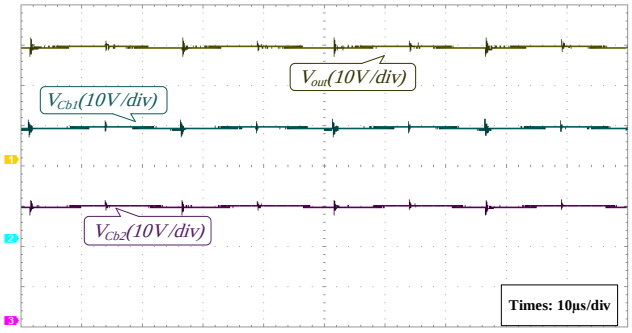

Fig. 6. Output voltage and average voltage on blocking capacitors.

To compare the semiconductor rating and losses, the SDP_{pk} and SDP_{avg} are calculated for each converter, and the results are shown in Fig. 10. As can be seen, the SDP_{avg} is equal in the converters, but the SDP_{pk} in the proposed RCC is lower than the PPRCC, which means with the same semiconductor ratings, the proposed RCC has lower losses in the semiconductors. Also, it can be concluded that the proposed RCC does not affect the voltage and current stress of the flyback converter semiconductors.

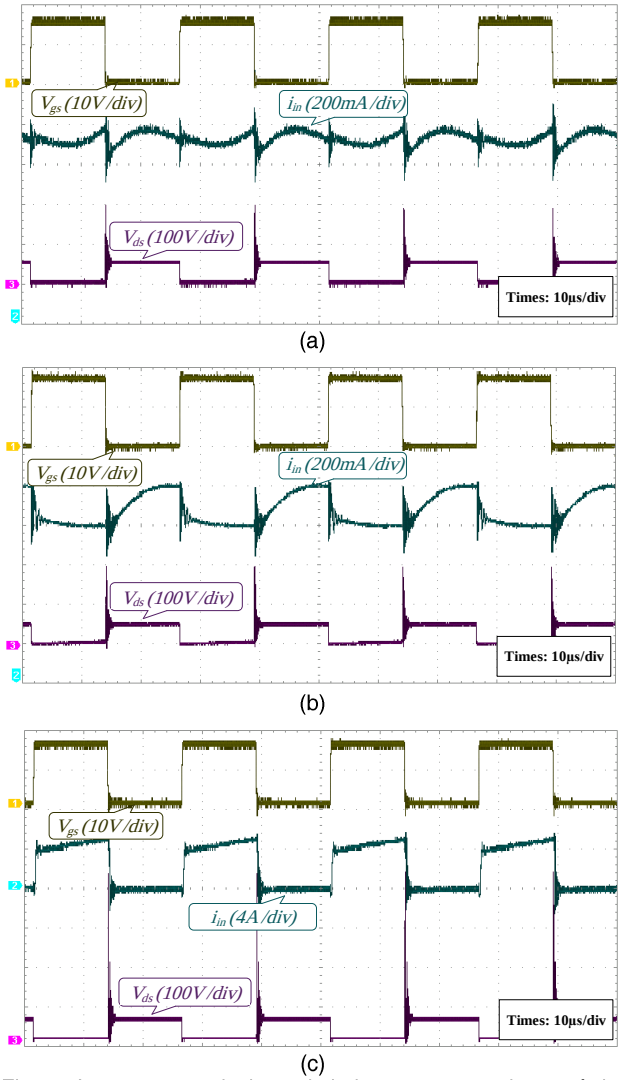

Fig. 7. Input current ripple and drain to source voltage of the switch by the: (a) proposed RCC, (b) PPRCC, (c) CFC.

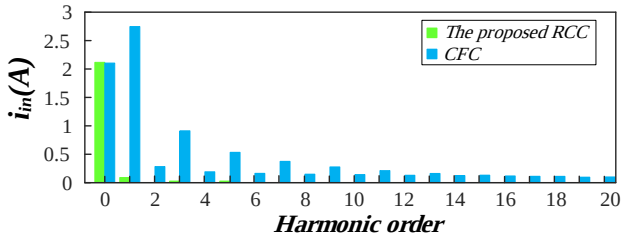

Fig. 8. Input current harmonics amplitude of the proposed converter and the conventional Flyback converter.

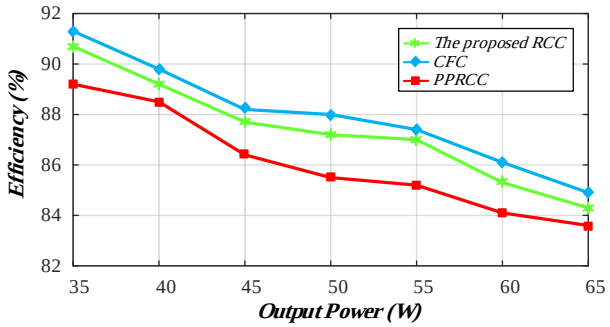

Fig. 9. Efficiency comparison of the converters

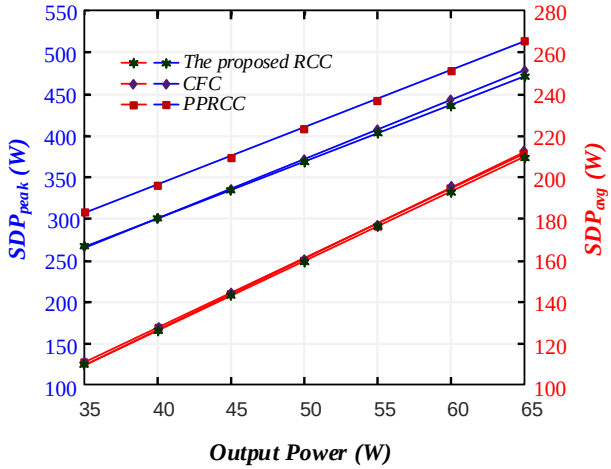

Fig. 10. Peak and average SDP of the converters.

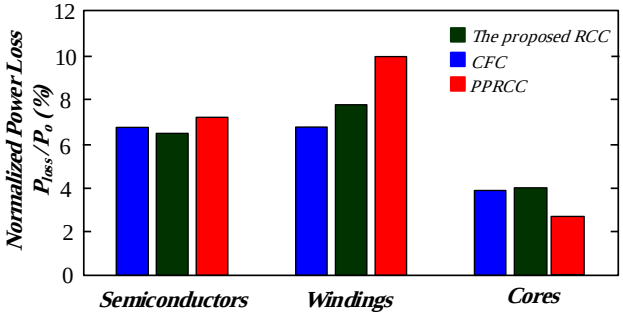

Fig. 11. Distribution of the total power losses

In order to fair comparison and comprehensive analysis of the power losses, the method used in [29, 30] has been exploited, and the converters are simulated with PSIM software. The loss distribution of the converters is shown in Fig. 11. As discussed previously, because the proposed RCC

has less diode and transformer, the semiconductor and winding losses in the proposed RCC are smaller than PPRCC. On the other hand, the PPRCC provides a second path to supply the load. Therefore, the peak magnetizing current of T_m is reduced, and consequently, the core loss is reduced in this converter.

VI. Conclusion

In this paper, a ripple canceling circuit for the flyback converter was proposed, causes ripple-free input current. Therefore, the input filter could be removed completely, which was essential for this converter. The proposed RCC has fewer elements in comparison with previous studies. As discussed, the proposed RCC saves all excellent features of the CFC, but eliminates the pulsating input current and reduce the voltage spikes on the switch of the CFC, with the same conversion efficiency and current stresses on the semiconductor devices approximately. The results showed that by using the proposed RCC, the peak-to-peak input current could be reduced to 6% of its average value, and a 0.7% improvement could be obtained in the conversion efficiency in comparison with previous studies.

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