An Isolated High Boost Ratio DC-DC Converter with Very Low Input Current Ripples

Sobhan Sarani, Ali Nikbahar, Hossein Abootorabi Zarchi, and Xiaodong Liang, *Senior Member*, *IEEE*

***Abstract* —This paper proposes an isolated DC-DC converter with a highly flexible voltage gain, which can be adjusted by three independent parameters. The proposed converter also offers the smooth input current, a simple structure and high efficiency. The only switch of the converter experiences extremely low voltage spikes; its output diode works under the zero current switching (ZCS), leading to reduced switching losses and overall converter costs. Low magnetizing current of coupling inductors and low voltage stress of capacitors of this converter indicates its high power density. The input current ripple reduction technique is independent of the coupling factor and can be easily implemented in the converter. The operating principle and parameter design guideline of the proposed converter are explained in detail, and its performance is compared with two existing DC-DC converters. To further validate the proposed converter, a 400 W prototype is built and tested in the laboratory.**

***Index Terms*—DC-DC converter, electrical isolation, high-voltage gain, input current ripple reduction.**

I. Introduction

High-gain DC-DC converters are widely used in low-voltage resources, such as solar and battery storage systems. High efficiency, reliability, and safety are the main crucial factors for the system operation. The galvanic isolation is recommended to solve safety and grid leakage current problems [1], which can reduce the imposition of input perturbations to the output, and protect the input source against short-circuit currents on the load side [2]. Input current ripples of converters may reduce the efficiency and shorten the lifespan of the system [3, 4]. Bulky filters are traditionally used to mitigate input current ripples, but such filtering makes the converter oversized with low efficiency. Therefore, many studies have attempted to offer alternative methods to reduce input current ripples [5].

To address these issues, a family of high-gain DC-DC converters with low input current ripples is introduced in [6]. These topologies utilize a capacitive loop to reduce input current ripples with an input inductor located in the capacitive loop. Therefore, the voltage across the inductor is almost zero, restricting input current variations. The topology in [6] is shown in Fig. 1 (a), where the capacitive loop is in pink. In this converter, a voltage doubler stage is added to the output side, and an active clamp technique is used to suppress voltage spikes on the main switch. A high-gain DC-DC converter with low input current ripples is proposed in [7], the high gain is achieved by the switched-inductor and switched-capacitor cells, and low input current ripples are achieved through a capacitive loop. Despite benefits of these converters, their MOSFETs do not have a common source, which increases their complexity and costs. The capacitive loop links the input to the output, which is more beneficial for non-isolated applications. Although the capacitive loop technique offers a simple way to smooth input currents, an additional discrete input inductor is required to cancel input current ripples, leading to a relatively low power density converter. As a step forward, a ripple canceling circuit (RCC) is proposed in [8] to cancel pulsating input current ripples and keep the galvanic isolation in conventional flyback converters. Fig. 1(b) shows a RCC that comprises a transformer, a winding that is added to the flyback's coupled inductor, and two capacitors. Voltage spikes across the switch in [8] are also improved. In [9], an input current ripple canceling circuit for a family of impedance source DC-DC converters is introduced, which includes an inductor, a capacitor, and an added winding to the coupled inductor in the basic topology, similar to the RCC. A simple auxiliary circuit consisting of a coupled inductor and a capacitor is introduced in [10] to eliminate the input current ripple of the boost converter. Converters in [8, 9] offer an advanced and efficient solution to cancel input current ripples by using multipurpose magnetic cores. However, except the number of elements and the volume of converters, other features of these basic topologies, such as the voltage gain, remain the same. Their current ripple-canceling approaches also depend on the coupling factor and turn ratio of the coupled inductor. Since the coupling coefficient is a critical factor for the input current ripple cancellation in these studies, it is challenging to accurately implement their ripple cancellation techniques. A high-voltage gain converter based on a coupled inductor is proposed in [11]. This converter adds a coupled inductor in a voltage lift cell, providing a flexible high-voltage gain that can be adjusted by the turn ratio of the coupled inductor and the duty ratio of its single switch; however, it has high input current ripples. The interleaved structure is a promising solution to reduce input current ripples, the current stress on elements, and the total harmonic distortion in AC-DC converters [12]. However, the input current ripple reduction in interleaved converters can be affected by the input inductance mismatch at each phase and the converter operation point [13]. A high-gain isolated converter is proposed by interleaving a current doubler and a resonant half-bridge [14], an active clamp is used to suppress voltage spikes on switches, and input current ripples become zero when the duty ratio of switches on the primary side is 0.5. Due to the two current paths in this converter, its elements experience relatively low stresses, but the converter has a complex structure and control strategy.

In this paper, an isolated DC-DC converter with a flexible high voltage gain and very low input current ripples is proposed; it also has a simple structure, high power density, and

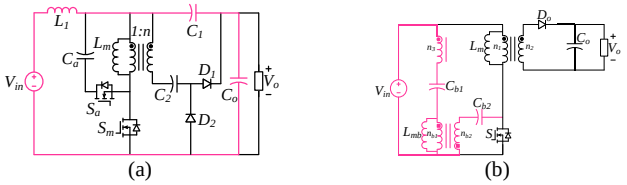

Fig. 1. The circuit diagram of (a) converter in [6] and (b) converter in [8].

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high efficiency. The input current ripple reduction method is realized through the coupled inductor and its performance only depends on the inductor's turn ratio, which is easy to implement. Capacitors in the circuit keep the voltage across the switch at an almost constant value, and voltage spikes are effectively reduced. The output diode operates in the zero current switching (ZCS) mode. The magnetizing current requirement and the voltage stress across the capacitors of the converter are relatively low. In summary, the proposed converter has the following improvements compared to the converters in [6] and [8]: 1) a lower volume due to its lower reactive component volume, 2) a higher efficiency, 3) a minimum dependency on the circuit design parameters for the input current ripple reduction methodology, 4) providing the galvanic isolation, and 5) a higher voltage gain, and thus, a lower voltage stress on its single switch.

II. Topology and Operation Principles

The circuit structure of the proposed converter is shown in Fig. 2(a), consisting of two coupled inductors (T_1 and T_2), four capacitors (C_1, C_2, C_3, and C_o), and two diodes (D_1, and D_o). To explain its operating principle, it is assumed that the converter is working in the continuous conduction mode (CCM), and the two coupled inductors, T_1 and T_2, are modeled by the magnetizing inductances (L_{m1} and L_{m2}) and leakage inductances (L_{k1} and L_{k2}), and as ideal transformers with n_1:n_2:n_3 and a_1:a_2 turn ratios, respectively. Fig. 2 shows equivalent circuits of operating modes and key waveforms.

A. Operating principle

Fig. 2(d) shows that the proposed converter has two operating modes, as described below.

Mode I [$t_0 - t_1$]: In this mode, *SW* is turned ON by setting its gate pulse to the high logic level. D_1 is blocked and D_o is forward-biased. The equivalent circuit of the proposed converter in this mode is shown in Fig. 2(b). Figs. 2(b) and 2(d) indicate that T_1 directly forwards energy from the input source to the output load. Adversely, the stored energy in T_2 is discharged to the output load. By applying Kirchhoff's voltage and current laws (KVL and KCL) in this mode, we have

$$V_{Lm1} = \frac{n_1}{n_3} V_{C1} \tag{1}$$

$$V_{Lm2} = \frac{a_1}{a_2}\left(V_{C3} + \frac{n_2}{n_3} V_{C1} - V_o\right) \tag{2}$$

$$I_{C3} = \frac{-I_o}{D} \tag{3}$$

$$I_{C2} = I_{Lm2} - \frac{a_2}{a_1}\frac{I_o}{D} \tag{4}$$

$$I_{C1} = \frac{n_1}{n_3}(I_{Lm1} - I_{in}) - \frac{n_2}{n_3}\frac{I_o}{D} \tag{5}$$

where D is the duty cycle of the switch.

Mode II [$t_1 - t_2$]: As shown in Fig. 2(c), Mode II starts when *SW* is turned OFF, while D_1 and D_o are forward-biased and reverse-biased, respectively. Complementary to Mode I, T_1 delivers its energy to capacitors, while T_2 is charged (Fig. 2(d)). By applying KVL and KCL in the equivalent circuit and applying the ampere-second balance law on capacitors, the main equations of Mode II are obtained as follows:

$$V_{L_{m1}} = -\frac{n_1}{n_2} V_{C3} \tag{6}$$

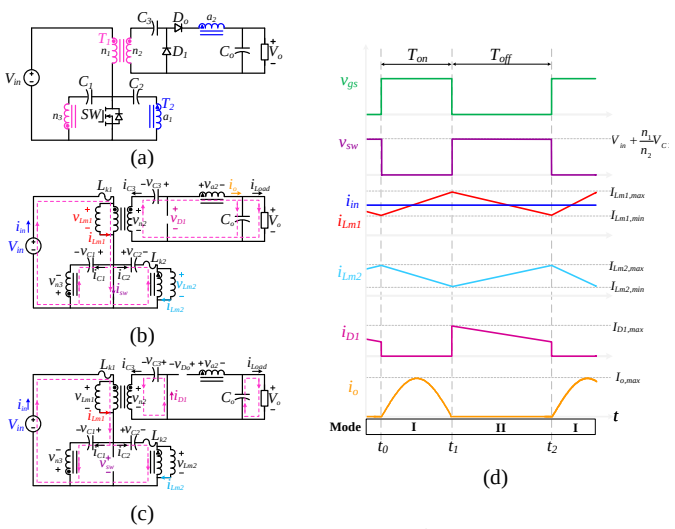

Fig. 2. The circuit diagram and operating modes of the proposed converter: (a) The circuit diagram, (b) Mode I, (c) Mode II, (d) Key waveforms.

$$V_{Lm2} = \frac{n_3 L_{m2} V_{C3}}{n_2 (L_{m2} + L_{k2})} \tag{7}$$

$$I_{C3} = \frac{I_o}{(1-D)} \tag{8}$$

$$I_{C2} = I_{Lm2} \tag{9}$$

$$I_{C1} = \frac{n_1}{n_3}(I_{Lm1} - I_{in}) - \frac{n_2}{n_3}\frac{I_o}{(1-D)}. \tag{10}$$

In this mode, the second winding of T_1 is in parallel with C_3. As a result, the voltage across the third winding of T_1 is equal to $n_{32}V_{C_3}$. C_1 and C_3 can thus prevent high voltage spikes on the switch.

B. Voltage Conversion Ratio

Based on the volt-second balance law, the average voltage across inductors equals to zero during a switching period. Therefore, as shown in Figs. 2(b) and 2(c), the average voltages across C_1 and C_2 are equal to the input voltage source.

$$V_{C1} = V_{C2} = V_{in}. \tag{11}$$

Thus, by applying the volt-second balance law on L_{m1} and considering (1), (6), and (11), the voltage across C_3 is

$$V_{C3} = \frac{n_{23} D}{1-D} V_{in} \tag{12}$$

By applying the volt-second balance law on L_{m2} and considering (2), (7), and (12), the voltage gain is obtained as follows:

$$M = \frac{n_{23}}{1-D} + a_{21}. \tag{13}$$

Where $n_{23} = n_2/n_3$, and $a_{21} = a_2/a_1$. This equation shows that the desired voltage gain can be obtained by adjusting three independent parameters, n_{23}, a_{21} and D, providing more flexibility in the converter design.

III. Design Procedure

In this section, the design guideline for elements of the converter is provided. The voltage across and the current flowing through active and passive components of the converter are calculated to determine their ratings.

A. Input Current Ripple Reduction

In the proposed converter, the third winding of T_1 and C_1 are responsible for the near zero-ripple input current. To achieve this goal, the following equation should be satisfied:

$$\frac{di_{in}}{dt}=\frac{di_{Lk1}}{dt}=\frac{V_{Lk1}}{L_{k1}}=0 \tag{14}$$

In Fig. 2(d), the voltage across L_{k1} in Modes I and II can be calculated by (15) and (16), respectively.

$$V_{Lk1}^{I}=V_{in}-V_{Lm1}=V_{in}-\frac{n_1}{n_3}V_{C1} \tag{15}$$

$$V_{Lk1}^{II}=(n_3-n_1)\frac{V_{C3}}{n_2} \tag{16}$$

Accordingly, the simple constraint that guarantees the input current ripple cancellation is

$$n_1=n_3. \tag{17}$$

i.e., the ripple reduction only depends on n_3, and the voltage gain of the proposed converter with the low-ripple input current is modified as follows:

$$M=\frac{n_{21}}{1-D}+a_{21}. \tag{18}$$

As the voltage across L_{k1} is equal to zero, not only the input current ripples are effectively reduced, but the leakage inductance problem is also minimized. Therefore, as a critical parameter in the design of magnetic components, the coupling coefficient is not challenging for T_1. The stored energy in the leakage inductance is considerably decreased, so voltage spikes on the switch are also decreased accordingly.

B. Passive Elements Design

By applying the ampere-second balance law on the capacitor's current and considering (3) to (5) and (8) to (10), the average magnetizing currents are calculated by

$$I_{Lm1}=I_{in} \tag{19}$$

$$I_{Lm2}=\frac{a_{21}I_{in}}{M}. \tag{20}$$

To obtain the desired magnetizing current ripple, a proper inductance must be designed considering the voltages across the inductor during its charging/discharging and the dwell time. Based on (1), (2), and (18) to (20), the magnetizing inductances, L_{m1} and L_{m2}, can be expressed by

$$L_{m1}=\frac{V_{in}}{\beta\%I_{in}}DT_s \tag{21}$$

$$L_{m2}=\frac{MV_{in}}{\beta\%a_{21}I_{in}}DT_s \tag{22}$$

Where T_s and β are the switching period and acceptable ripples of the magnetizing current, respectively.

An adequate capacitance should be determined based on the current and the dwell time for tolerable voltage ripples. Consequently, by considering the average current of L_{m1} and L_{m2} in (19) and (20), the capacitance of C_1, C_2, and C_3 are

$$C_1=\frac{n_{21}I_{in}T_s}{\gamma\%MV_{in}} \tag{23}$$

$$C_2=\frac{a_{21}(1-D)I_{in}T_s}{\gamma\%MV_{in}} \tag{24}$$

$$C_3=\frac{(1-D)I_{in}T_s}{n_{21}\gamma\%MDV_{in}} \tag{25}$$

where γ represents acceptable voltage ripples of the capacitor.

C. Active Elements Design

The voltage stresses on D_1, D_o and SW are calculated by

$$V_{D1}=\frac{n_{21}}{1-D}V_{in} \tag{26}$$

$$V_{Do}=\frac{n_{21}+a_{21}}{1-D}V_{in} \tag{27}$$

$$V_{sw}=\frac{1}{1-D}V_{in}. \tag{28}$$

As shown in Fig. 2(d), the maximum current of D_1 can be calculated by

$$I_{D1,\max}=n_{12}(I_{Lm1,\max}-I_{Lm2,\min})=\frac{2L_cP_o+V_{in}^2n_{12}D(1-D)MT_s}{2L_cV_{in}(1-D)M} \tag{29}$$

where P_o is the output power, and L_c is the equivalent of the magnetizing inductance defined as $L_c = L_{m1}L_{m2}/(L_{m1}+L_{m2})$. The current of D_o is equal to i_o, and its maximum value is

$$I_{Do,\max}=I_{o,\max}=\frac{\pi P_o}{2V_{in}DM}. \tag{30}$$

By applying KCL in Mode I, the maximum switch current is calculated by

$$I_{sw,\max}=\frac{n_{21}P_o}{V_{in}(1-D)M}+(n_{21}+a_{12})I_{o,\max}. \tag{31}$$

D. Zero Current Switching

The output diode of the proposed converter can operate under ZCS, leading to an effective reduction of switching losses. A half-cycle resonant between passive components of the converter should be complete before the end of *Mode I*. To simplify the analysis, the effect of magnetizing inductances is ignored compared to capacitors and leakage impedances. The equivalent circuit of the converter in *Mode I* can be simplified as Fig. 3 with all components' parameters referred to the output side. Therefore, to achieve ZCS, Eq. (32) must be satisfied, where C_t is the equivalent capacitor defined by (33).

$$2f_r=\frac{1}{\pi}\sqrt{\left(\frac{1}{(L_{k2}'C_t)}\right)}>\frac{f_s}{D} \tag{32}$$

$$C_t=\frac{C_1'C_2'C_3C_o}{C_1'C_2'C_3+C_1'C_2'C_o+C_1'C_3C_o+C_2'C_3C_o} \tag{33}$$

Where C_1', C_2', and L_{k2}' are determined by $n_{32}^2C_1$, $a_{12}^2C_2$, and $a_{21}^2L_{k2}$, respectively.

IV. Comparison with Existing DC-DC Converters

The proposed converter is compared with two existing DC-DC converters in [6] and [8]. The switch in the proposed converter is directly connected to the negative node of the input voltage source, so an extra isolated power supply is not needed, showing a cost-effective feature. Although the proposed converter uses one more capacitor than the converter in [8], it provides a higher voltage gain, leading to smaller duty ratios. The input current ripple reduction in the proposed converter has the minimum parameter dependency compared to the converter in [8], resulting in the simpler implementation and improved reliability. The leakage inductance does not appear in the design procedure of the proposed converter, but the voltage gain in [6] and the current ripple cancellation in [8] show a direct relation with the coupling coefficient. The galvanic isolation in the proposed converter and the converter in [8] is an attractive feature, when the electrical isolation between the input and the output is required. For a fair comparison, the graphical analyses

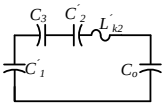

Fig. 3. The simplified equivalent circuit of the converter during Mode I, referred to the output side.

between the proposed converter and the converters in [6] and [8] are shown in Fig. 4 with all turn ratios assumed equal to *n*.

A. *Voltage gain*

The voltage gain of the proposed converter and the existing converters in [6] and [8] versus the duty cycle and the turn ratio, are shown in Fig. 4(a). The proposed converter offers a higher voltage gain in almost all ranges of control parameter variations. The turn ratios play a more critical role in the voltage gain characteristics of the proposed converter than the two existing converters. The proposed converter uses turn ratios of the two coupled inductors, T_1 and T_2, to boost its input voltage, providing more degrees of freedom in the design. The two coupled inductors play an essential role in reducing input current ripples and switching losses. In contrast, the two existing converters add a magnetic element to the converter topology for the ripple cancellation purpose only.

B. *Voltage stress of active switches*

For the same voltage gain, the switch of the proposed converter experiences the lowest voltage stress among the three converters due to a lower duty cycle requirement with considerably decreased switching spikes, so a lower-rating MOSFET with a lower $R_{ds(on)}$ can be used. Conduction losses of the switch can thus be reduced, and its efficiency improved.

C. *The Volume of reactive components*

The volume of reactive components is directly determined by their stored energy, which can be estimated through the average voltage across capacitors and the average current of inductors [15,16]. The normalized total values of these parameters are compared in Figs. 4(b) and 4(c), respectively. It can be deduced that capacitors in the proposed converter experience a lower voltage stress, especially than that in the converter in [6]. The lowest total magnetizing current is another attractive feature of the proposed converter. As a result, at the same power rating, the volume of reactive components is low, and the proposed converter has a high power density.

V. Practical Evaluation

To validate the proposed converter's performance, a 400 W prototype is built in the lab (Fig. 5(*a*)). The prototype is designed with the maximum voltage ripple of capacitors equal to 10%, and the magnetizing current ripple of inductors equal to 50%. Table I summarizes main parameters of the prototype and the test conditions. For the voltage gain of 3, the operating duty cycle is 0.5. Turn ratios used are also shown in Table I.

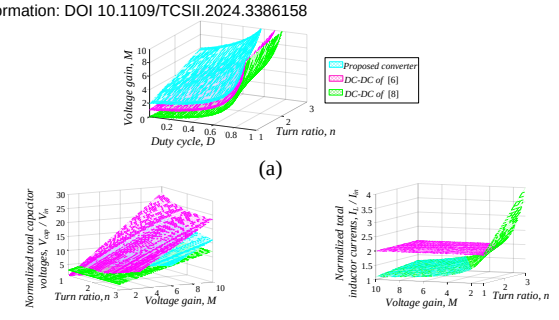

Fig. 4. Comparison of the proposed converter and the existing converters in [6] and [8]: (a) the voltage conversion ratio, (b) the normalized total voltage stress across capacitors, (c) the normalized total inductor current.

The input and output characteristics of the prototype are shown in Fig. 5(*b*). The input voltage is boosted to 116 V, which is consistent with the theoretical value of 120 V. The error may be caused by the equivalent series resistance of passive elements, the ON-state resistance of the MOSFET, and the forward voltage of diodes. The input current has a very smooth waveform, showing the effectiveness of the input current ripple reduction method. In Fig. 5(*g*), input current ripples have a direct relationship with voltage ripples across C_1. By decreasing C_1 to 10 μF, input current ripples increase. The experiment shows that the third side leakage inductance of T_1 affects input current ripples, but this is neglected in the theoretical analysis. The voltages across capacitors are shown in Fig. 5(c). By considering (11), (12), (18), and (23) to (25), the average voltage across C_1, C_2, and C_3 in the prototype is equal to the input voltage source, and their voltage ripples are less than 10%, confirmed by these experimental waveforms.

Voltage and current stresses of semiconductors are measured in Figs. 5(*d*) and 5(*e*), respectively, showing complementary switching of D_o and *SW* or D_1, which confirms the converter's operating principle. Fig. 5(*d*) shows low voltage spikes on *SW* and confirms the maximum voltage stresses of semiconductor devices as derived in (26) to (28). The *LC* circuit comprising the leakage inductance of T_2, and capacitors causes a sinusoidal

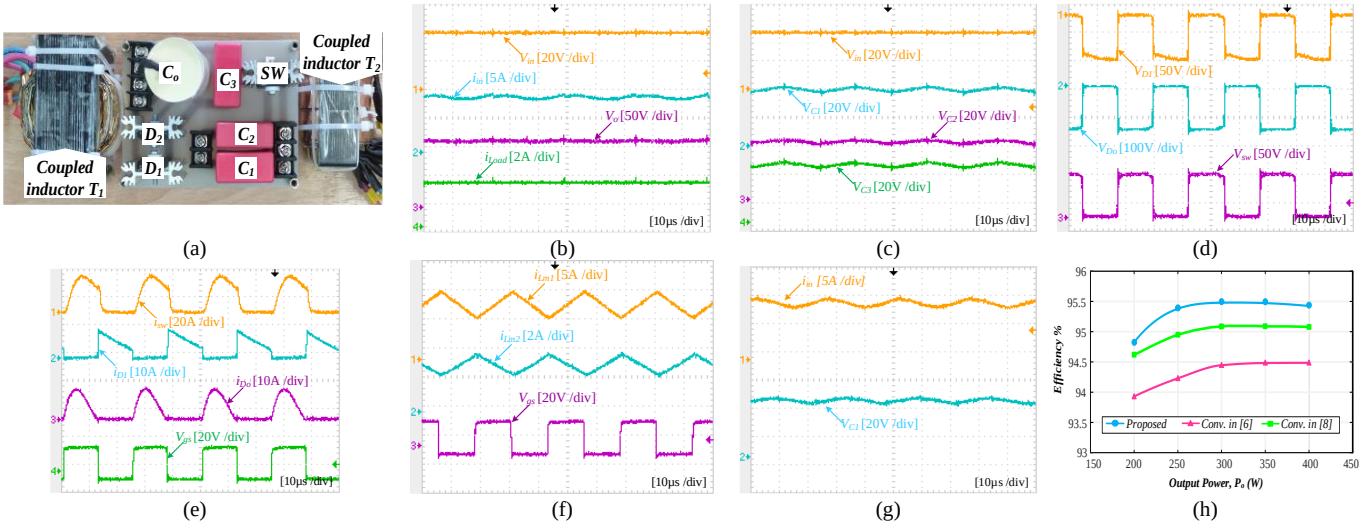

Fig. 5. Experimental results. (a) implemented setup, (b) input and output voltages and currents, (c) voltage across the capacitors, (d) voltage across the semiconductors, (e) current stress of the semiconductors, (f) magnetizing currents of the coupled inductors along with the gate pulse of *SW*, (g) input current ripples and voltage ripples across C_1 (C_1=*10µF*), and (h) efficiency comparison.

TABLE I
THE CIRCUIT PARAMETERS OF THE PROTOTYPE

Parameters	Symbols	Values
Input voltage	V_{in}	40V
Output voltage	V_o	120V
Output power	P_o	400W
Switching frequency	f_s	40KHz
Magnetizing inductances	L_{m1}, L_{m2}	102uH, 298uH
Leakage inductances	L_{k1}, L_{k2}	16.6uH, 2.2uH
Turns ratio	n_{21}, n_{31},a_{21}	1, 1, 1
Capacitors	C_1, C_2, C_3, C_o	22uF, 15uF, 22uF, 16uF
Switch	SW	SPW47N60CFD
Diodes	D_1, D_o	APT30D60B

half-cycle resonance in the current of D_o during Mode I. It can be completed if the resonant interval of the LC circuit set to be lower than twice of DT_s. In experimental waveforms in Fig. 5(*e*), this condition is satisfied. Thus, the ZCS switching of the semiconductor device is possible with reduced switching losses and smooth switching transients. Fig. 5(*f*) shows the magnetizing current of coupled inductors. Considering (19) to (22), the computed average values of magnetizing currents of T_1 and T_2 are 10 A and 3.33 A, respectively, and their current ripples are equal to 50%.

Table II shows a comparison of the proposed converter and the existing converters in [6] and [8]. For a fair comparison, the converters are designed according to input and output characteristics in Table I, and all turn ratios are equal to 1.5, except $a_{21} = 1$ [6]. Although the converter in [8] has the minimum number of capacitors, their stored energy is more than the proposed converter. All three converters utilize two magnetic cores. The stored energy in the two coupled inductors of the proposed converter is significantly lower than that in the two existing converters in [6] and [8] due to the lower magnetizing current of its coupled inductors, T_1 and T_2. In the proposed converter, the two coupled inductors share the current stress between them, and their magnetizing current is only determined by one winding, because based on the ampere-second balance principle in capacitors, the average current of two windings of T_1 and one winding of T_2 is zero. To compare semiconductors' ratings, the switching device power (SDP) can be used, as defined by (34) [11].

$$SDP = \frac{1}{P_o}\sum_{i=1}^{n} V_i^{\max} I_i^{\max}. \tag{34}$$

Where V_i^{max} and I_i^{max} are the peak voltage and current of the i^{th} semiconductor. According to Table II, the converter in [8] has the minimum rating of semiconductors. However, switching losses in the proposed converter and the converter in [6] are lower due to their ZVS and ZCS operations, leading to lower voltage spikes on their switches.

Fig. 5(*h*) shows theoretically calculated efficiency curves of the proposed converter and the existing converters in [6] and [8] for the output power ranging from 200 W to 400 W. The output voltage is fixed at 120 V by adjusting the duty cycle *D* in their output power. It is found that the efficiency of the proposed converter in the entire range of the output power is higher than that of the two existing converters. The full-load efficiency of the proposed converter is 95.4% due to a lower magnetizing current, which leads to lower core losses and lower switching losses of semiconductor devices.

TABLE II
THE TOTAL STORED ENERGY IN PASSIVE COMPONENTS AND SDP OF ACTIVE ELEMENTS

Parameters	The converter in [6]	The converter in [8]	The proposed converter
The stored energy in capacitors (mJ)	101.89	72.96	69.24
The stored energy in magnetic elements (mJ)	8.82	9.99	3.34
SDP of active elements (W)	22.89	10.45	16.18

VI. CONCLUSION

In this paper, an isolated DC-DC converter with a high voltage gain and the almost ripple-free input current is proposed for low voltage sources. The proposed converter also has a simple structure, high power density and high efficiency. The input current ripple reduction technique only depends on the turn ratio of the coupled inductor, which is easy to implement accurately. The single switch of the proposed converter experiences a low voltage spike, and thus, the MOSFET with a low $R_{ds(on)}$ can be used. The output diode operates at the ZCS, which reduces semiconductor losses effectively. The proposed converter can use a lower volume of passive components than existing converters, leading to a lower cost. Experimental results verified its operating principle and effectiveness.

REFERENCES

[1] A. M. S. S. Andrade and M. L. d. S. Martins, "Isolated boost converter based high step-up topologies for PV microinverter applications," *IET Power Electronics*, vol. 13, no. 7, pp. 1353-1363, 2020.

[2] Z. Saadatizadeh, et al, "Expandable Non-Isolated Multi-Input Single-Output DC-DC Converter With High Voltage Gain and Zero-Ripple Input Currents," *IEEE Access*, vol. 9, pp. 169193-169219, 2021.

[3] D. Sadeghpour and J. Bauman, "High-Efficiency Coupled-Inductor Switched-Capacitor Boost Converter With Improved Input Current Ripple," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7940-7951, 2022.

[4] S. B. Santra, D. Chatterjee, et al, "Coupled Inductor Based Soft Switched High Gain Bidirectional DC-DC Converter With Reduced Input Current Ripple," *IEEE Trans. Ind. Electron.*, vol. 70, no. 2, pp. 1431-1443, 2023.

[5] S. Sarani, H.A. Zarchi, and H.D. Poor, "A Passive Circuit to Cancel Input Pulsating Current of Flyback Converter," in 2020 Power Electronics, Drive Systems, and Technologies Conference, Feb. 2020, pp. 1-5.

[6] A. Kumar and P. Sensarma, "Ripple-Free Input Current High Voltage Gain DC–DC Converters With Coupled Inductors," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3418-3428, 2019.

[7] H. Bi, Z. Mu, and Y. Chen, "Common Grounded Wide Voltage-Gain Range DC–DC Converter With Zero Input Current Ripple and Reduced Voltage Stresses for Fuel Cell Vehicles," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2607-2616, 2023.

[8] S. Sarani, H. Abootorabi Zarchi, and H. Delavaripour, "Ripple-Free Input Current Flyback Converter Using a Simple Passive Circuit," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2557-2564, 2022.

[9] W. Wang, Y. Wang, Y. Guan, T. Yao, Y. Wang, and D. Xu, "A Family of Impedance Source DC-DC Converters With Zero Input Current Ripple," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 8883-8894, 2023.

[10] W. Jing, W. G. Dunford, and K. Mauch, "Analysis of a ripple-free input-current boost converter with discontinuous conduction characteristics," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 684-694, 1997.

[11] S. M. Chen, M. L. Lao, Y. H. Hsieh, T. J. Liang, and K. H. Chen, "A Novel Switched-Coupled-Inductor DC–DC Step-Up Converter and Its Derivatives," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 309-314, 2015.

[12] N. Tashakor, et. al, "An Interleaved Bi-Directional AC–DC Converter With Reduced Switches and Reactive Power Control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 1, pp. 132-136, 2020.

[13] P. Cervellini, P. Antoszczuk, et. al, "Current Ripple Characterization in DCM Interleaved Power Converters Under Inductance Mismatch," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1269-1273, 2020.

[14] H. Seok, B. Han, et. al. "High Step-Up Resonant DC–DC Converter With Ripple-Free Input Current for Renewable Energy Systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8543-8552, 2018.

[15] A. Nikbahar and M. Monfared, "Smooth DC-Link Y-Source Inverters: Suppression of Shoot-Through Current and Avoiding DC Magnetism," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12357-12369, 2022.

[16] S. Sharifi, M. Monfared, and A. Nikbahar, "Highly Efficient Single-Phase Direct AC-to-AC Converter With Reduced Semiconductor Count," IEEE Trans. Ind. Electron., vol. 68, no. 2, pp. 1130–1138, Feb. 2021, doi: 10.1109/TIE.2020.2970652.