Hardware Implementation of the DVI Protocol for Displaying Neural Network and Image Processing Outputs on FPGA ML605

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Abstract— This paper presents the implementation and testing of the Digital Visual Interface (DVI) protocol on the ML605 FPGA hardware. The goal was to create a DVI transmitter capable of converting VGA output to DVI pinouts while adhering to protocol standards. Using VHDL and the Xilinx Virtex-6 architecture, the system successfully met DVI specifications and demonstrated its applicability in displaying outputs from neural networks and image processing tasks.

Keyword: ML605 Field-Programmable Gate Array, Digital Visual Interface, Neural networks, Image Processing

INTRODUCTION

The Digital Visual Interface (DVI) protocol is widely used for transmitting digital video signals. FPGAs, like the ML605 with the Xilinx Virtex-6 architecture, offer a versatile platform for implementing such protocols. Displaying neural network and image processing outputs on monitors requires precise synchronization of pixel data and clock signals, a task well-suited for FPGA-based systems.

In recent years, FPGAs have gained attention for their ability to implement deep learning algorithms efficiently, combining low power consumption with real-time processing capabilities. This paper addresses the challenge of integrating a DVI transmitter to display neural network outputs accurately.

The structure of this paper is organized as follows: Section 2 introduces relevant studies addressing the topic. The proposed method architecture is presented in Section 3. The experimental results are provided in Section 4. Finally, the conclusions are presented in Section 5.

RELATED WORK

The development of hardware implementations of neural networks and image processing systems on FPGA platforms has significantly advanced, particularly with the integration of DVI protocols for efficient output display.

Paper [1] demonstrated the effective use of FPGAs for neural network deployment, specifically YOLO-tiny, using the DVI protocol for video output. The work highlighted the advantages of hardware-software codesign in achieving real-time video processing. Similarly, paper [2] employed lightweight neural networks on FPGAs for citrus fruit sorting, showcasing the com- bination of neural network inference and DVI-based display mechanisms. These approaches align with the broader design principles for embedded image processing on FPGA platforms discussed in [3], which emphasizes efficient interfacing for real-time applications.

The DVI protocol's utility in healthcare monitoring systems was explored in [4]. This work implemented convolutional neural network (CNN) architectures for contactless epidemic prevention, leveraging FPGA-embedded DVI Transmitter IP cores for efficient image processing and recognition. Comparable results were achieved in [5], which developed memory-efficient FPGA designs for real-time motion detection using a similar DVI interface for video output. Such advancements are consistent with the signal integrity optimization techniques reviewed in [6], where high- speed interconnect protocols like DVI were analysed for efficient data transmission in FPGA systems.

In the field of video analytics, paper [7] proposed an FPGA-based system for smart

sports monitoring. Their integration of CNNs with DVI-supported output significantly improved object recognition and real-time analytics for hockey games. Meanwhile, [8] investigated edge artificial intelligence, employing FPGA implementations of oscillatory neural networks with DVI support for displaying AI-powered edge analytics. These studies resonate with [3], which covers advanced FPGA design techniques for real-time multimedia applications.

The application of neural networks in industrial automation has also been well-documented. Paper [9] implemented image processing blocks on FPGA platforms, integrating feedforward neural networks for real-time bottle classification. This work aligns with [10], which utilized memristor-induced fractional-order neural networks on FPGAs for image encryption, combining high-speed processing with secure output via the DVI interface.

Additionally, [11] examined the integration of DVI and VGA interfaces with FPGA systems for video enhancement. Their work employed convolutional neural networks for multimedia processing, underlining the versatility of FPGAs in handling various output standards. Further advancements in multimedia applications were demonstrated in [12], which utilized feedforward neural networks for image processing and efficient DVI display. These findings complement the statistical methodologies discussed in [6], particularly in terms of improving signal integrity for multimedia outputs.

PROPOSED METHOD

The implementation of the DVI protocol involved the following key aspects:

- Clock Domain Crossing (CDC): Synchronizing multiple clock frequencies (pixel, character, and timing signals).
- Timing Signal Generation: Producing pixel clock, horizontal/vertical sync, and data enable signals to meet DVI specifications.
- Neural Network Output Display: Visualizing processed neural network outputs, such as class probabilities or heatmaps, on a monitor using the DVI interface.

A. DVI SIGMAL CONVERSION

Pixel data (RGB values), synchronization signals (HSYNC, VSYNC), and a clock signal (DVI_CLK) ensure accurate rendering of images on an LCD. The FPGA-generated signals align pixel data with the display's grid structure.

B. VERILOG IMPLEMENTATION

The system comprises modules for clock generation, display timing, and neural network output visualization:

- Clock Module: Generates pixel clock signals for synchronization.
- Timing Module: Produces sync signals and pixel positions (sx, sy) for rendering.
- AI Model Module: Maps neural network out- puts to RGB pixel values for display.

A User Constraints File (UCF) was used to assign FPGA pins to DVI signals, ensuring correct routing and functionality.

EXPERIMENTAL RESULT

The implementation successfully met DVI protocol standards, supporting resolutions up to 1920x1080 at 60 Hz. Key findings include:

- Precise synchronization with no visible distortion.
- High-resolution video output, capable of rendering neural network results in real time.
- Efficient resource utilization, allowing additional FPGA tasks.

The results validated the feasibility of using the ML605 FPGA for real-time visualization of neural network and image processing outputs has been shown in Fig. 1.

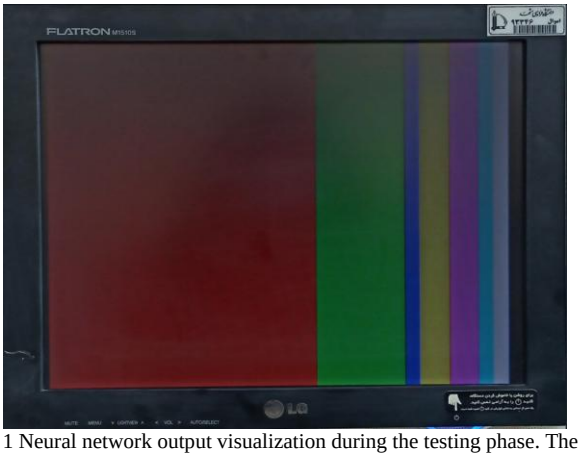

Fig. 1 Neural network output visualization during the testing phase. The width of the colour bar represents the probability of the most likely class.

CONCLUSION

This work demonstrates the ML605 FPGA's capability to implement the DVI protocol for displaying neural network outputs and image processing tasks. The system provides real-time feedback, enabling better validation and interaction in embedded applications.

Future work includes optimizing for higher resolutions, exploring additional video protocols, and integrating more complex neural networks. The results validate FPGAs as powerful platforms for intelligent, real-time systems in embedded applications.

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