Abstract
In this paper challenges observed in 65nm technology for circuits utilizing subthreshold region operation are presented. Different circuits are analyzed and simulated for ultra low supply voltages to find the best topology for subthreshold operation. To support the theoretical discussions different topologies are analyzed and simulated. Various aspects of flip-flop circuits are described in detail to study which topology would be most suitable for ultra low supply voltage and low-power applications. Simulation results show that the power consumption decreases by at least 23% compared with other flip-flops. Also, the setup time and the hold time are improved.

Keywords
Low-voltage, low-power, subthreshold, nanoscale

1. Introduction
In the last few years, large efforts have been made in research and development on low energy circuits for battery operated wireless sensor nodes. Recently a number of papers reporting ADC's utilizing time-domain instead of amplitude domain have been reported [1]-[4]. This class of converters may be built entirely of digital components, but this would put strict requirements on the comparator and sampling circuitry. To meet these requirements low power and high speed flip-flops with a sufficiently low possibility for metastability must be designed. Recently, as we approach atomic scale devices, leakage currents have increased dramatically, leading to higher static power dissipation. Therefore, leakage must be taken into consideration when evaluating these circuits since it has become a significant contributor to the overall power consumption in deep-submicron CMOS processes.

Subthreshold current rises due to lowering of threshold voltage which is scaled down to maintain transistor ON current in the face of falling power supply voltage. Voltage scaling for standby power reduction was suggested since both subthreshold current and gate current decrease dramatically (with Vd for gate leakage) [5]. Lowering supply voltage thus saves standby power by decreasing both standby current and voltage [6]. The subthreshold region (weak inversion) is often utilized to implement power efficient circuits for ultra low power wireless applications, but due to the much lower current in subthreshold region compared with higher supply voltages, the evaluation speed of such circuits operating in weak inversion is decreased. Therefore, new techniques to improve circuit speed need to be developed.

The rest of the paper is organized as follows. In section 2, some characteristics of 65nm CMOS technology in weak inversion are described. Also the effect of some techniques in subthreshold region is explained in details. In section 3, new flip-flop design concepts in 65nm CMOS technology for operation in subthreshold region are proposed by improving upon existing designs. The comparison of results is also included in this section. Conclusions are presented in section 4.

2. Subthreshold 65nm characteristics
Subthreshold design has emerged as a good potential for ultra low power applications such as wireless sensor networks, medical instruments, and portable devices.

We have observed some specific behaviors from devices operating in subthreshold region in the 65nm technology due to lack of well-engineered models for subthreshold region. Short channel devices have been optimized for regular strong inversion circuits to meet various objectives such as high mobility, reduced DIBL, low leakage current, and minimal Vth roll-off. However, a transistor that is optimized for operation in superthreshold logics are not necessarily optimal in low voltage, low power dissipation applications designed for operation in the subthreshold region. Optimization problems include the transistor sizing, the drive current for PMOS and NMOS devices, the effects of some techniques such as Forward Body Bias (FBB), Reverse Body Bias (RBB), and stacking effects on threshold voltage and drive current. Although it would be ideal to have a dedicated process technology optimized for subthreshold circuits this is not practically achievable. In order to design optimal subthreshold circuits using CMOS devices that are targeted for superthreshold operation, it is crucial to develop design techniques that can utilize the side effects that appear in this new regime. However, in the absence of such dedicated process the development of low voltage low power applications using the 65nm CMOS technology requires care and novelty in design.

2.1 DC Analysis
In this section three topologies for basic circuits are presented and simulated using DC analysis. Fig.1 illustrates the topologies that are simulated in 65nm technology with supply voltage equal to VDD=0.9V. In all topologies minimum sizes for the transistors are used. Fig.1 (a) shows the three stacked devices (two PMOS and one NMOS referred to as 2PMOS). Fig.1 (b, c) are referred to as 3PMOS and 2NMOS respectively. Simulation results based on DC analysis for these three configurations are illustrated in Fig. 2. As it can be observed, the short circuit current in 2NMOS is higher than for the other circuits, which implies that the delay for 2NMOS is higher than for the other topologies causing increased short circuit current through this circuit.