Analog Integr Circ Sig Process (2009) 58:153–160
DOI 10.1007/s10470-008-9226-1

Design of low-power single-stage operational amplifiers based on an optimized settling model

Hamed Aminzadeh · Reza Lotfi · Khalil Mafinezhad

Received: 29 July 2006 / Revised: 6 May 2008 / Accepted: 29 September 2008 / Published online: 19 November 2008

Abstract Settling behavior of operational amplifiers (opamps) is important in many analog signal-processing applications. In this paper, the analysis of single-stage opamps based on settling time has been performed. A simple yet accurate model for the settling response of first-order opamps that modifies conventional models is proposed to revise the equations. The presented approach leads to a new simple settling-based design methodology for single-stage operational amplifiers. Circuit-level simulations demonstrate the effectiveness of the procedure.

Keywords Design methodology · Opamp · Operational amplifier · Power optimization · Settling model · Settling time · Slew rate

1 Introduction

Negative feedback operational amplifiers are widely employed in analog integrated circuits such as voltage regulators, filters and data converters [1, 2]. Optimization of these basic building blocks based on their speed and accuracy have been always of concern. Single-stage opamps have superior frequency response and higher speed compared to their multistage counterparts. Furthermore, with only one low-frequency open-loop pole, they do not need extra circuitry for closed-loop stability [3]. These advantages greatly simplify the design complexity and the specifications of input transistors are remained as the only critical parameters in settling performance of these opamps.

The main drawback of single-stage amplifier in modern technologies is their relatively low open-loop DC gain. Depending on the required accuracy, a lower bound of this parameter is needed to adequately suppress the structure inherent nonlinearities [1, 2]. Advanced gain-boosting techniques have been reported to alleviate these shortcomings. However these techniques are at the cost of more complexity, additional power and degraded frequency response and dynamic range. Compensating for opamp nonlinearities in digital domain is possible in analog-to-digital converters (ADCs) [4, 5]. Although the required post processing might be complicated, the needed accuracy for analog-domain circuits is greatly relaxed. Hence opamps can be optimized according to their speed rather than accuracy. In such applications, low-power fast-settling single-stage operational amplifiers can be the best choice.

Regarding the importance of settling time for the desired accuracies in many applications such as regulators and switched-capacitor amplifiers, the analysis of single-stage opamps based on settling time have been performed here. A simple yet accurate model for the settling response of first-order opamps is presented that modifies the conventional model. As will be shown later, conventional model always overestimates the amplifier required bandwidth when a specified settling time is to be achieved. This stems from the fact that the transition point between nonlinear (large-signal) and linear (small-signal) sections of step response is ambiguous [1]. Consequently the large-signal settling time is conventionally computed for total step amplitude. Based on the revised model, the optimized relationships between open-loop gain-bandwidth product

H. Aminzadeh (✉) · R. Lotfi · K. Mafinezhad
Integrated Systems Laboratory, EE Department,
Ferdowsi University of Mashhad, Mashhad, Iran
e-mail: haminzadeh@ieee.org

R. Lotfi
e-mail: rlotfi@ieee.org

(*GBW*), power consumption and settling time are obtained. The proposed approach also leads to a new design methodology for single-stage opamps. Although the analysis has been performed for single-stage topologies, it can be easily extended to higher-order cases [6].

This paper is divided into five additional parts. Section 2 discusses about the small-signal settling behavior of single-stage opamps. In Sect. 3, large-signal settling is also considered for the case of total settling time analysis. In Sect. 4, the proposed model is presented and equations are revised. Finally simulation results are presented in Sects. 5 and 6 gives the conclusions.

2 Small-signal settling analysis

In this section, the relationship between small-signal settling part of the step response and gain-bandwidth product in single-stage opamps will be derived. A relationship for total settling time is only possible after taking into account both nonlinear (slewing) and linear (small-signal) sections of the response. This will be accomplished in the next section. The open-loop voltage transfer function part of a first-order single-stage opamp with one left-half-plane pole and no zero is as follows [1–3]:

$$A_V(s) = \frac{A_0}{1 + s/\omega_0}, \tag{1}$$

where A_0 and ω_0 are the open-loop DC gain and -3dB angular frequency respectively. According to the required accuracy, the closed-loop total settling error ($e_{SS,t)}$ is achievable. Assuming that the opamp is not slew limited, this error is comprised of two different sources, one originated from opamp finite open-loop DC gain ($e_{SS,A}$) and one from its finite open-loop gain-bandwidth product (to be named $e_{SS,GBW}$ or e_{SS} for convenience). In closed-loop systems with negative feedback, one can easily show that the error caused by finite DC gain is as follows [2]:

$$e_{SS,A} = \frac{1}{1 + A_0\beta} \cong \frac{1}{A_0\beta}, \tag{2}$$

where β is the closed-loop feedback factor. Thus, the total settling error is obtained from:

$$e_{SS,t} = e_{SS} + 1/A_0\beta. \tag{3}$$

The time domain expressions for the closed-loop configuration can be manipulated to achieve the following relationship between small-signal settling time (t_{SS}) and the error caused by finite bandwidth [2]:

$$e_{SS} = \exp(-t_{SS}/\tau) = \exp(-\beta \cdot GBW \cdot t_{SS}). \tag{4}$$

In this equation, τ is the closed-loop time constant ($\tau = 1/(\beta \cdot GBW)$). *GBW* represents the opamp gain-bandwidth product (or its angular open-loop unity—gain frequency where $|A_V(jGBW)| = 1$). Equation 4 shows the relationship between t_{SS} and *GBW*. It can be rearranged as:

$$t_{SS} = n\tau = n \cdot \frac{1}{\beta \cdot GBW}, \tag{5}$$

where n is the number of required linear time constants, in which the error caused by the finite bandwidth becomes less than e_{SS}. It is a function of e_{SS} and can be expressed as follows:

$$n = \frac{t_{SS}}{1/(\beta \cdot GBW)} = \ln\frac{1}{e_{SS}} = f(e_{SS}). \tag{6}$$

In addition based on (5), the required gain-bandwidth to achieve a specified small-signal settling time is given by:

$$GBW = \frac{n}{\beta \cdot t_{SS}}. \tag{7}$$

3 Total settling analysis

The analysis performed here, includes all single-stage opamps assuming single-pole transfer functions i.e. the effect of parasitic poles and zeros should be ignored. Figure 1 shows a fully-differential instance. In this circuit, the tail current is expressed as:

$$I_{Tail} = 2I_i = C_L \cdot SR = C_L \cdot V_{Swing}/t_{LS}, \tag{8}$$

where *SR*, V_{Swing} and t_{LS} are slew rate, peak-to-peak differential swing of output voltage and large-signal settling time respectively. Besides, C_L and I_i are the load capacitance and the current value of input transistors, respectively. Equation 8 shows that to ensure the amplifier reliability, large-signal settling time should be calculated for the maximum output swing as the worst case [1, 2].

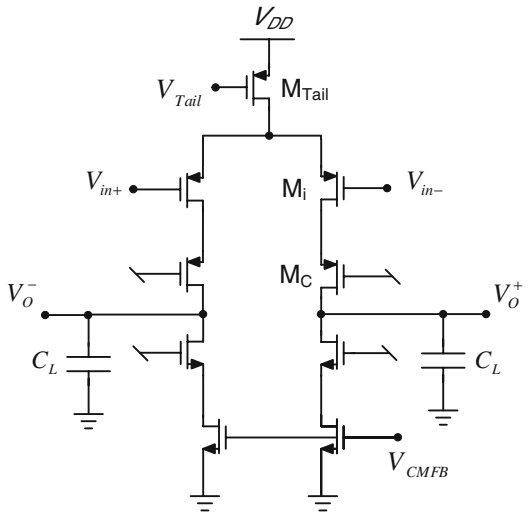

Fig. 1 A single-stage fully-differential amplifier

The goal of the analysis performed in this part is to obtain the optimized *GBW* in which the amplifier is able to settle within the desired amplitude with the required accuracy. The relationship should be obtained for maximum step amplitude as the worst case so that the required accuracy for smaller amplitudes is guaranteed. If there was a relationship between *GBW* and t_{LS}, it would be possible to express the total settling time in terms of this parameter. As will be seen later, such a relation is achievable if the required current to satisfy large-signal settling constraints is set equal to the one required to satisfy small-signal settling constraint [7]. The equation derived by this method is indeed optimized because if the large-signal and small-signal settling times are predetermined independently (as proposed in [8]), the tail current is to be chosen as the larger value which satisfies both of them. However, if the large-signal and small-signal currents are set equal (by appropriately choosing the overdrive voltage of input transistors (V_{effi})), optimum condition is obtained:

$$I_{Tail} = 2I_i = g_{mi} \cdot V_{effi} = C_L \cdot V_{Swing}/t_{LS}, \tag{9}$$

where g_{mi} is the transconductance of the input transistors. Since:

$$GBW = A_0\omega_0 = \frac{g_{mi}}{C_L}, \tag{10}$$

the relationship between t_{LS} and *GBW* becomes:

$$t_{LS} = \frac{V_{Swing}}{V_{effi} \cdot GBW}. \tag{11}$$

The total settling time is comprised of both small-signal and large-signal settling sections. The analysis for small-signal part is performed formerly in Sect. 2. By adding (5) with (11), the total settling time becomes:

$$t_S = t_{SS} + t_{LS} = \left(\frac{1}{\beta}\ln(1/e_{SS}) + \frac{V_{Swing}}{V_{effi}}\right)\frac{1}{GBW}. \tag{12}$$

So by appropriately choosing the gate overdrive voltage of input transistors, the following meaningful relation between gain-bandwidth product and settling time is obtained:

$$GBW = \left(\frac{n}{\beta} + \frac{V_{Swing}}{V_{effi}}\right)\frac{1}{t_S}. \tag{13}$$

This expression clearly proves that by reducing the required small-signal settling accuracy (decreasing *n* according to (6)) and output swing, the needed *GBW* for a given settling time decreases. It also reveals that for a particular settling time, decreasing β increases the required *GBW*.

From (13), the required slew rate (*SR*) for a particular settling time can be acquired as well if the following relationship between *GBW* and *SR* is considered:

$$SR = \frac{2I_i}{C_L} = \frac{2I_i}{V_{effi}C_L}V_{effi} = \frac{g_{mi}}{C_L}V_{effi} = V_{effi} \cdot GBW. \tag{14}$$

4 Proposed model, analysis of power and design methodology

As demonstrated earlier, a closed-form equation between the settling time and bandwidth of a single-stage opamp is available. The obtained equation is based on the conventional model. In this section, we shall modify this equation and continue to obtain the optimized relationship between settling time and power consumption. At last, a new design methodology will be proposed.

4.1 Proposed settling model

The proposed settling model can be analyzed as follows:

4.1.1 The opamp is not slew-limited

This occurs when slew rate at the first moment is larger than the slope of linear small-signal step response, i.e.:

$$SR > \left(\frac{dV_o}{dt}\right)_{\max}. \tag{15}$$

Beginning from (15), one can easily show that the maximum allowable amplitude for this condition to be satisfied is [1]:

$$V_{o\max} < \frac{V_{effi}}{\beta}, \tag{16}$$

where V_{omax} is the final steady-state amplitude. This situation holds in very small feedback factors or step amplitudes which is less common. In this case, small-signal equations are valid and the needed gain-bandwidth for the required settling time can be obtained from (7).

4.1.2 The opamp is slew-limited

By applying a large-signal step input to a closed-loop amplifier configuration, one of the input transistors turns off and all the tail current passes through the turned-on device. So the slewing effect might be dominant. In the slewing region, the output behavior is approximately independent of input signal [1, 2, 9, 10] and could be modeled as a straight line with particular slope. The circuit gradually enters the linear section where small-signal settling equations are valid. The transition point between the two regions is ambiguous in traditional model. In the conventional model already discussed, the point is usually considered as the amplitude in which the turned-off transistor begins to conduct (i.e. $V_{GS} \sim V_T$) [1]. According to (16) which is for the

case when the opamp is not slew-limited, this is not generally correct. Hence, to properly revise the equations a simple yet accurate model is necessary.

Based on the proposed model, when the initial slope of equivalent small-signal response is larger than the slew rate, the step response begins with slewing effect. *At the moment the slope of equivalent small-signal response becomes equal to the slew rate, independent of input transistors situation the transition between small-signal and slewing regions occur.* For simplicity, Fig. 2 shows the regions. They can be summarized as follows:

$$\begin{cases} 0 < t < t_{LS} \Rightarrow \text{Slewing is dominant effect} \\ t_{LS} < t < \infty \Rightarrow \text{Small - Signal equation is dominant} \end{cases}$$

Notating the slewing period as t_{LS}, one can write:

$$0 < t < t_{LS} : V_o(t) = SR \times t. \tag{17}$$

On the other hand, when the output response enters the second linear region it obeys the small-signal equation. Hence:

$$t_{LS} < t < \infty : V_o(t) = \alpha \cdot (1 - \exp(-\beta.GBW \cdot (t - t_{LS}))) + \gamma. \tag{18}$$

As V_{omax} is the final steady-state voltage, t_{LS} is obtained from:

$$t_{LS} = \frac{V_{o\max} - \alpha}{SR}. \tag{19}$$

In (18) and (19), α and γ are the amplitude of small-signal and large-signal sections respectively (Fig. 2). These two parameters should be determined according to boundary conditions and the fact that the response and its derivative are naturally both continuous at the transition point:

$$V_{o,Nonlinear}(t_{LS}) = V_{o,Linear}(t_{LS}) = SR \times t_{LS}, \tag{20}$$

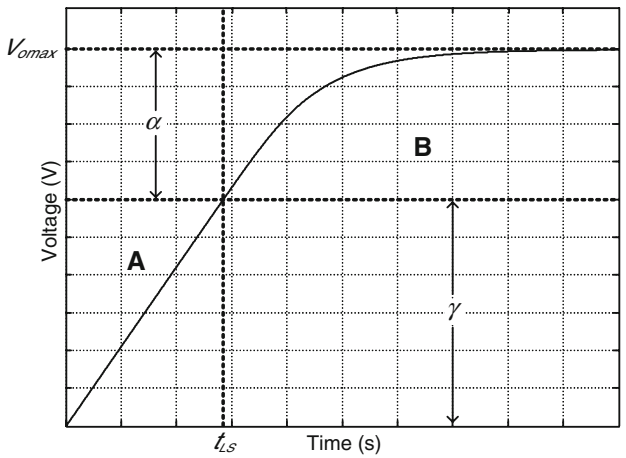

Fig. 2 Different sections of step response a: Nonlinear section b: Linear (small-signal) section

$$\frac{dV_{o,Nonlinear}(t_{LS})}{dt} = \frac{dV_{o,Linear}(t_{LS})}{dt} = SR. \tag{21}$$

Based on these two conditions, α and γ are obtained from:

$$\alpha = \frac{SR}{\beta \cdot GBW}, \tag{22}$$

$$\gamma = SR \times t_{LS}. \tag{23}$$

Applying (22) and (23) into (18), the response is expressed as:

$$t_{LS} < t < \infty : \quad V_o(t) = V_{\text{omax}} - \frac{SR}{\beta \cdot GBW} \exp(-\beta \cdot GBW \cdot (t - t_{LS})). \tag{24}$$

In addition, by combining (19) with (22) the large-signal settling time is given by:

$$t_{LS} = \frac{V_{o\max}}{SR} - \frac{1}{\beta \cdot GBW}. \tag{25}$$

An important and interesting consequence of this model which is very useful for our analysis is the relationship between large-signal settling time and gain-bandwidth. Substituting (14) into (25) and setting $V_{omax} = V_{Swing}$ as the worst case, one may obtain:

$$t_{LS} = \left(\frac{V_{Swing}}{V_{effi}} - \frac{1}{\beta}\right) \frac{1}{GBW}. \tag{26}$$

To be able to use this equation, one should know that only positive values of t_{LS} are acceptable. Based on (16) and (25), negative values of large-signal settling time are due to the fact that the circuit is not slew-limited (i.e. $t_{LS} = 0$). In such cases, the circuit begins with small-signal settling equation and (5), (6) and (7) are the case.

Instead of (11) derived by conventional model, (26) can be used to extract the optimized relationship between settling time and gain-bandwidth product:

$$GBW = \left(\frac{n-1}{\beta} + \frac{V_{Swing}}{V_{effi}}\right) \frac{1}{t_S}. \tag{27}$$

As is seen, this equation is similar to (13) from conventional model but with a lower value for predicted *GBW*.

4.2 *Power Dissipation Analysis*

For the circuit topology shown in Fig. 1, the following relationship between power consumption (P) and the tail current is valid:

$$P = 2 \cdot V_{DD} I_i = V_{DD} \cdot I_{Tail}. \tag{28}$$

In this equation, the current consumption of the bias circuit as well as that of the common-mode-feedback

circuit (in fully-differential circuits) is not included. The contributions of those circuits, however, can be assumed proportional to the current of the main branches. Employing (9), the relationship between power and *GBW* therefore is expressed as:

$$P = V_{DD} \cdot V_{effi} \cdot C_L \cdot GBW. \tag{29}$$

This equation reveals the fact that power consumption is proportional to the required unity gain-bandwidth. Combining (29) with (27) and (3), for the case the circuit is slew-limited the relationship between power and settling time becomes:

$$P = V_{DD} \cdot V_{effi} \cdot C_L \left(\frac{1}{\beta} \left(\ln \left(\frac{1}{e_{SS,t} - 1/A_0\beta} \right) - 1 \right) + \frac{V_{Swing}}{V_{effi}} \right) \frac{1}{t_S}. \tag{30}$$

As it is seen, for a fixed value of settling time by increasing the load capacitance, output voltage swing (or equivalently the required dynamic range) and also by decreasing the feedback factor (increasing the closed-loop gain) and the steady-state error (increasing the required accuracy), power dissipation increases. As a particular case, assuming that the amplifier is purely class-A and beginning from (30), the relationship between power and sampling frequency of a switched-capacitor circuit (f_S) is obtained as follows:

$$P = 2 \cdot V_{DD} \cdot V_{effi} \cdot C_L \left(\frac{1}{\beta} \left(\ln \left(\frac{1}{e_{ss,t} - 1/A_0\beta} \right) - 1 \right) + \frac{V_{Swing}}{V_{effi}} \right) \cdot f_S. \tag{31}$$

This expression takes into account the requirement that switched-capacitor circuits need to settle in ½ clock period. It is an important result and shows that although the analog power (the dominant power consumer in ADCs) is mostly static resulted by the static bias currents used to bias transistors in the saturation region, its optimized value is linearly proportional to the sampling frequency. Hence it can be used as a reference in programmable variable sampling frequency data converters [11] both for power evaluation and optimization.

It is also interesting to note that Eq. 31 is similar to the representation of dynamic power consumption in digital circuits:

$$P_{Digital} = f_S \cdot C \cdot V_{DD}^2 = f_S \cdot V_{DD} \cdot (CV_{DD}) = f_S \cdot V_{DD} \cdot Q_{Digital}, \tag{32}$$

where, $Q_{Digital}$ is the equivalent charge of digital dissipated power. If single-stage operational amplifiers are regarded as the representatives of analog circuits, (31) can be rewritten as the following symbolic form:

$$P_{Ana\log} = f_S \cdot V_{DD} \cdot Q_{Ana\log}, \tag{33}$$

where Q_{Analog} is the equivalent charge of analog power dissipation.

Using (32) and (33), the total power dissipation of a mixed-signal integrated circuit assuming identical analog and digital operating frequency is approximated as:

$$P_{Total} = f_S \cdot V_{DD} \cdot (Q_{Digital} + Q_{Ana\log}). \tag{34}$$

4.3 Proposed design methodology

It is now possible to present a simple well-defined design procedure for single-stage opamps based on the derived equations. In the proposed methodology, load capacitor (C_L), total settling time (t_S), overdrive voltage of input transistors (V_{effi}), feedback factor (β) and the settling total error ($e_{SS,t}$) are input parameters which should be specified. The design procedure begins with determining DC gain and required output voltage swing. The amount of required DC gain is specified based on the desired accuracy and feedback factor. The selected topology should be capable to provide the required gain. The full-scale voltage swing should be determined according to the needed dynamic range. After specifying these parameters, the transconductance of input transistors versus total settling time of the slew-limited amplifier is obtained. Combining (27) with (10) yields:

$$g_{mi} = C_L \left(\frac{1}{\beta} \left(\ln \left(\frac{1}{e_{SS,t} - 1/A_0\beta} \right) - 1 \right) + \frac{V_{Swing}}{V_{effi}} \right) \frac{1}{t_S}. \tag{35}$$

For the case the circuit is not slew-limited which is less common, g_{mi} can be obtained through combining (7) with (10). The input stage current value has major effect on the settling behavior of the opamp. The optimized value of this parameter to satisfy both large-signal and small-signal settling times is calculated from:

$$I_i = \frac{1}{2} g_{mi} \cdot V_{effi} = \frac{1}{2} C_L \left(\frac{V_{effi}}{\beta} \left(\ln \left(\frac{1}{e_{SS,t} - 1/A_0\beta} \right) - 1 \right) + V_{Swing} \right) \frac{1}{t_S}. \tag{36}$$

The current consumption can also be obtained according to the sampling frequency of a switched-capacitor sampling circuit:

$$I_i = C_L \left(\frac{V_{effi}}{\beta} \left(\ln \left(\frac{1}{e_{SS,t} - 1/A_0\beta} \right) - 1 \right) + V_{Swing} \right) f_S. \tag{37}$$

Other devices can be sized such that the circuit performance in terms of noise requirements, DC gain,

output swing, common mode feedback loop-gain and the location of parasitic poles and zeros are satisfied.

5 Simulation results

Circuit-level simulation results are obtained with 0.25 μm BSIM3 2.5 V models using HSPICE. To verify the accuracy of the analysis, a fully-differential opamp with structure shown in Fig. 1 and a single-ended opamp with the structure shown in Fig. 3 are manually designed using the proposed design methodology. Most of the obtained equations are valid for single-ended topologies as well. Both opamps are employed in unity-feedback structure. To implement the unity-feedback, fully-differential opamp is utilized in a flip-around sample-and-hold architecture (SHA) [1, 2]. Table 1 compares the expected values with simulation results for 5pF load capacitor of each SHA outputs. The 0.5% settling time is obtained relatively close to the calculated value.

In the single-ended topology, the opamp output is directly shortened to its negative input for the sake of implementing unity-feedback factor. In this case, the open-loop specifications are $V_{effi} = 135$ mV, DC gain = 50dB, $V_{Swing} = 1$Vp-p and $g_{mi} = 8.5$ mA/V. Note that single-ended structures suffer from a parasitic mirror-pole in which its effect might have minor influence on the settling behavior. This is not a shortcoming in fully-differential topologies. Figure 4 shows the actual step response for 10pF load capacitor in the simulated single-ended topology. The linear settling model and the proposed model are also included for comparison.

Figure 5 compares the actual relationship between 0.5% settling time and gain-bandwidth of the single-ended topology. To vary the gain-bandwidth product, load capacitor is changed here. The behavior of the proposed model is very close to the simulation results. The deviation between predicted and simulated values does not exceed from five percent. Equation 13 derived by conventional model is also presented for comparison in this figure. As is

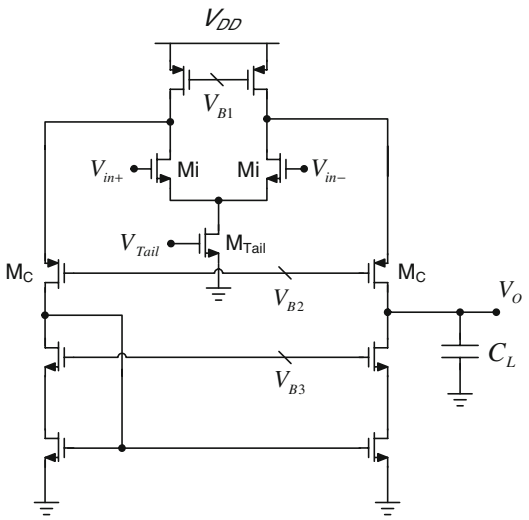

Fig. 3 Single-ended opamp topology used in simulation

Table 1 Simulated and calculated results for S/H

Parameter	Simulation	Calculation
V_{effi}	0.29 V	0.3 V
Output swing	0.9Vp-p	0.9Vp-p
Load capacitor (C_L)	5pF	5pF
Feedback factor (β)	1	1
DC gain	50 dB	50 dB
Total settling error	0.5%	0.5%
Settling time	9.31 ns	10 ns
Transconductance (g_{mi})	4.16 mA/V	4.15 mA/V

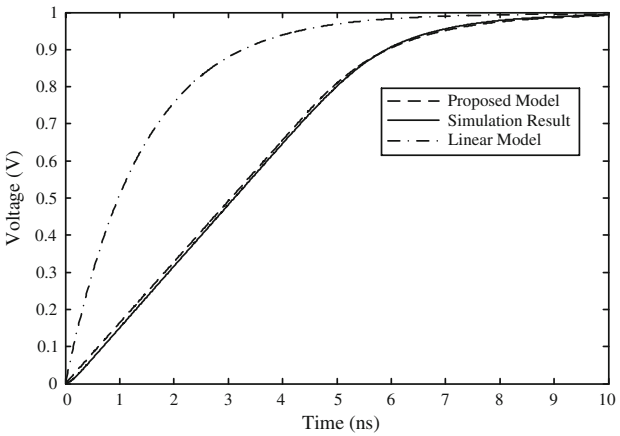

Fig. 4 Comparison between proposed model and simulation result step response ($C_L = 10$pF)

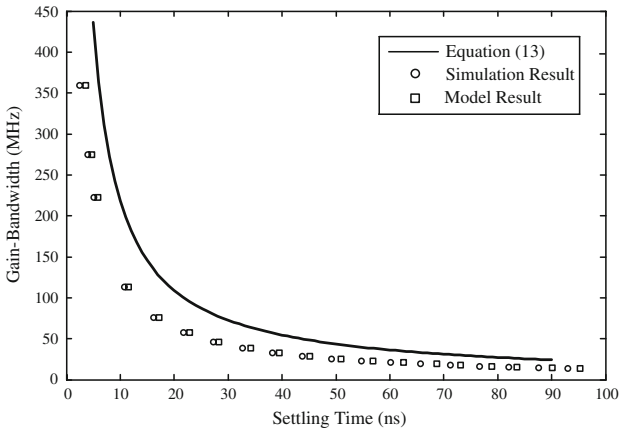

Fig. 5 Relationship between settling time and gain-bandwidth

seen, this equation always overestimates the needed gain-bandwidth for a particular settling time. Hence the structures that are designed by conventional model are never power optimized.

It is worth mentioning that, to fairly obtain the efficiency of proposed model in both Figs. 4 and 5, the correct value of slew rate is extracted from simulation and employed by the model. This is essential to distinguish the error caused by model and the one caused by inaccurate slew rate value predicted by (14).

6 Conclusions

A thorough analysis based on total settling time of single-stage operational amplifiers has been presented in this paper. By considering the effect of feedback factor and also by revising the equations, the optimized relationship between power consumption and settling time are obtained. Simulation results confirm that the proposed design procedure can be used to design operational amplifiers that meet all the given specifications. The advantages of the proposed methodology are:

- The methodology is based upon the optimized relationship between settling time and bandwidth. Hence, it could be very helpful for the design of switched-capacitor circuits without much blind effort on adjusting open-loop parameters to achieve the required closed-loop specifications.
- The methodology is straightforward and flexible and could be easily utilized in analog knowledge-based CAD tools both for the design and for power optimization.

References

1. Gray, P., Hurst, P. J., Lewis, S. H., & Meyer, R. (2001). *Analysis and design of integrated circuits* (4th ed.), Wiley.
2. Razavi, B. (2001). *Design of analog CMOS integrated circuits*. McGraw-Hill.
3. Leung, K. N., & Mok, P. K. T. (2001). Analysis of multistage amplifier frequency compensation. *IEEE Transactions on Circuits and Systems I: Fundamental Theory, 48*(9), 1041–1056.
4. Murmann, B., & Boser, B. (2003). A 12b 75 MS/s pipelined ADC using open-loop residue amplification. *IEEE Journal of Solid-State Circuits, 38*(12), 2040–2050. doi:10.1109/JSSC.2003.819167.
5. Grace, C. R., Hurst, P. J., & Lewis, S. H. (2005). A 12-bit 80-MSample/s Pipelined ADC With Bootstrapped Digital Calibration. *IEEE Journal of Solid-State Circuits, 40*(5), 1038–1046. doi:10.1109/JSSC.2005.845972.
6. Aminzadeh, H., Danaie, M., & Lotfi, R. (2007). Design of two-stage miller-compensated amplifiers based on an optimized settling model. In *Proc. Int. Conf. on VLSI Design held jointly with Int. Conf. on Embedded Systems (VLSID'07)*, pp. 171–176, Jan. 2007.
7. Lotfi, R., Taherzadeh, M., Yaser Azizi, M., & Shoaei, O. (2003). Low power design for low-voltage fast-settling operational amplifier in switched capacitor applications. *Integration, the VLSI Journal, 36*, 175–189.
8. Waltari, M. (2002). *Circuit techniques for low-voltage and high-speed A/D converters*, Ph.D. Dissertation, Helsinki University of Technology.
9. Wang, F., & Harjani, R. (1995). An improved model for the slewing behavior of opamps. *IEEE Transactions on Circuits Systems-II, 42*, 679–681. doi:10.1109/82.471400.
10. Kamath, B. Y., Meyer, R. G., & Gray, P. R. (1974). Relationship between frequency response and settling time of operational amplifiers. *IEEE Journal of Solid-State Circuits, 9*, 347–352. doi: 10.1109/JSSC.1974.1050527.
11. Ahmed, I., & Johns, D. A. (2005). A 50-MS/s (35 mW) to 1-kS/s (15 μW) power scaleable 10-bit pipelined ADC using rapid power-on opamps and minimal bias current variation. *IEEE Journal of Solid-State Circuits, 40*(12), 2446–2455. doi: 10.1109/JSSC.2005.856289.

Hamed Aminzadeh was born in Mashhad, Iran, in 1982. He received B.S. and M.S. degrees (both with honors) in 2004 and 2006 respectively, in electronics engineering. His research interests include: design of low-voltage low-power analog and mixed-signal integrated circuits in CMOS deep sub-micron technologies, digital-to-analog and digitally-calibrated analog-to-digital converters for telecommunication applications, and power supply optimization for battery-operated portable devices. Mr. Aminzadeh was awarded the outstanding graduating student award in 2004 and a research excellence award in 2007.

Reza Lotfi received his BSc from Ferdowsi University of Mashhad, I.R. Iran, his MSc from Sharif University of Technology, Tehran, I.R. Iran in 1999 and his PhD from the University of Tehran, Tehran, I.R. Iran in 2003 all in Electrical Engineering. Since, 2003 he has been with Ferdowsi University of Mashhad, I.R. Iran as assistant professor where he founded the Integrated Systems Lab in 2004. Since Jan. 2008, he has been with Delft University of Technology, Delft, the Netherlands as a post-doctoral scientific researcher working on design of ultra-low-power analog and mixed-signal integrated circuits for biomedical applications. His research interests include low-voltage low-power analog integrated circuit design for biomedical applications as well as high-speed data converters for telecommunication systems.

Khalil Mafinezhad was born in Mashhad, Iran on 21 April 1947. He received the B.S. degree in Communication Engineering from Khajenasir University, Tehran Iran, in 1972, and the MS and PhD degrees from the E.N.S.T. (Ecole National Superieur de Telecommunication) de Paris in 1978 and 1982 respectively in Electronic Engineering. In 1982, he joined the Ferdowsi University of Mashhad as Assistant Professor. In 1998 he was promoted to an Associate Professor. In 1990 and 2001 he was a visiting professor for one year at the University of Wales (Cardiff, UK), and the University of New South Wales (UNSW), Australia, respectively. His main field of interest is RF Circuits, particularly, non linear modeling, high power Amplifier, and LNA. Dr. Mafinezhad has authored or co-authored over 70 journal papers and international conferences articles and has written two books in electronics design. He is a member of editorial board of Iranian IEEE. He chaired the twelfth Iranian Conference on Electrical Engineering (ICEE).