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Distortion analysis of bootstrap switch using Volterra series

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Abstract: Linear behaviour of bootstrap switches is of critical importance in low-voltage analogue circuits and understanding the major factors affecting the linearity helps design a better switch. This study presents a theoretical approach for evaluating the distortion of bootstrap switches in the frequency domain based on the Volterra series. Five major factors affecting the linearity of the bootstrap switch are examined. In order to obtain a general design guideline the analysis is done in two parts. First, the distortion because of the non-linear $I-V$ characteristic of the main transistor of the switch is considered. In the second part, the distortion because of sampling errors, such as clock feed-through and charge injection, are added to the analysis. The theoretical results are verified by circuit simulations in a 0.18 μm CMOS process, using HSpice.

1 Introduction

The scaling of the physical dimensions of MOS devices into deep sub-micron regions and the reduction of the supply voltage aggravate the effect of the non-linear characteristics of MOS devices on the behaviour of analogue integrated circuits. Meanwhile, switched capacitor circuits are used in a variety of applications because of their robustness with regard to the impact of low supply voltage. In these circuits the performances of switches, especially the ones that are placed in the signal path, is of critical importance. Bootstrap switches are the best candidates for these applications since they can operate under a low supply voltage [1, 2]. The linearity of this kind of switches is crucial in many applications since they directly affect the overall linearity of the entire analogue circuit. Hence, understanding the sources of non-linearity and analysing the non-linear behaviour of bootstrap switches can help design a better switch [3].

In this paper, the sources of non-linearity in bootstrap switches are discussed and their harmonic distortion is thoroughly analysed. The analysis is done using Volterra series [4] and closed form equations are derived for the second and third harmonic distortion. The analytical results are compared with that of simulations in 0.18 μm CMOS technology using HSpice. General design rules for the bootstrap switch are also provided.

This paper is organised as follows: Section 2 presents a short summary on distortion analysis via Volterra series and provides the notation used throughout the rest of the paper. In Section 3, the bootstrap switch is discussed and the error sources that cause non-linearity are explained. Distortion analysis because of error sources are discussed in detail in Section 4. In Section 5, certain issues related with the design of bootstrap switch are discussed and design guidelines, for having high linearity performance, are given. Finally, conclusions are drawn in Section 6.

2 Volterra series and harmonic distortion

The non-linearity of a system can be obtained using the Volterra series. A non-linear system with input $x(t)$ and output $y(t)$ can be represented by Volterra series as the sum of infinite number of operators as the following [5]

$$y(t) = H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + \cdots \quad (1)$$

where $H_n[x(t)]$ is the nth-order operator with kernel h_n and is

obtained from the following equation

$$H_n[x(t)] = \int_{-\infty}^{+\infty} \dots \int_{-\infty}^{+\infty} h_n(\tau_1, \tau_2, \dots, \tau_n) x(t-\tau_1) \dots x(t-\tau_n) \mathrm{d}\tau_1 \dots \mathrm{d}\tau_n \quad (2)$$

Using Volterra series expansion, it is possible to find the response of a system to a sinusoidal input. It can be shown that when a non-linear system is excited by a sine wave $A\cos(\omega t)$ the output of the second-order non-linearity is given by [3]

$$y_2(t) = \frac{A^2}{2}|H_2(\omega, \omega)|\cos\{2\omega t + \arg(H_2(\omega, \omega))\} + \frac{A^2}{2}H_2(\omega, \omega) \quad (3)$$

where $H_2(\omega, \omega)$ is the Fourier transform of the second-order Volterra kernel. According to the above equation, the output of the second-order non-linearity consists of a constant term and a sinusoidal term at frequency 2ω.

Also, the output of the third-order non-linearity is [3]

$$y_3(t) = \frac{A^3}{4}|H_3(\omega, \omega, \omega)|\cos\{3\omega t + \arg(H_3(\omega, \omega, \omega))\} + \frac{3A^3}{4}H_3(\omega, \omega, -\omega)\cos\{\omega t + \arg(H_3(\omega, \omega, -\omega))\} \quad (4)$$

where $H_3(\omega, \omega, \omega)$ is the Fourier transform of the third-order Volterra kernel. As can be seen in (4), the response consists of components at frequencies 3ω and ω. Here, because of weak non-linearity operation of the device, we ignore the effect of spectral leakage from the third-order non-linearity to the first order.

According to (2) and (3), the second-order and third-order harmonic distortions (HD_2 and HD_3), as defined in [3], can be related to the Volterra kernels as the following

$$HD_2 = \frac{A}{2}\frac{H_2(\omega, \omega)}{H_1(\omega)}, \quad HD_3 = \frac{A^2}{4}\frac{H_3(\omega, \omega, \omega)}{H_1(\omega)} \quad (5)$$

In the above equation, $H_1(\omega)$ is the Fourier transform of the first-order Volterra kernel. Therefore obtaining the Volterra series kernels is key in calculating the harmonic distortion of a non-linear system [3].

3 Error sources of the bootstrap switch

Bootstrap switches are used in very-low-voltage applications where there is not enough voltage to keep the switch on for all the input signal range. The schematic of a typical bootstrap switch is shown in Fig. 1 [6]. In this circuit the transistor M_{sw} is the main switch. Other switches, which

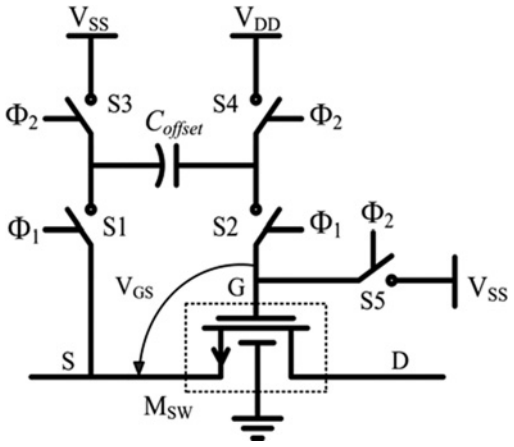

Figure 1 *Bootstrap switch model for distortion analysis in presence of sampling errors*

are controlled by two clock signals $\phi 1$ and $\phi 2$, can be implemented by a PMOS or an NMOS transistor. When the main transistor is off the capacitor C_{offset} is charged to V_{dd} and when M_{sw} is on C_{offset} is placed across the gate and source terminals of M_{sw}, hence providing a constant V_{GS} for the main switch that keeps it on irrespective of the input signal. Although a constant voltage drops across the gate and source terminals, the switch main transistor shows some non-linear behaviour. The main factors causing this non-linearity are introduced below.

1. *Threshold voltage variations:* One of the main reasons of the non-linearity of the bootstrap switch is the variation of the threshold voltage of the switch transistor M_{sw} with input signal. The conductance of the switch transistor g_{ds} can be found from the following equation

$$g_{ds} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th}) \quad (6)$$

where μ_n is the electron mobility, C_{ox} is the gate capacitance per unit area, W and L are the width and length of the transistor, V_{GS} is the gate-source voltage and V_{th} is the threshold voltage of the transistor. As can be seen in Fig. 1, the source of M_{sw} is not connected to the bulk, and therefore V_{th} in (6) becomes a function of the input voltage. This in turn causes g_{ds} to become a function of the input voltage and M_{sw} shows non-linear behaviour.

2. *The parasitic gate capacitance:* Another factor causing non-linearity in a bootstrap switch is the parasitic capacitance at the gate of M_{sw}. Fig. 2 shows the switch in the on state along with the parasitic capacitance (C_j). In this circuit V_{GS} of M_{sw} can be found from the following equation

$$V_{GS} = \frac{C_{offset}}{C_{offset} + C_j}V_{dd} - \frac{C_j}{C_{offset} + C_j}V_{in} \quad (7)$$

According to (7) the gate-source voltage of M_{sw} is a function of V_{in} because of charge sharing between C_{offset} and C_j. This

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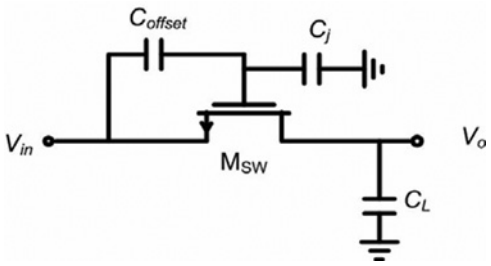

Figure 2 *Bootstrap switch model for distortion analysis*

causes non-linearity in the behaviour of the switch. The above two error sources are only related to the MOS $I-V$ characteristic and switch structure, not to sampling phenomenon. The following three error sources are due to charge sampling.

3. *Clock feed-through:* Another source of error causing non-linearity is the clock feed-through. In the circuit of Fig. 1 the switching happening at the gate of M_{sw} affects the output voltage. Since the gate voltage depends on V_{in} because of C_{offset}, the error caused by the clock feed-through becomes a function of the input voltage and causes non-linearity. The error at the output voltage because of clock feed-through (ΔV_{ocf}) can be shown to be

$$\Delta V_{ocf} = \left(\frac{C_{gd}}{C_{gd}+C_L}\right)\underbrace{\left(\frac{C_{offset}}{C_{offset}+C_j}\right)}_{\beta_1}(V_{DD}+V_{in}) \quad (8)$$

where C_{gd} is the overlap capacitance of the gate and drain terminals and C_L is the load capacitance.

4. *Charge injection:* When a MOSFET turns off the channel charge should be depleted from source and drain terminals. In the worst case if we assume that all the channel charge goes to the output then the error voltage would be

$$Q_{ch} = WLC_{ox}(V_{GS}-V_{th}) \Rightarrow \Delta V_{och} = \frac{WLC_{ox}}{C_L} \times \left(V_{GS}-V_{th0}-\gamma\left(\sqrt{2\phi_F+V_{in}}-\sqrt{2\phi_F}\right)\right) \quad (9)$$

where γ is the body effect coefficient and $2\phi_F$ denotes the surface potentials. As can be seen ΔV_{och} is a function of V_{in} and hence is a source of non-linearity.

5. *Non-zero fall time of the clock:* The non-zero fall time of the gate voltage of M_{sw} is another source of error. As a result of this non-zero fall time, the instant at which M_{sw} turns off becomes a function of the input voltage. To model this error correctly, the switch is represented as a time-varying system with time-varying Volterra series [4] used for analysis.

Previous works on switch distortion analysis have focused only on the non-linear $I-V$ characteristics of the transistor [4, 7]. In these works the body effect, which has an important role on the output distortion, is ignored. As will be shown later in this paper, the body effect is critical in the non-linearity of the bootstrap switch. Moreover, the non-linearity because of other factors explained above is generally ignored in the previous analyses. In the following section, we calculate the distortion of the bootstrap switch considering the first four of the above-mentioned factors causing non-linearity.

4 Distortion analysis of bootstrap switch

In this section, the distortion analysis of the bootstrap switch is presented. The analysis is done in two separate parts. First, we only consider the initial two error sources mentioned in Section 3. In the second part, the last three sources of non-linearity mentioned in Section 3 are added to the distortion analysis.

4.1 Analysis of the distortion because of $I-V$ non-linear characteristic

To determine the harmonic distortion because of switch non-linearity, we assume that the switch time-constant is much smaller than the sampling period. Using this assumption, the output voltage of the switch reaches a steady-state value within several time-constants after the switch turns on. To eliminate the errors because of the switching phenomenon, we assume that switch passes the input signal to the output continuously and there is no switching. In other words, we consider the bootstrap switch only in the sampling phase. Hence, we can ignore the impact of the clock feed-through and charge injection in the first part of the following analysis.

As shown in Fig. 2 by considering the KCL at the output node, the differential equation governing the output voltage can be found as the following

$$I_D = -C_L\frac{dV_o}{dt} \Rightarrow \mu_n C_{ox}\frac{W}{L}\left(\frac{C_{offset}}{C_{offset}+C_j}V_{dd} - \frac{C_j}{C_{offset}+C_j}V_{in} - V_{th0} - \gamma\left(\sqrt{2\phi_F+V_{in}}-\sqrt{2\phi_F}\right)\right)(V_o-V_{in}) - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_o-V_{in})^2 = -C_L\frac{dV_o}{dt} \quad (10)$$

To handle the term containing the root square of the input signal, we approximate the threshold voltage by its Taylor series. That is

$$V_{th} = V_{th0} + \gamma\sqrt{2\phi_F}\left[\frac{V_{in}}{4\phi_F} - \frac{V_{in}^2}{8(2\phi F)^2}\right] \quad (11)$$

We now express the output voltage $V_o(t)$ by its Volterra series, that is, $V_o(t) = V_1(t) + V_2(t) + V_3(t) + \ldots$, where

$V_n(t) = H_n[V_{in}(t)]$, and substitute it in (10) along with (11). Manipulating the equation and keeping only the first-, second- and third-order terms, we obtain

$$k(\beta_1 V_{dd} - \beta_2 V_{in} - V_{th0} - \beta_3 V_{in} + \beta_4 V_{in}^2)(V_1 + V_2 + V_3 - V_{in}) - \frac{k}{2}((V_1 + V_2 + V_3)^2 - 2(V_1 + V_2 + V_3)V_{in} + V_{in}^2) = -C_L \frac{d}{dt}(V_1 + V_2 + V_3) \quad (12)$$

where k, β_1, β_2, β_3, β_4 are found to be

$$k = \mu_n C_{ox} \frac{W}{L}, \quad \beta_1 = \frac{C_{offset}}{C_{offset} + C_j}, \quad \beta_2 = \frac{C_j}{C_j + C_{offset}}, \quad \beta_3 = \frac{\gamma}{2\sqrt{2\phi_F}}, \quad \beta_4 = \frac{\gamma}{8(2\phi_F)^{3/2}}$$

Note that V_{in} is a first-order term, the term V_1^2 is a second-order term and V_1V_2 is a third-order term. Now, by equating the terms of the same order on each side of (12), differential equation of each Volterra kernel is obtained. The related equations are shown in (13). Solving this set of equations gives the Volterra kernels H_1, H_2 and H_3, which are shown in (14)–(16). Substituting (14)–(16) into (5) yields the second- and third-order harmonic distortion

$$\begin{cases} C_L \frac{dV_1}{dt} + k(\beta_1 V_{dd} - V_{th0})V_1 = k(\beta_1 V_{dd} - V_{th0})V_{in} \\ C_L \frac{dV_2}{dt} + k(\beta_1 V_{dd} - V_{th0})V_2 = k(\beta_2 + \beta_3)V_{in}(V_1 - V_{in}) + \frac{k}{2}(V_1^2 - 2V_1V_{in} + V_{in}^2) \\ C_L \frac{dV_3}{dt} + k(\beta_1 V_{dd} - V_{th0})V_3 = k(\beta_2 + \beta_3)V_{in}V_2 + k\beta_4(V_{in}^3 - V_{in}^2V_1) + k(V_1V_2 - V_2V_{in}) \end{cases} \quad (13)$$

$$H_1(\omega_1) = \frac{k(\beta_1 V_{dd} - V_{th0})}{k(\beta_1 V_{dd} - V_{th0}) + j\omega_1 C_L} \quad (14)$$

see (15))

see (16))

To verify the analytical results, a bootstrap switch as shown in Fig. 2 is designed. The transistors' dimensions, capacitor values, input signal amplitude and the threshold voltage non-linearity coefficients are summarised in Table 1 for this design. The switch is then simulated in the 0.18 μm CMOS technology using BSIM3v3 device model. The transistor level simulations are done using HSpice. The above equations are also plotted with Maple. The results for HD_2 and HD_3 are illustrated in Fig. 3.

Table 1 Design parameters for circuits in Fig. 1

Parameter	Value
W/L	10 μm/0.18 μm
C_{offset}	5 pF
C_j	50 fF
input signal amplitude	0.9
β_3	0.22
β_4	0.0195

As can be seen in Fig. 3, the results obtained from the above analysis are in a good agreement with those of the simulation. In the case of HD_3, the two results are a bit different at frequencies above 100 MHz. (This frequency is very close to the pole frequency of HD_3 [8]). This can be due to the fact not all the parasitic capacitances are accurately modeled and hence, at very high frequencies, the analytical results deviate from those of the simulation.

4.2 Analysis of the distortion because of I–V non-linear characteristic and sampling errors

As mentioned above, previous works on switch distortion analysis have focused only on the non-linear I–V

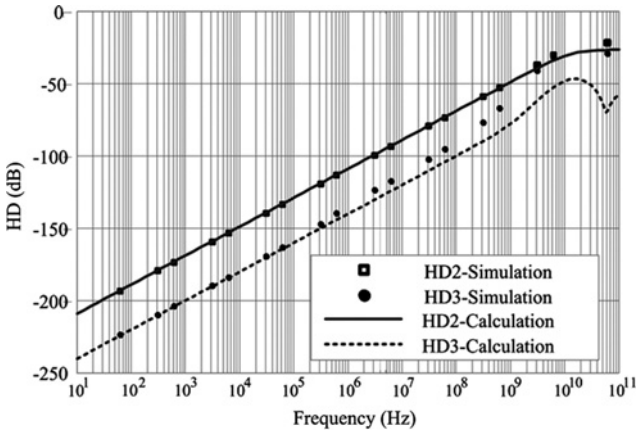

Figure 3 *Simulation results and calculation results of bootstrap switch harmonic distortion without sampling errors*

$$H_2(\omega_1, \omega_2) = \frac{K/2H_1(\omega_1)H_1(\omega_2) - k(\beta_2 + \beta_3 - 1/2) + k(\beta_2 + \beta_3 - 1)H_1(\omega_1)}{k(\beta_1 V_{dd} - V_{th0}) + j(\omega_1 + \omega_2)C_L} \quad (15)$$

$$H_3(\omega_1, \omega_2, \omega_3) = \frac{k(\beta_2 + \beta_3 - 1)H_2(\omega_1, \omega_2) + k\beta_4(1 - H_1(\omega_1)) + kH_1(\omega_1)H_2(\omega_2, \omega_3)}{k(\beta_1 V_{dd} - V_{th0}) + j(\omega_1 + \omega_2 + \omega_3)C_L} \quad (16)$$

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characteristics of the transistor [4, 7, 9] and the sampling errors were generally not considered. Now we consider the first four factors mentioned in Section 3 causing non-linearity in the bootstrap switch.

As discussed earlier, clock feed-through introduces an error in the sampled output voltage. If we assume that C_{gd} is constant the error ΔV_{ocf} (as given by (8)) is dependent on the input level, representing itself as a constant offset voltage as well as a first-order error in the input/output characteristic. The channel charge injection is another source of sampling error. As mentioned before, the total charge in the inversion layer is given by the following equation

$$Q_{ch} = \mathrm{WLC_{ox}}(V_{GS} - V_{th}) = C_{ch}\left(\frac{C_{offset}}{C_{offset}+C_j}V_{dd} - \frac{C_j}{C_{offset}+C_j}V_{in} - V_{th0} - \gamma\left(\sqrt{2\phi_F + V_{in}} - \sqrt{2\phi_F}\right)\right) \quad (17)$$

where C_{Ch} is equal to $\mathrm{WLC_{ox}}$ and represents the transistor channel capacitance. As a worst-case estimate, we assume that the entire charge is injected onto the sampling capacitor. We also approximate the threshold voltage by the first three terms of its Taylor series. This leads to the following equation for the error caused by the channel charge injection (ΔV_{ochi})

$$\Delta V_{ochi} = \left(\frac{C_{ch}}{C_L}\right)(\beta_1 V_{DD} - \beta_2 V_{in} - V_{th0} - \beta_3 V_{in} + \beta_4 V_{in}^2 - \beta_5 V_{in}^3) \quad (18)$$

In the above equation $\beta_5 = 3\gamma/(48(2\Phi_F)^{5/2})$. Equation (18) shows that the charge injection error introduces an offset at the output voltage as well as non-linearity in the input/output characteristic.

Now from (8) and (18) the total sampling error voltage at the output is equal to

$$\Delta V_{ot} = \underbrace{\left[\left(\frac{C_{gd}}{C_{gd}+C_L}\right)\beta_1 V_{dd} + \frac{C_{ch}}{C_L}\beta_1 V_{dd} - \frac{C_{ch}}{C_L}V_{th0}\right]}_{\text{DC component}} + \underbrace{\left[\left(\frac{C_{gd}}{C_{gd}+C_L}\right)\beta_1 - \frac{C_{ch}}{C_L}(\beta_2+\beta_3)\right]V_{in}}_{\text{First-order component}} - \underbrace{\frac{C_{ch}}{C_L}\beta_4 V_{in}^2}_{\text{Second-order component}} + \underbrace{\frac{C_{ch}}{C_L}\beta_5 V_{in}^3}_{\text{Third-order component}} \quad (19)$$

Equation (19) shows the effect of charge injection and clock feed-through errors on the output voltage. Using the superposition theory and combining (19) and (14) to (16), the transfer function for each harmonic can be obtained. These equations are shown in (20)–(22)

$$H_1(\omega_1) = \frac{k(\beta_1 V_{dd} - V_{th0})}{k(\beta_1 V_{dd} - V_{th0}) + j\omega_1 C_L} - \left[\left(\frac{C_{gd}}{C_{gd}+C_L}\right)\beta_1 - \frac{C_{ch}}{C_L}(\beta_2+\beta_3)\right] \quad (20)$$

see (21))

see (22))

In order to verify the above analysis the circuit of Fig. 1 is used for simulation. Switches S1–S5 are realised with ideal switches to eliminate the impact of any undesired non-ideal behaviour of these switches. By using an ideal switch for S5 the fall time error of the gate voltage is eliminated. The circuit parameters are as shown in Table 1. The circuit is simulated in 0.18 μm CMOS technology and HD_2 and

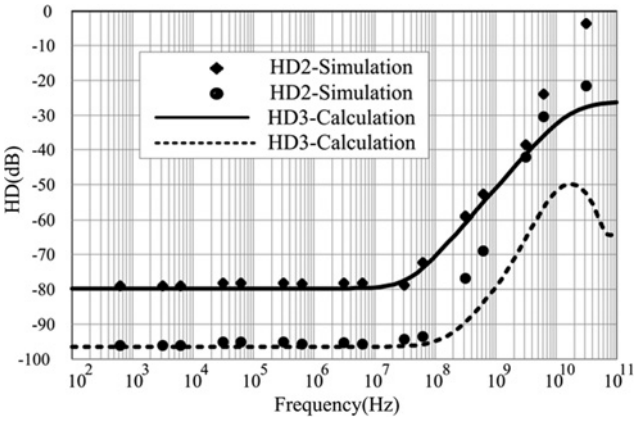

Figure 4 *Simulation results and calculation results of bootstrap switch harmonic distortion with sampling errors*

$$H_2(\omega_1, \omega_2) = \frac{K/2H_1(\omega_1)H_1(\omega_2) - k(\beta_2+\beta_3-1/2) + k(\beta_2+\beta_3-1)H_1(\omega_1)}{k(\beta_1 V_{dd} - V_{th0}) + j(\omega_1+\omega_2)C_L} + \frac{C_{ch}}{C_L}\beta_4 \quad (21)$$

$$H_3(\omega_1, \omega_2, \omega_3) = \frac{k(\beta_2+\beta_3-1)H_2(\omega_1, \omega_2) + k\beta_4(1 - H_1(\omega_1)) + kH_1(\omega_1)H_2(\omega_2, \omega_3)}{k(\beta_1 V_{dd} - V_{th0}) + j(\omega_1+\omega_2+\omega_3)C_L} - \frac{C_{ch}}{C_L}\beta_5 \quad (22)$$

HD_3 are obtained at different input frequencies. The sampling frequency is chosen to be equal to the Nyquist frequency. The simulation results are compared with that of the calculation in Fig. 4. Clearly, there is a good agreement between the simulation results and those obtained from (20) to (22) and (5) for a wide range of frequencies. However, at very high frequencies the calculated results deviates from those of the simulation. This is due to the assumption that the assumption that the time constant of the switch is much smaller than the clock period no longer being true at very high frequencies.

5 Discussion

By comparing Figs. 3 and 4, it becomes clear that at low frequencies the impact of clock feed-through and charge injection are the main factors in determining HD_2 and HD_3. Therefore in the low-frequency range increasing the load capacitance and decreasing the size of the switch reduces the impact of these two factors and increases the switch linearity. However, at high frequencies HD_2 and HD_3 are mainly determined by the non-linearity of switch $I-V$ characteristics. Hence, at high frequencies it is better to reduce the load capacitance and increase the switch size to have a larger conductance.

Moreover, according to (21) and (22) the charge injection has a negative impact on the linearity of the switch which is due to the threshold voltage variations. This suggests that if the source-bulk voltage of the main switch can be kept constant then the impact of charge injection would be mainly eliminated on the second- and third-order harmonics and switch behaves more linearly at the low-frequency range.

By examining (20), it becomes obvious that by choosing an appropriate value for the load capacitance it is possible to make the second term in (20) zero. In this way, the impact of the sampling phenomenon on the first-order terms is cancelled. The value of the load capacitance which satisfies this condition is

$$C_L = \frac{C_{gd}C_{ch}(\beta_2 + \beta_3)}{C_{gd}\beta_1 - C_{ch}(\beta_2 + \beta_3)} \tag{23}$$

In some applications, such as bio-implantable ICs, in order to minimise power consumption, it is desirable to use very low supply voltages [10]. According to (20)–(22), by decreasing the supply voltages, the poles (roots of the denominator) of each harmonic decreases too. It means that the maximum input frequency for a given clock frequency is reduced, which is not desirable. To solve this problem for low-voltage application, it is better to use clock boosting technique to increase the gate-source voltage.

6 Conclusion

A detailed distortion analysis of the bootstrap switch circuit has been presented. Error sources of this switch has been determined and discussed individually. These error sources were divided in two parts: error sources because of $I-V$ non-linear characteristics of switch and error sources resulting from the sampling phenomenon. Considering these error sources, distortion analysis of bootstrap switch circuit: with and without sampling errors was presented and a closed-form expression of output HD_2 and HD_3 was derived. Certain issues relating to the design of bootstrap switch were discussed and design guidelines for obtaining higher linearity were presented.

7 References

[1] ABO A.M., GRAY P.R.: 'Design for reliability of low-voltage, switched-capacitor circuits'. PhD dissertation, University of California, Berkeley, CA, 1999

[2] STEENSGAARD J.: 'Bootstrapped low-voltage analog switches'. Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), 1999, vol. 2, pp. 29–32

[3] WAMBACQ P., SANSEN W.: 'Distortion analysis of analog integrated circuits' (Kluwer, Norwell, MA, 1998)

[4] YU W., SEN S., LEUNG B.H.: 'Distortion analysis of MOS track-and-hold sampling mixers using time-varying volterra series', *IEEE Trans. CAS II*, 1999, **46**, (2), pp. 101–113

[5] SCHTZEN M.: 'The Volterra and Wiener theories of nonlinear systems' (Wiley, New York, 1980)

[6] DESSOUKY M., KAISER A.: 'Very low-voltage digital-audio modulator with $\Delta\Sigma$ 88-dB dynamic range using local switch bootstrapping', *IEEE J. Solid-State Circuits*, 2001, **36**, (3), pp. 349–355

[7] GOTHENBERG A., TENHUNEN H.: 'Performance analysis of sampling switches in voltage and frequency domains using Volterra series'. ISCAS, 2004, pp. 765–768

[8] BROWN T., HAKKARAINEN M., FIEZ T.S.: 'Prediction and characterization of frequency dependent MOS switch linearity and the design implications'. 2006 IEEE Custom Integrated Circuits Conf., September 2006, pp. 237–240

[9] AKSIN D., AL-SHYOUKH M., MALOBERTI F.: 'Switch bootstrapping for precise sampling beyond supply voltage', *IEEE J. Solid-State Circuits*, 2006, **41**, (8), pp. 1938–1943

[10] CHEUNG V.S.L., LUONG H.C.: 'A 0.9 V 0.5 W CMOS single-switched-op-amp signal-conditioning system for pacemaker applications'. Proc. IEEE Int. Solid-State Circuits Conf., February 2003, vol. 1, pp. 408–409

doi: 10.1049/iet-cds.2008.0354