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Modelling and Controller Design for a Non-inverting Buck-Boost Chopper

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Abstract— **Due to its simplicity, low voltage stress, high reliability, low switch and inductor losses, and small inductor size, the non-inverting buck-boost chopper has found a lot of attentions in applications where it is necessary to step-up or step-down the DC voltage. In this paper, a successful switching strategy for this converter is reported and small signal averaged state-space model is obtained, which lets decide about the control strategy and analyse the stability and performance of the closed loop control system. Appropriate control requirements have been defined and the closed loop performance under several control strategies has been investigated through extensive simulations.**

Keywords— **Small signal averaged model, non-inverting buck-boost chopper, control.**

I. Introduction

As the demand for battery charge controllers increases, so different kinds of design solutions are proposed. Traditionally the buck converter topology is used as a DC to DC converter to provide the controlled output power supply to the batteries. But in many applications such as renewable generations, due to the wide variations of energy source output voltage, it is often necessary either to step-up or step-down the output voltage. Several topologies are capable of both step-up and step-down the voltage [1].

Thanks to its simplicity, low voltage stress, high reliability, low switch and inductor losses, and small inductor size, the non-inverting buck-boost chopper has found a lot of attentions [2-7]. As depicted in Fig. 1, the non-inverting buck-boost chopper is often implemented with diodes; however, in order to increase the efficiency, it might be advantageous to replace the diodes with transistors.

In this work, the small signal averaged equations of a non-inverting buck-boost chopper are derived. Accordingly the small signal equivalent model is developed which lets decide about the control strategy and analyse the stability and performance of the closed loop control system. As it will be shown, this converter, as an indirect energy transfer type, suffers from the presence of a right half-plane zero when operated in CCM. Then, this work deals with control difficulties arisen from this right half-plane zero. Appropriate control requirements have been defined and the closed loop performance under several control strategies has been investigated through extensive simulations.

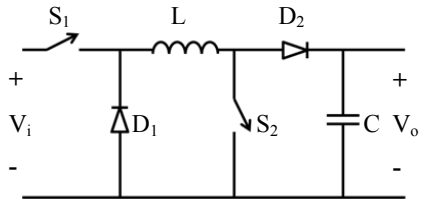

Fig. 1 Non-inverting buck-boost chopper

II. Switching Strategy

The non-inverting buck-boost converter is controlled by two PWM signals. As summarized in Table 1, one can use this converter as a buck converter, as a boost converter or as a buck-boost converter by selecting different combinations of switches S_1 and S_2.

TABLE I
Operation Modes According to Switch Combinations

Mode	**S_1**	**S_2**
buck	switching with D_1	off ($D_2 = 0$)
boost	on ($D_1 = 1$)	switching with D_2
buck-boost	switching with D_1	switching with D_2 ($D_2 < D_1$)

If the duty cycles of PWM signals driving S_1 and S_2 are D_1 and D_2, respectively, then the output DC voltage V_o is given by the following formula:

$$\frac{V_o}{V_i}=\frac{D_1}{(1-D_2)}\quad\begin{cases}D_1+D_2>1:\text{Step}-\text{up}\\ D_1+D_2<1:\text{Step}-\text{down}\end{cases}\tag{1}$$

In the buck-boost operation mode, if S_2 becomes on while S_1 is off, the inductance will be shorted by D_1 and the short circuit current may damage the diode or the inductance. To avoid this situation, D_2 must be always smaller than D_1. Indeed, S_2 must receive the switching signal if only S_1 is on.

Fig. 2 shows a switching strategy to realize the reference voltage. The PWM pulses are generated by intersection of the reference signal and two overlapped carrier signals. Because in buck-boost mode, both S_1 and S_2 are switched on and off, the losses are higher than buck or boost modes. So, a narrower range of buck-boost operation means a higher efficiency.

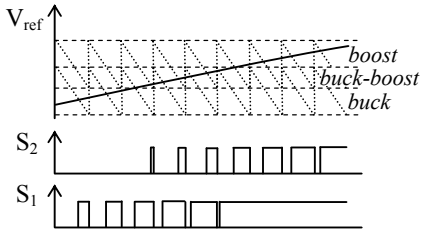

Fig. 2 PWM pulse generation

III. Small signal averaged model

Given a PWM converter, operating in the continuous conduction mode, in each switching position, the converter reduces to a linear circuit that can be described by independent state equations. During consequent subintervals, the circuit elements are connected differently; therefore, the respective state equation matrices differ. Given these state equations, the result of state-space averaging is the state equations of the equilibrium and small-signal AC models. Provided that the natural frequencies of the converter, as well as the frequencies of variations of the converter inputs are much lower than the switching frequency, then the small signal averaged model is a valid representative of converter performance in response to small AC variations about the equilibrium operating point.

For the converter of Fig. 1, there are three distinct switching states as follows:

1) Both S_1 and S_2 conduct ($0 < t < D_2T$):

$$\begin{cases}\dfrac{dv_o}{dt}=\dfrac{1}{C}\left(-\dfrac{v_o}{R}\right)\\ \dfrac{di_L}{dt}=\dfrac{1}{L}(v_i)\end{cases}\tag{2}$$

2) Only S_1 conducts and S_2 does not receive the switching pulse ($D_2T < t < D_1T$):

$$\begin{cases}\dfrac{dv_o}{dt}=\dfrac{1}{C}\left(i_L-\dfrac{v_o}{R}\right)\\ \dfrac{di_L}{dt}=\dfrac{1}{L}(v_i-v_o)\end{cases}\tag{3}$$

3) Both S_1 and S_2 are off ($D_1T < t < T$):

$$\begin{cases}\dfrac{dv_o}{dt}=\dfrac{1}{C}\left(i_L-\dfrac{v_o}{R}\right)\\ \dfrac{di_L}{dt}=\dfrac{1}{L}(-v_o)\end{cases}\tag{4}$$

Based on equations (2)-(4), the small signal averaged state-space model is obtained as bellow, in which the variables with a hat are small AC variations about the equilibrium operating point:

$$\begin{pmatrix}\dfrac{d\hat{v}_o}{dt}\\ \dfrac{d\hat{i}_L}{dt}\end{pmatrix}=\begin{pmatrix}-\dfrac{1}{RC} & \dfrac{(1-D_2)}{C}\\ -\dfrac{(1-D_2)}{L} & 0\end{pmatrix}\begin{pmatrix}\hat{v}_o\\ \hat{i}_L\end{pmatrix}+\begin{pmatrix}0 & -\dfrac{I_L}{C}\\ \dfrac{V_i}{L} & \dfrac{V_o}{L}\end{pmatrix}\begin{pmatrix}\hat{d}_1\\ \hat{d}_2\end{pmatrix}+\begin{pmatrix}0\\ \dfrac{D_1}{L}\end{pmatrix}\hat{v}_i\tag{5}$$

Applying the Laplace transform to (5) and adding the effect of output capacitor ESR (R_{ESR}), to the following small signal transfer function of the output voltage variation due to input voltage and duty cycles changes will be obtained:

$$\begin{aligned}\hat{v}_o=&\frac{(1-D_2)V_i(1+R_{ESR}Cs)/LC}{s^2+s/RC+(1-D_2)^2/LC}\hat{d}_1\\ &+\frac{I_L/C\left(V_iD_1/LI_L-s\right)(1+R_{ESR}Cs)}{s^2+s/RC+(1-D_2)^2/LC}\hat{d}_2\\ &+\frac{(1-D_2)D_1/LC}{s^2+s/RC+(1-D_2)^2/LC}\hat{v}_i\end{aligned}\tag{6}$$

This transfer function has a right half-plane zero at $f_{Z,RHP}$, a left half-plane zero due to the capacitor ESR at $f_{Z,ESR}$, and two left half-plane poles at f_P: $f_{Z,RHP}=R(1-D_2)^2/(2\pi L)$, $f_{Z,ESR}=1/(2\pi R_{ESR}C)$, $f_P=(1-D_2)/\left(2\pi\sqrt{LC}\right)$.

The interesting point is that the frequency of double poles and the location of right half-plane zero are only determined by the boost switch duty cycle D_2.

Fig. 3 illustrates the magnitude and phase plots of $\hat{v}_o/\hat{d}_2$. Two apparent features are the resonance and the right half-plane zero. The physical origin of the right half-plane zero is the indirect energy transfer in boost operation. This converter must first store the energy in the inductor during a certain time before dumping it into the output capacitor during the rest of the switching period. If the duty cycle quickly changes in response to a perturbation, the inductor naturally limits the current slew rate and the output voltage drops.

IV. Controller design

Looking at Fig. 3, it is obvious that the phase margin is inadequate and a compensator is required to increase it.

The challenge of the controller design is that the right half-plane zero limits the crossover frequency, f_C, of the closed-loop non-inverting buck-boost converter.

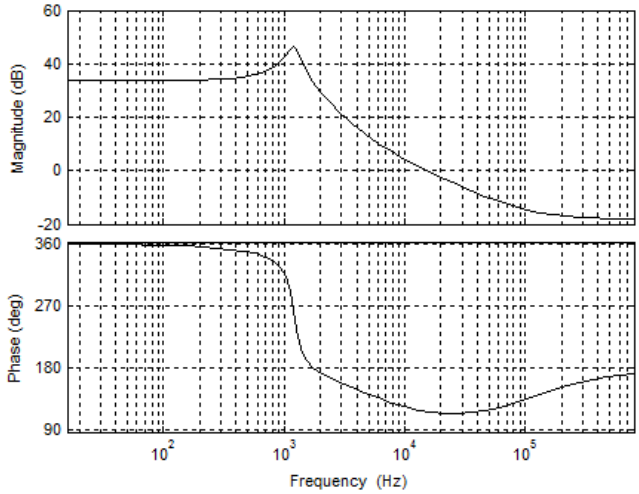

Fig. 3 Bode plot of $\frac{\hat{v}_o}{\hat{d}_2}$

A. PI Compensator

This compensator has a pole at origin and a zero that can be located at any desired frequency.

$$G_{PI} = K\frac{\left(s/\omega_Z + 1\right)}{s} \tag{7}$$

According to Bode plot of Fig. 3, there is a sharp phase drop around f_P which may move the phase bellow -180°. So, the only way to ensure the closed loop stability using a PI compensator is to choose the crossover frequency smaller than f_P. Indeed, f_C should be much smaller than f_P to guarantee that once the gain crosses the 0 dB axis the gain resonance peak will remain below 0 dB. A small crossover frequency means narrow available loop bandwidth and slow dynamics performance. A good compromise is to choose the crossover frequency one decade before the dual poles position (f_P). Hereby, in expense of a narrow bandwidth, a positive phase margin, some value about 90°, will be assured and at the same time an adequate gain margin will be provided.

On the other hand, due to the high value of the available phase margin at the selected crossover frequency, there is no need to compensate the negative phase induced by the compensator origin pole. So, the compensator zero will be located beyond f_P to ensure that it has no effect on the gain slope around the resonance frequency.

B. Type III Compensator

In order to achieve a higher bandwidth, type III compensation can be used. The compensator provides three poles and two zeros with one pole located at the origin:

$$G_{type3} = K\frac{\left(s/\omega_Z + 1\right)^2}{s\left(s/\omega_P + 1\right)^2} \tag{8}$$

This compensation provides two zeros to cancel out the double poles and thus avoids sharply decreasing phase margin and effectively increases the phase angle at the crossover frequency. In addition, it contributes one dominant pole at origin and two high-frequency poles. The pole at the origin increases the regulation. The two high-frequency poles are intended to compensate for the effects of $f_{Z,ESR}$ and to control the gain slope beyond the crossover frequency. Because of the phase boost capability of this compensator, the crossover frequency can be chosen beyond f_P, therefore, compared to the PI compensation a higher bandwidth can be achieved.

There are some limitations when designing such a high order compensator for our converter system. The high-frequency poles of the compensator must be located before $f_{Z,ESR}$. In order to attain an increase of 60° to 90° in the phase at f_C, the crossover frequency should be one to two decades before the compensator poles position, also, the compensator zeros should be one to two decades before f_C. On the other hand, by choosing the frequency of the compensator poles enough smaller than the switching frequency, a good immunity of the closed loop system against the switching transients will be obtained.

V. Simulations and Performance Evaluation

The non-inverting buck-boost chopper of Fig. 1 is simulated with the parameters listed in Table 2.

TABLE II
Simulation Parameters

$\mathbf{V_i}$	4-18 V
$\mathbf{V_o}$	14 V
P	500 W
$\mathbf{f_S}$	50 kHz
L	1 μH
C	1.4 mF

The Bode plots of the closed loop system are shown in Figs. 4 and 5. It is clear that with a PI compensator the achievable loop bandwidth is limited to a small value; however a type III compensator can effectively increase the bandwidth. As shown in Figs. 6 and 7, a type III compensated chopper has a faster dynamic response and at the same time, experiences lower oscillations during transients.

VI. Conclusions

In this work, the small signal averaged state-space model of a non-inverting buck-boost chopper is developed which lets decide about the control strategy and analyse the stability and performance of the closed loop control system. This converter suffers from the presence of a right half-plane zero.

The implementation of two control strategies such as conventional PI and type III compensator and the relevant control requirements are thoroughly discussed. The closed loop performance has been investigated through extensive simulations.

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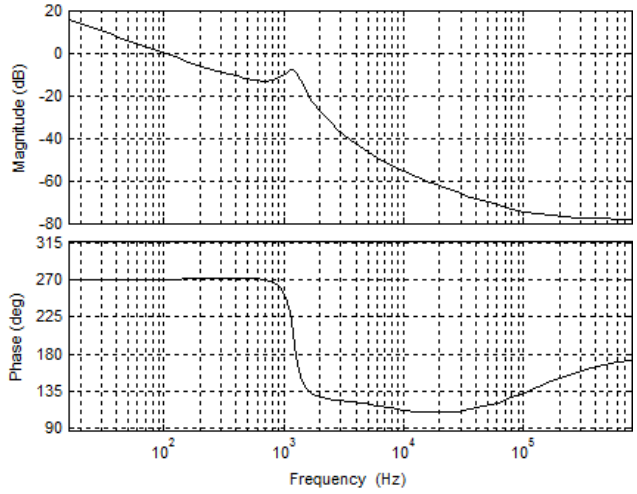
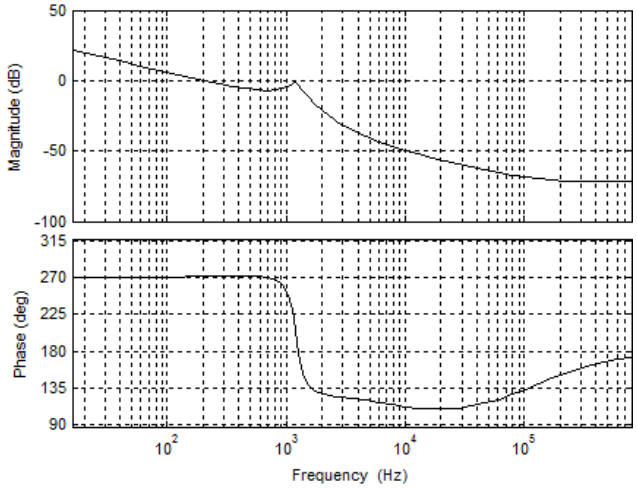


(a)



(b)

Fig. 4 Closed loop Bode plot of PI compensated chopper, a: f_C = 100 Hz, and b: f_C = 200 Hz

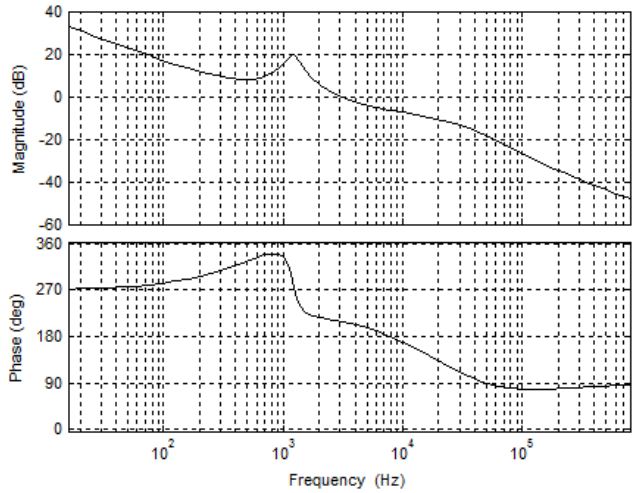
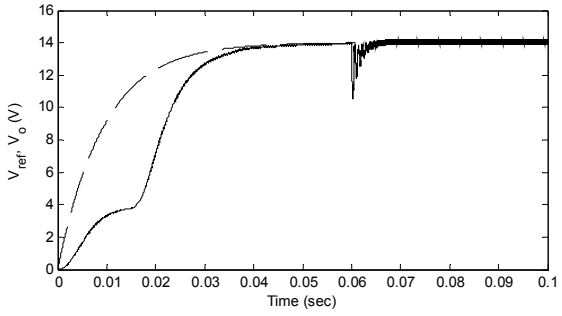


Fig. 5 Closed loop Bode plot of type III compensated chopper, f_C = 3 kHz



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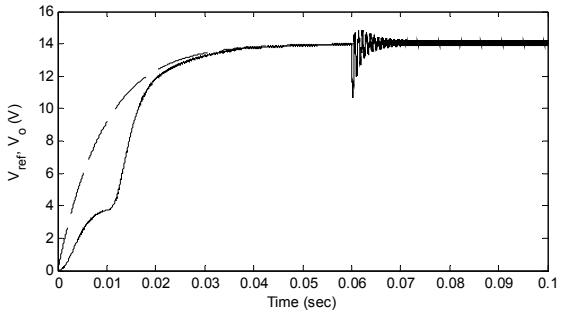

(b)

Fig. 6 Output voltage waveform of PI compensated chopper with load jump from 100 W to 500 W at t = 0.06 s, a: f_C = 100 Hz, and b: f_C = 200 Hz

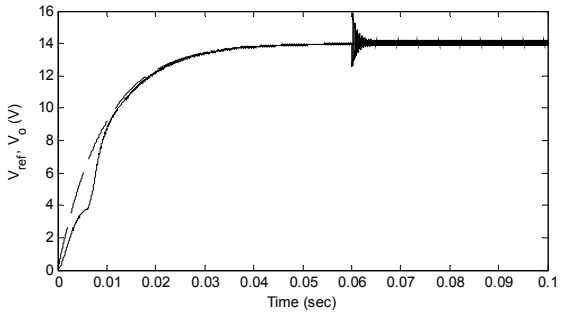

Fig. 7 Output voltage waveform of type III compensated chopper with load jump from 100 W to 500 W at t = 0.06 s, f_C = 3 kHz

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