DC and RF characteristics of SiC MESFETs with different channel doping concentrations under the gate

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Abstract. A Silicon carbide (SiC) metal semiconductor field effect transistor (MESFET) with step doping under the gate is proposed. The channel under the gate is divided into two Source Side (SS) and Drain Side (DS) regions with the same lengths and thicknesses, but with different doping levels. Changes that occur in the breakdown voltage, DC trans-conductance, drain current, gate-source capacitance, cut off frequency, and short channel effect as a function of different source side (N_{SS}) and drain side (N_{DS}) channel doping levels are studied in details. Simulation results illustrate that a larger N_{SS} compared to N_{DS} improves the breakdown voltage. On the other hand, decreasing N_{SS} reduces the gate-source capacitance. A larger channel doping concentration under the gate improves the short channel effect such as DIBL. With varying N_{SS} and N_{DS} the DC transconductance has a nonlinear variations. Also, simulation results demonstrate that NSS effects on the DC and RF characterization of SiC-MESFET is more than that of N_{DS}.

INTRODUCTION

The MESFET have drawn considerable attention in recent years due to its potentiality as a good contender of MOSFET in VLSI/ULSI technology because of the following device characteristics: enhanced radiation hardness, immunity to hot carrier aging, scaling well and less mobility degradation. The SiC MESFETs technology is a candidate for high power microwave applications. Its wide band gap and high thermal conductivity offer several advantages compared to Si- and GaAs-based technologies. SiC MESFETs are very well-suited for high voltage, high power and high temperature applications due to its superior material properties especially high critical electrical field, high electron saturation velocity, large band gap and high thermal conductivity. SiC MESFETs are emerging as a promising technology for high power microwave applications such as transmitters for commercial and military communications. This is made possible due to the superior properties of SiC and the relatively mature material growth and device fabrication technology. The main drawback in using SiC for microwave devices lies in its poor low field electron mobility of 300-500 cm²/volt.sec, at doping levels of interest for MESFETs in the range of 1×10^{17} - 5×10^{17} cm⁻³. This results in a larger source resistance and lower trans-conductance compared to GaAs based MESFETs [1-4].

In order to improve the transistor characteristics, in this paper, a non-uniform doping scheme is proposed for the channel of MESFET. In this scheme, the channel region under the gate is divided into two source and drain side regions with the same lengths and thicknesses, but with different doping levels. We investigate the effects of source/drain sides channel doping concentrations under the gate on the DC and RF performance of the SiC MESFET using extensive simulations.
1. DEVICE STRUCTURE

Fig. 1 shows the schematic cross-section of the conventional SiC MESFET[5],[6]. The dimensions of the structure are as follows: gate length \( L_g = 0.7 \, \mu m \), gate-drain spacing \( L_{gd} = 1 \, \mu m \), gate-source spacing \( L_{gs} = 0.5 \, \mu m \), channel thickness 0.25 \( \mu m \). Channel doping \( N_d = 3 \times 10^{17} \, cm^{-3} \) which is changed from \( N_d = 2 \times 10^{17} \, cm^{-3} \) to \( 4 \times 10^{17} \, cm^{-3} \) under the gate in the source/drain sides. The doping and thickness of the P-buffer layer are 1.4 \( \times 10^{15} \, cm^{-3} \) and 0.5 \( \mu m \), respectively. The substrate is semi-insulating. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV. The device is simulated using two dimensional ATLAS software[7] with SiC material parameters[8-10].

2. RESULTS AND DISCUSSION

2.1 Short Channel Effect

The device performance can be greatly improved by reducing the gate length to enhance the trans-conductance and reduce the gate capacitance. On the other hand as the technology is pushing the gate length to the sub-quarter micrometer range, short channel effects are becoming increasingly significant. One of the most pervasive short channel effects is the drain-induced barrier lowering (DIBL). DIBL is an electrostatic effect causing the barrier between the source and drain of a field effect transistor (FET) in or near the sub-threshold region to be lowered when the drain voltage is increased. This effect causes the channel to return from a pinch-off state to conduct and shifts the threshold voltage. Consequently, the DIBL places a hard limit on the minimum gate size and degrades the trans-conductance and output conductance, which are critical to the gain and power output for a power FET and the noise margin for a digital FET [11],[12].

Fig. 2 reveals that increasing \( N_{SS} \) and \( N_{DS} \) reduces the negative shift in the threshold voltage with increasing drain-source voltage. For example, according to this figure the negative shift in the threshold voltage with increasing the drain-source voltage for \( N_{SS} = N_{DS} = 2 \times 10^{17} \, cm^{-3} \) and \( N_{SS} = N_{DS} = 4 \times 10^{17} \, cm^{-3} \) are -5.6V and -5V respectively. Therefore, a larger channel doping concentration under the gate can be used to improve the short channel effect such as DIBL.

Fig. 2. Threshold voltage as a function of drain-source voltage for different \( N_{DS} \) and \( N_{SS} \).

2.2 DC Trans-Conductance

Fig. 3 illustrates the DC trans-conductance as a function of the \( N_{SS} \) for different \( N_{DS} \) at \( V_{DS}=5V \) and \( V_{GS}=0V \). As this figure shows, for small values of \( N_{DS} \) (2\( \times 10^{17} \, cm^{-3} \)), increasing \( N_{SS} \), increases the DC trans-conductance. But at higher values of \( N_{DS} \), DC trans-conductance decreases with increasing \( N_{SS} \). The maximum DC trans-conductance is obtained at \( N_{SS}=2\times 10^{17} \, cm^{-3} \) and \( N_{DS}=3\times 10^{17} \, cm^{-3} \).

The minimum DC trans-conductance is obtained at maximum values of \( N_{SS} \) and \( N_{DS} \) (4\( \times 10^{17} \, cm^{-3} \)). This is because larger doping concentration in the channel, degrade the carrier mobility and therefore, decreases the DC trans-conductance. Also, simulation results in the fig. 3 demonstrate that a higher \( N_{DS} \) increases the DC-trans-conductance variations for different values of \( N_{SS} \).
2.3 Gate-Source Capacitance

Simulated gate-source capacitances as a function of $N_{SS}$ for different values of $N_{DS}$ at $V_{DS} = 30$ V and $V_{GS} = 0$ V at frequency of 10 GHz are shown in the fig.4. As is shown in this figure, the gate-source capacitance reduction is significantly with decreasing the $N_{SS}$ at a constant $N_{DS}$ which improves the device performance at high frequencies. But varying the $N_{DS}$ at a fixed value of $N_{SS}$, changes the gate-source capacitance slightly. Smaller $N_{SS}$, increases depletion layer width between gate and source in the channel and then reduces the gate-source capacitance. The minimum gate-source capacitance is obtained at $N_{SS} = N_{DS} = 2 \times 10^{17}$ cm$^{-3}$. Therefore, decreasing $N_{SS}$ and $N_{DS}$ improves the gate-source capacitance. However, $N_{SS}$ effect is more pronounced than that of $N_{DS}$.

2.4 Cut-off and Maximum Oscillation Frequency

The cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) can be calculated from the below equations[6] where $g_m$ is the maximum DC trans-conductance and $c_{gs}$ is the gate-source capacitance.

\[
    f_T = \frac{g_m}{2\pi c_{gs}}
\]

\[
    f_{max} = \frac{f_T}{2} \sqrt{2 c_{gs}}
\]

These above equations show that a larger $g_m/c_{gs}$ ratio, improves the $f_T$ and $f_{max}$. Simulation results in the figs. 3 and 4 demonstrate that smaller $N_{SS}$ and $N_{DS}$, increases $g_m$ and decreases $c_{gs}$ which improves the $f_T$ and $f_{max}$. Minimum values of $f_T$ and $f_{max}$ are obtained at $N_{SS} = N_{DS} = 4 \times 10^{17}$ cm$^{-3}$ because $g_m$ is minimum and $c_{gs}$ has its maximum value. Also, it can be seen from figs. 3 and 4 that RF characteristics dependence on $N_{SS}$ is greater than that of $N_{DS}$.

2.5 Breakdown Voltage

Simulated breakdown voltages as a function of the $N_{SS}$ for different $N_{DS}$ at $V_{GS} = -1$ V is shown in the fig. 5. According to this figure, a larger $N_{SS}$ compared to $N_{DS}$ can be used to improve the breakdown voltage. A further investigation shows that the breakdown happens at the gate corner near the drain due to the electric field crowding [5], [6]. A smaller $N_{DS}$ reduces the maximum electrical field at the gate corner near the drain and increases the breakdown voltage. The maximum breakdown voltage occurs when $N_{SS}$ is maximum ($4 \times 10^{17}$ cm$^{-3}$) and $N_{DS}$ is minimum ($2 \times 10^{17}$ cm$^{-3}$). The minimum breakdown voltage is obtained at $N_{SS} = 2 \times 10^{17}$ cm$^{-3}$ and $N_{DS} = 4 \times 10^{17}$ cm$^{-3}$. As can be seen in the figure, the breakdown voltage improvement with increasing the $N_{SS}$ is higher compared to decreasing the $N_{DS}$. Therefore, the $N_{SS}$ value is an important factor in the breakdown voltage.
2.6 Drain Current

Simulated drain currents versus $N_{SS}$ for different values of $N_{DS}$ at $V_{DS} = 40$ V and $V_{GS} = 0$ V are shown in the fig. 6. Simulation results in this figure show that a larger $N_{SS}$ and $N_{DS}$ increases the saturated drain current because to allow for a high drain current, a large product of the channel doping and thickness ($N \times a$) is required [5], [6]. The device with $N_{SS}$=$4\times10^{17}$ cm$^{-3}$ and $N_{DS}$=$4\times10^{17}$ cm$^{-3}$ has maximum channel doping and therefore has maximum saturated drain current. Also, the minimum saturated drain current is achieved when the $N_{SS}$ and $N_{DS}$ are minimum ($2\times10^{17}$ cm$^{-3}$).

Increasing $N_{SS}$ at a constant $N_{DS}$, increases the saturated drain current significantly while increasing $N_{DS}$ at a constant $N_{SS}$, increases the saturation drain current slightly. Therefore, the $N_{SS}$ effect on the saturation drain current is more pronounced compared to the $N_{DS}$.

Fig. 6. Saturated drain current as a function of $N_{SS}$ for different $N_{DS}$ at $V_{DS}=40$V and $V_{GS}=0$V.

CONCLUSION

In conclusion, the effects of source/drain sides channel doping concentrations under the gate, on the device performance of SiC MESFETs are studied. Simulation results illustrate that at a constant $N_{DS}$, increasing $N_{SS}$, increases the breakdown voltage, saturated drain current and gate-source capacitance. The effect of $N_{SS}$ and $N_{DS}$ variations in the DC trans-conductance, cut-off frequency and maximum oscillation frequency is nonlinear. A larger channel doping concentration under the gate can be used to improve the short channel effect such as DIBL. However, the effect of $N_{SS}$ on the DC and RF characteristics is higher compared to the $N_{DS}$.

REFERENCES