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NOVEL STRUCTURES FOR CARBON NANOTUBE FIELD EFFECT TRANSISTORS

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A carbon nanotube field effect transistor (CNTFET) has been studied based on the Schrödinger–Poisson formalism. To improve the saturation range in the output characteristics, new structures for CNTFETs are proposed. These structures are simulated and compared with the conventional structure. Simulations show that these structures have a wider output saturation range. With this, larger drain-source voltage (Vds) can be used, which results in higher output power. In the digital circuits, higher Vds increases noise immunity.

Keywords: Carbon nanotube; FET; simulation; Schrödinger equation; CNT.

1. Introduction

Multi-wall carbon nanotubes (CNTs) were fabricated in 1991 for the first time.[1] Two years later, single wall nanotubes were produced.[2,3] A CNT is a sheet of graphite rolled-up as a tube, with a diameter typically in the nanometer range, which can be from less than one nanometer, up to several nanometers. CNTs are one dimensional (1D) devices in which electron transport is quasi ballistic. Moreover, mobility of CNTs is considerably larger than silicon, and can be as large as 10^5 cm^2/V $\cdot$ S.[4] These properties have promoted CNTs as a candidate for nanometer (10 nm) electronics technology.[5–10]

CNTs can be semiconducting or metallic according to the chiral vector.[11] In semiconducting CNTs, the bandgap decreases with increasing tube diameter, therefore, tubes of few nanometers in diameter can be used as channels for field effect transistors (FETs).

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In this paper, a CNT field effect transistor (CNTFET) with Schottky barrier contacts is simulated, and its characteristics are evaluated. Then, novel structures are proposed which have superior characteristics, both for digital and analogue applications. These transistors have a wider output saturation range. This means that these transistors can be used with higher supply voltages (higher Vds). With higher Vds, a transistor can deliver more power to the load in analogue applications. In digital applications, higher Vds results in higher noise immunity. This paper is outlined as follows. In Sec. 2, CNT parameters and the model used in our simulation is introduced. Section 3 deals with the I-V characteristics of a CNTFET. In Sec. 4, new structures are proposed and their I-V is discussed. Main conclusions are summarized in Sec. 5.

2. CNT Parameters and Transport Model

We consider a (16, 0) nanotube with radius $R_t = 0.6$ nm, bandgap $E_g = 0.62$ eV, dielectric constant $\varepsilon_t = 1$, and the tube length $L_t = 20$ nm. Due to the azimuthal symmetry of the tube, the simulation domain is two dimensional (2D). The gate insulator has $\varepsilon_{\text{ins}} = 25$ and thickness $R_g = 2.5$ nm. Dielectric constant of 25 is due to Zirconium oxide.[12] Drain and source metals make Schottky contact to the channel with $\Phi_{\text{M}} = 4.5$ eV. Figure 1 shows the CNTFET structure. This is the structure used in Ref. 13.

To derive I-V characteristics of the transistor, the 1D Schrödinger equation is solved consistently with the Poisson's equation. Poisson's equation with azimuthal symmetry is:

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho}\frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\varepsilon}\,. \tag{1}$$

In this equation, ρ is the tube axis direction, z is the channel direction, Q is the charge density on the tube surface and is derived from the Schrödinger equation. Poisson's equation is solved using finite difference discretization scheme with

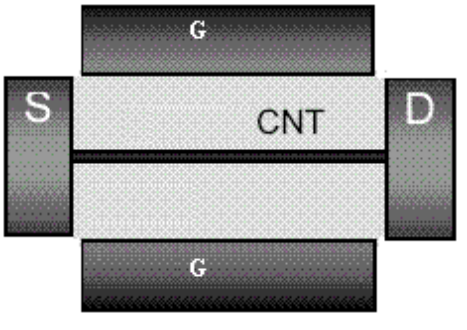

Fig. 1. CNTFET structure.

boundary conditions:

$$V(R_g, z) = V_{\mathrm{GS}} - V_{\mathrm{MS}} \tag{2}$$

$$V(\rho, 0) = -V_{\mathrm{MS}} \tag{3}$$

$$V(\rho, L_t) = V_{\mathrm{DS}} - V_{\mathrm{MS}}\,. \tag{4}$$

Where $V_{\mathrm{MS}} = (\Phi_{\mathrm{M}} - \Phi_{\mathrm{CN}})/q$, Φ_{M}, Φ_{CN} are metal and nanotube work functions respectively. The charge density is zero everywhere except at the tube surface:

$$Q = \frac{q(p-n)}{2\pi}\,\frac{\delta(\rho - R_t)}{\rho}\,. \tag{5}$$

Where n and p are electrons and hole densities respectively and are derived from the Schrödinger equation.

In a carbon nanotube, the electron transport is almost ballistic, therefore the Schrödinger equation is solved to compute the charge density and the transmission probability. The Schrödinger equation in one dimension is:

$$\frac{\partial^2 \Psi}{\partial z^2} = -\frac{2m}{\hbar^2}\,(E - U)\Psi\,. \tag{6}$$

Where E is the electrons or holes energy, U is the potential energy, which is $-qV$ for electrons and $qV + E_g$ for holes. The Schrödinger equation is solved using the central difference discretization method. In the drain and source metals (outside of the tube), Ψ is written as[13]:

$$\Psi = \begin{cases} Ae^{ik_{\mathrm{S}}z} + Be^{-ik_{\mathrm{S}}z} & z < 0 \\ Ce^{ik_{\mathrm{D}}z} + De^{-ik_{\mathrm{D}}z} & z > L_t\,. \end{cases} \tag{7}$$

Where k_{S} and k_{D} are wave vectors in the source and the drain contacts. For a wave traveling from the source to the drain (left to right), $A = 1$ and $D = 0$, and for a wave traveling from the drain to the source, $D = 1$ and $A = 0$. For the former case, the normalization factor is:

$$|N_{\mathrm{S}}|^2 = \frac{2mf_{\mathrm{S}}}{\pi\hbar^2 k_{\mathrm{S}}}\,. \tag{8}$$

The transmission probability is:

$$T = \frac{k_{\mathrm{D}}}{k_{\mathrm{S}}}|C|^2\,. \tag{9}$$

Solving the Schrödinger equation gives us the wave function for electrons and holes, hence electrons and holes density is computed from:

$$n(z) = \int_{E_n}^{\infty} dE(|N_{\mathrm{S}}|^2|\Psi_{e,\mathrm{S}}|^2 + |N_{\mathrm{D}}|^2|\Psi_{e,\mathrm{D}}|^2) \tag{10}$$

$$p(z) = \int_{E_h}^{\infty} dE(|N_{\mathrm{S}}|^2|\Psi_{h,\mathrm{S}}|^2 + |N_{\mathrm{D}}|^2|\Psi_{h,\mathrm{D}}|^2)\,. \tag{11}$$

The current from the source to the drain is computed from[14]:

$$I^{n,p} = \frac{4q}{\hbar} \int dE[f_{\mathrm{S}}^{n,p}(E) - f_{D}^{n,p}(E)]TC^{n,p}(E)\,. \tag{12}$$

Where the superscripts n and p stand for electron and hole respectively.

3. Current-Voltage Characteristics

For a conventional CNTFET depicted in Fig. 1, drain current (Id) versus the drain-source voltage (Vds) for various gate-source voltages (Vgs) is shown in Fig. 2. With $Vgs = 0.2$ V, for Vds up to 0.6 V, the output characteristics are similar to conventional FET transistors. But for larger Vds voltages, the drain current is suddenly increased. This is due to the hole injection from the drain to the source. As this figure shows, the saturation region in the output characteristics is about 0.6 V, which is small for typical applications. Figure 3 shows the electron potential energy for the gate voltage $Vgs = 0.4$ V and three values of the drain voltages. For $Vds = 0.2$ V, electrons surmount (or tunnel) through the source and drain Schottky barriers and produce the drain current. By increasing the drain voltage,

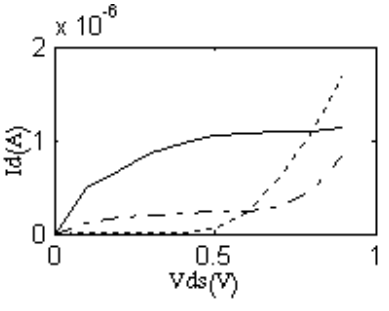

Fig. 2. Id–Vds for $Vgs = 0.2$ V (dot), 0.4 V (dash-dot) and 0.6 V (solid).

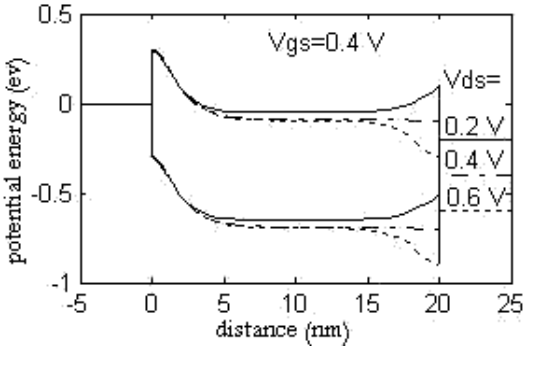

Fig. 3. Potential energy for $Vgs = 0.2$ V and $Vds = 0.2$ V (solid), 0.4 V (dash-dot) and 0.6 V (dot).

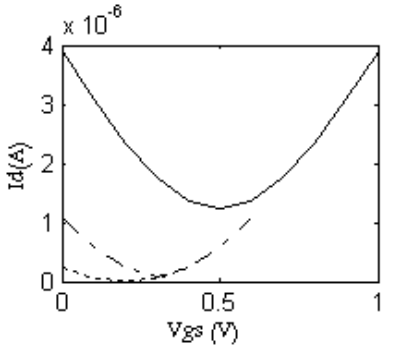

Fig. 4. Id–Vgs for $Vds = 0.4$ V (dot), 0.6 V (dash-dot) and 1.0 V (solid).

the potential on the drain side decreases and the electron current increases. At a special Vds, the drain barrier vanishes. If the Schottky barrier equals $E_g/2$, this occurs at $Vds = Vgs$. In Fig. 3, this happens for $Vds = 0.4$ V. For larger Vds values, the holes injection is increased. At $Vds = 2Vgs$, the holes and the electrons current coincide. Beyond $Vds = 2Vgs$, the holes current will increase exponentially, as is known for a Schottky diode.

Figure 4 shows the drain current versus gate voltage with drain voltage as parameter. For $Vgs = Vds/2$, the barrier height for electrons and holes is the same, and therefore corresponding currents coincide. For gate voltages less than $Vds/2$, the source barrier is narrow. This makes the electrons current less than the holes current. For Vgs greater than $Vds/2$, the source barrier becomes narrower and the drain barrier becomes wider. As a consequence, the electron current exceeds the hole current, and the drain current increases exponentially. At $Vgs = Vds/2$, the drain current reaches a minimum.

4. Novel Transistor Structures

In the simple CNTFET structure depicted in Fig. 1, for low Vgs, exponential increasing of the drain current begins at low drain voltages (tens of 1 V). This limits using the transistor for most applications, both for digital and analog circuits. To overcome this problem, one must prevent the drain Schottky diode from entering on state, and consequently increase the saturation range in the output characteristics. With a wider saturation range, a larger supply voltage can be used. For analog applications, this results in higher output power, and for digital circuits, this means greater noise immunity. In this section, novel structures are proposed in order to increase the saturation range.

4.1. *Double dielectric*

For the transistor of Fig. 1, if an insulator with higher dielectric is used, the gate control on the channel increases and vice-versa. Keeping this in mind, the transistor

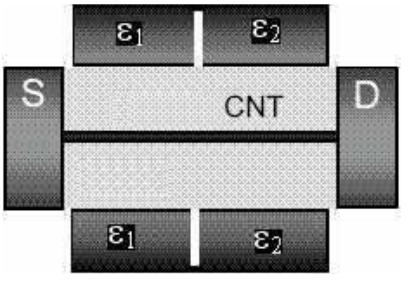

Fig. 5. Double dielectric CNTFET.

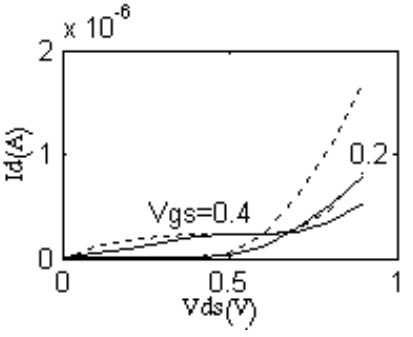

Fig. 6. Id–Vds for transistor proposed in Sec. 4.1 (solid) and conventional transistor (dot).

in Fig. 5 is proposed, in which the gate length is divided into two equal sections. The gate dielectric at the drain side is selected from a material with lower dielectric constant. Therefore, the gate control on the drain side of the channel is decreased. Figure 6 shows Id–Vds for this transistor. The dielectric constant at the drain side is assumed to be 5, whereas at the source side, the dielectric constant is assumed to be 25. Since the dielectric constant of the gate insulator near the drain is low, the gate potential has weaker influence on the channel near the drain. As Fig. 6 shows, this results in slightly increasing the saturation range of the transistor. From the fabrication point of view, however, deposition of two different insulators requires more fabrication processes.

4.2. *Double metal gate*

In this structure, as in the previous one, the gate length is divided into two parts, but with uniform dielectric, and different gate metals. The gate metal on the drain side is selected from a metal with lower work function. When the gate metal work function is lower, V_{MS} is decreased. Therefore, according to Eq. (2), the voltage boundary condition on the gate increases. This means that exponential increasing of the drain Schottky contact occurs at a higher drain voltage. Figure 7 shows Id–Vds for a transistor with gate metal of 0.2 V lower work function at the drain side.

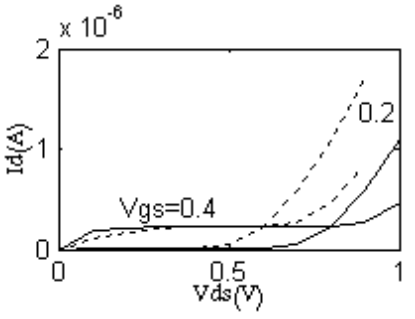

Fig. 7. *Id–Vds* for transistor proposed in Sec. 4.2 (solid) and conventional transistor (dot).

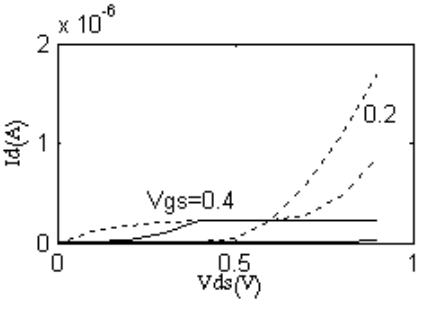

Fig. 8. *Id–Vds* for transistor proposed in Sec. 4.3 (solid) and conventional transistor (dot).

This figure shows that the current saturation portion in the output characteristics is almost 0.2 V wider than the transistor of Fig. 1. It must be noted that this method is limited to the available metal gates, i.e., any arbitrary work function is not available.

4.3. *Partially gate metallization*

In this structure, the gate metal on the drain side is not deposited. With this, gate affects the channel near the source, and has no effect on the channel near the drain. Therefore, it seems that the saturation region must be wider than previous structures. Figure 8 depicts the *Id–Vds* characteristics of the transistor. It is obvious from this figure that the saturation range of this transistor is much wider than two former structures. Moreover, this structure is easier to fabricate. In fact, no extra process is needed.

4.4. *Double dielectric with partially metallization*

The techniques proposed in subsections 4.2 and 4.3 can be merged, i.e., the drain side insulator be selected from a material with lower dielectric constant, without gate metal deposition. Figure 9 shows that this transistor has a wide saturation

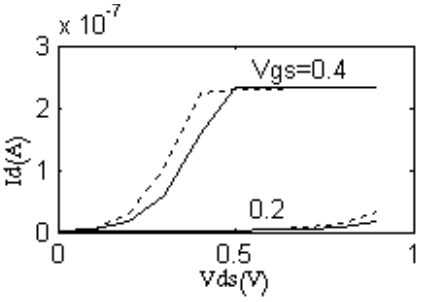

Fig. 9. Id–Vds for transistor proposed in Sec. 4.4 (solid) and conventional transistor (dot).

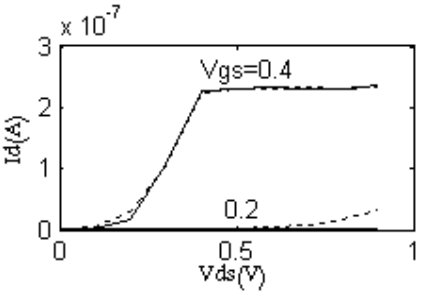

Fig. 10. Id–Vds for transistor proposed in Sec. 4.5 (solid) and conventional transistor (dot).

range. It must be noted that the fabrication process of this structure may be more complicated than the former transistors. In fact, fabrication complexity of this structure is the same as the transistor of subsection 4.2.

4.5. *Drain gate shorted*

If the drain metal is extended to cover a small portion of the channel, then the drain Schottky contact is always at zero bias, and therefore the holes current would be zero. This is very similar to the structure proposed in Ref. 15. Figure 10 shows the output characteristics of this transistor. It is assumed that the gate metal is deposited on the source half of the channel and the drain side metal connects to the drain metal. From the fabrication process point of view, this structure has no extra process.

In order to compare various structures, in Fig. 11 the Id–Vgs for various structures is depicted. This figure shows that methods of subsections 4.3–4.5 have better characteristics. From these three structures, we believe that because of larger output saturation range, the last one is superior. From the fabrication process point of view, it seems that the method of 4.3 is better since it requires no extra fabrication process.

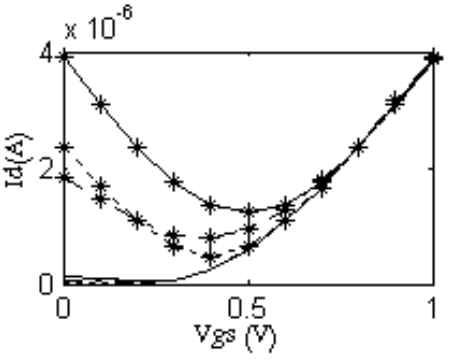

Fig. 11. *Id–Vgs* for conventional transistor (solid star) and transistors proposed in subsections 4.1 (dash-dot star), 4.2 (dot star), 4.3 (solid), 4.4 (dash-dot) and 4.5 (dot).

5. Conclusion

A CNTFET is simulated based on Schrödinger–Poisson formalism. This evaluation showed that the saturation range in the output characteristics is small. Five different structures are proposed to increase this range. These structures are evaluated and it is shown that proposed transistors have wider saturation range in the output characteristics. This makes them more suitable for both analog and digital applications. Increasing the saturation range in the output characteristics in three structures is at the expense of more fabrication processes.

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