An Offset Cancellation Technique for Comparators Using Body-Voltage Trimming

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***Abstract*— In this paper an offset cancellation technique based on body voltage trimming is presented to be used in the comparators employed in Flash or Successive-Approximation analog-to-digital converters. The proposed offset cancellation is achieved by body voltage adjustment using low-power simple analog control feedback circuit without any additional capacitive loading at the comparator output. The accuracy of the proposed technique is higher than its digital calibration counterparts due to its analog nature. The technique is employed in the design of a 6-bit 1-GSps Flash ADC in 0.18µm CMOS technology. Simulation results show that using the proposed technique the standard deviation of the comparator offset is significantly reduced from 28mV to 750µV operating at 1-GHz with only 25µW power in offset cancellation. The cancellation scheme generally improves the ENOB by approximately 0.5 bit after cancellation.**

I. INTRODUCTION

A voltage comparator is a principal building block in analog-to-digital converters (ADCs) with significant impact on the resolution and/or speed of the ADC. The ADCs often require the comparators to be low-power, low-offset, high speed with small area. While high speed and low power operation are benefited from technology scaling, the reduction of feature size leads to a larger mismatch of transistors. Therefore, many offset cancellation or calibration techniques have already been presented in order to improve the accuracy of the comparators and consequently the performance of the ADC.

Most common offset cancellation techniques are based on using pre-amplifiers with input/output offset storage (IOS/OOS) techniques [1]. However, often a high-gain, wide-bandwidth and thus power-hungry preamplifier is needed. In [2], a digital calibration technique was proposed, which calibrates the comparator offset through unbalancing the output loading of the comparator using arrays of MOS capacitors at each output. The number of MOS capacitors increases proportional to the increase in resolution, thus affecting the speed of the comparator and calibration accuracy. Another calibration technique is proposed in [3] in which a pair of calibrating transistors is shunt with the comparator input transistors. A resistance ladder generates the voltages which are applied to the gate of the shunt transistors using multiplexers. Although, this technique can achieve large calibration range but the accuracy of the reference voltage has to be better than the calibration resolution. In [4] an offset calibration is presented based on unbalancing the output loads using a single MOSCAP at each output. Despite the fact that using single MOSCAPs at the comparator output has less effect on the speed, in the worst mismatch condition, several clock cycles are required for the comparator to significantly reduce the offset as far as in each calibration clock, one reference voltage from the thermometer reference ladder has to be applied until the essential control voltage is detected. Finally, in [5] a digitally controlled bulk voltage trimming calibration is proposed. A calibration DAC is used to generate voltages above power supply in order to be applied to the body of one of the input transistors. This will increase the threshold voltage, decreasing its current. Calibration cycle continues until both input currents equalize. However, generating voltages above power supply will decrease the reliability of the operation of transistors in deep submicron technologies, while making use of resistor DAC will lead to static power consumption and extra offset. More importantly, in digital calibration techniques the accuracy is limited by the accuracy of the calibration DAC.

In this paper, a new high-resolution offset cancellation technique based on body-voltage trimming is proposed with no need to accurate reference voltages or additional capacitor array at the output. The idea is based on trimming the threshold voltages of the devices by changing the body voltage using a simple analog feedback circuit. The proposed technique is applied in the design of a 6-bit, 1-GSps Flash ADC. The calibration scheme significantly suppresses the effect of comparator offset with low power operation.

The rest of the paper is organized as follows. The proposed calibration scheme is explained in section II. Design considerations are addressed in Section III. Section IV presents the simulation results concluded by Section V.

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II. Offset Cancellation Scheme

The block diagram of the proposed cancellation scheme is illustrated in Fig. 1, which consists of a PMOS-input comparator; offset and polarity detector, two multiplexers (MUX) and the control feedback network. The comparator consists of a preamplifier, following a dynamic latch, as shown in Fig. 2. The main concept of the proposed technique is to cancel the offset of the preamplifier through adjusting the body voltages of the input transistors. Due to the fact that the preamplifier offset has prominent effect on the total equivalent input-referred offset voltage, cancelling it will lead to significant reduction in the total input-referred offset, as far as the effect of the latch offset is greatly reduced by the gain of the preamplifier.

Offset cancellation is performed in foreground during which the normal operation of the ADC is interrupted. During the offset-cancellation cycle, the common-mode voltage V_{cm} is applied to both input transistors of the preamplifier. Due to the mismatch, the outputs of the preamplifier differ. The offset and its polarity are detected through the value of the outputs. Then the feedback network generates the proportional control voltage, which is applied to the body of that input device which provides less current (due to the mismatch), through Multiplexers. Since the threshold voltage, V_{th}, changes with the source-body voltage, V_{SB}, and the transistor current changes with V_{th}, offset calibration is performed by modifying the body voltages of the input transistors, M1 & M2. The threshold voltage of a PMOS $|V_{th,p}|$ can be expressed as follows:

$$|V_{th,p}| = |V_{th0,p}| + |\gamma|\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right) \quad (1)$$

where $|V_{th0,p}|$ is the threshold voltage at V_{SB}=0, $_f$ is the Fermi voltage and γ is the body-effect coefficient. Our simulations show that V_{th} can vary about 350mV by changing V_{SB} which can be used to compensate the effect of mismatch.

A PMOS-input preamplifier is used, which makes it possible for the input transistors to be placed in different n-wells for adjusting their body voltages. To ensure the reverse-biasing condition of the source-body junction, the body of one of the inputs (with more current) is fixed to VDD while the body of the other input device (with less current) is decreased within the allowed possible rang, (i.e. V_{SB}<0.4V) to decrease its threshold voltage and consequently increasing its current. During calibration scheme, since the source terminal of the input transistors changes accordingly with the variation of body voltage of the input transistors, simulation results reveal that for different input common-modes, V_{SB} remains within allowed range. Besides, special attention is required in sizing the devices in the calibration feedback circuit to avoid forward-biasing of the source-body junction. This technique can be also used in comparators with NMOS input pair with deep n-well (or p-well) fabrication processes.

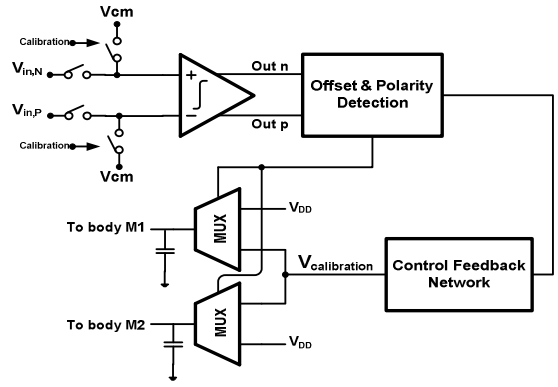

Figure 1. Block diagram of the proposed calibration scheme

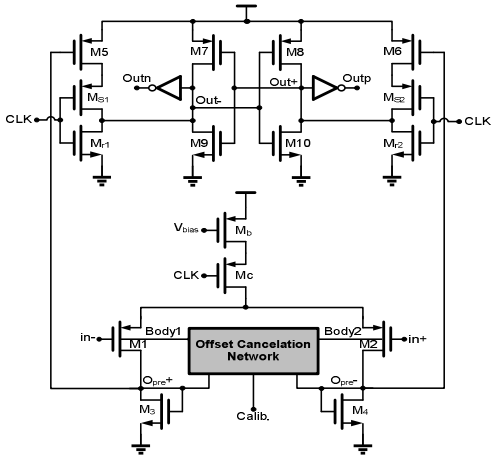

Figure 2. The schematic of the comparator: Preamplifier and dynamic latch

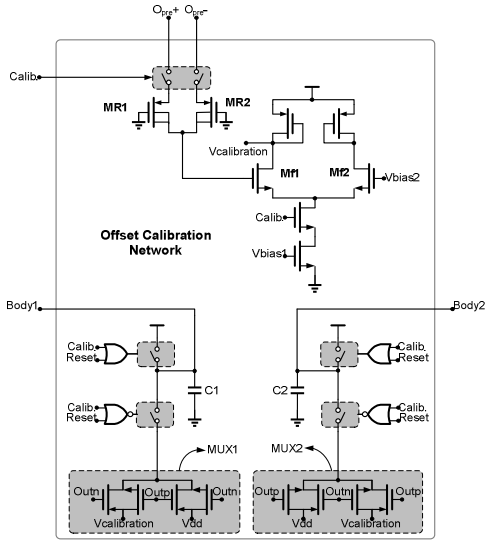

Figure 3. The schematic of the Calibration Feedback network

III. Circuit Implementation

A. Comparator

Both the preamplifier and the latch have the advantages of low power and high speed operation and are widely used in

flash ADCs. The operation of the comparator is as follows. When the clock is at V_{dd}, the outputs of the latch are reset to ground (by M_{r1} –M_{r2}), also transistors M_{s1}-M_{s2} disconnect the latch from the preamplifier in order to avoid kickback noise and hysteresis. Besides, the preamplifier tail transistor (M_c) is cut-off to prevent any static current from the supply to ground. When the clock becomes low, M_c is turned on and the input transistors force the current into diode-connected loads (M_3-M_4). The gain of the preamplifier has been chosen equal to 3, in order to reduce the input referred latch offset voltage below the acceptable value of $1V_{LSB}$. Based on the output voltage of the preamplifier, regeneration begins in the latch and the outputs are set to Vdd and ground. Any mismatch between the input transistors contribute the most in the preamplifier total offset as far as they control the currents to the loads. The following equations indicate how M1 and M2 affect the offset voltage of the preamplifier.

$$\Delta V_{os-eq,due\ to\ M1-M2} = \Delta V_{th1,2} + \frac{1}{2}\frac{\Delta s_{1,2}}{s_{12}}(V_{gs1,2} - V_{th1,2}) \quad (2).$$

where $\Delta V_{th1,2}$ is the threshold voltage offset of the differential pair M1-M2, $\Delta s_{1,2}$ is the physical dimension mismatch and $(V_{gs1} - V_{th1,2})$ is the effective voltage of the input pair. The first term is a static offset but the second term is a signal-dependent dynamic offset. Substituting $V_{gs1,2}$ in terms of input common-mode voltage, V_{cm} , it can be shown that the voltage offset due to the mismatch between the current factors of the input devices (i.e. $\beta=\mu.C_{ox}.W/L$) can be calculated from

$$\Delta V_{os-\Delta\beta} = \frac{1}{2}\frac{\Delta W_{1,2}}{W_{12}}\left[\frac{W_{ctail}(V_{dd}-V_{th})}{2W_{1,2}}\left(\sqrt{1+\frac{4W_{1,2}(V_{cm}-V_{th})}{W_{clk}(V_{dd}-V_{th})}}-1\right)\right] \quad (3).$$

Thus, V_{cm}-V_{th} affects $\Delta V_{os\text{-}eq}$ in approximately square root dependence. In order to reduce this dependency, a simple and effective way is to use a saturated MOS transistor (M_b in Fig. 2) as a cascode device above the switch transistor (M_c) [6]. Since M_b is biased in saturation, its current slightly varies with the variation of its drain-source voltage; therefore, it keeps the effective voltage of the input devices nearly constant when V_{cm} is changed; in other words,

$$\left(V_{gs1,2} - V_{th1,2}\right)^2 = \frac{1}{2}\frac{\beta_{p,mb}}{\beta_{p1,2}}(V_{bias} - V_{th})^2(1 + \lambda(V_{cm} - V_{gs1,2} - V_{ds,mc}) \quad (4).$$

where λ is the channel-length modulation coefficient and V_{bias} is the bias voltage of M_{btail}. Solving (4) to find V_{gs1}, it will be found that the dependence of the effective voltage of the input devices to V_{cm} variation is significantly reduced.

B. Offset Cancellation Network

Fig. 3 demonstrates the calibration feedback network. It is controlled by a control signal called "Calib" (shown in Fig. 3). Its pulse width is equal to half of the ADC clock period and it will remain at "0" until the end of calibration. Before the calibration starts, the ADC clock is high and the comparator is reset. When the calibration starts (calib='1'), the input transistors are disconnected from the input signal and tied to V_{cm}. Ideally if no offset exists, both preamplifier outputs have equal voltages but assuming any mismatch between devices, one branch of the differential amplifier senses more current, resulting in higher output voltage. Consequently this difference voltage between the preamplifier's outputs is sensed by the latch. During this phase (Calib="1"), offset and its polarity is detected and the input transistor, whose body should be modified is determined. The bodies of both input transistors are tied to V_{dd} during reset and offset detection phase. Then when calib="0", calibration network connects to the preamplifier outputs and the bodies are connected to the outputs of the multiplexers. One of them remains at V_{dd} and the other one is connected to the calibration voltage which is generated by calibration feedback circuit (shown in Fig. 3) and will be saved in the corresponding capacitor (i.e. C_1 or C_2). The value of these holding capacitors has been selected so that they would be able to hold the calibration voltage till the next calibration phase. For high-speed ADCs, the leakage voltage due to the leakage current is ignorable (simulation results confirm this matter). Based on the leakage current, the size of the capacitor and the frequency at which the calibration process must be repeated are chosen based on the sampling frequency of the ADC.

The operation of the calibration feedback circuit is as follows: during calibration (calib="0"), the preamplifier outputs are connected to PMOS Transistors M_{R1}-M_{R2} (Fig. 3) which are realized as integrated high-value resistors (IHVR). The difference between the outputs is averaged through IHVRs and applied to the gate of a differential pair. To implement high-value resistors, the configuration presented in [7] is employed in which transistors are biased in sub-threshold regime and the bulk of the PMOS transistors (which are in isolated n-wells) are connected to their drains. Thus, by increasing V_{SD}, the threshold voltage of these devices is modified, and consequently, the drain current will increase. This dependence of current on drain voltage results in a large and finite output conductance that can be expressed based on EKV model as [7]:

$$G_{SD} = \left(\frac{I_{SD}}{nU_T}\right)\left[\frac{n}{1-\exp\left(-\frac{V_{SD}}{U_t}\right)} - 1\right] \quad (5).$$

In our design, based on simulation results, the value of R_{SD} was about 100MΩ.

The operation of the negative feedback control of output preamplifiers can be explained as follows: ideally when there is no offset, both outputs are equal to 768mV (in our design). In the presence of the offset, for instance, when the averaged voltage of the outputs (which is applied to the gate of M_{f1}) increases, the

current of M_{f1} increases, (since the bias voltage applied to another transistor (M_{f2}) is fixed), leading to a decrease in the control voltage, which decreases the body of an input (which had been selected when Calib='1'), increasing its current and therefore increasing the averaged voltage. Similar to common-mode feedback networks, the feedback continues until the averaged voltage reaches the value of the fixed bias voltage and $V_{calibration}$ settles to a fixed value and is stored on the body capacitors. The size of the transistors and the tail current of the feedback circuit has been designed in such a way that $V_{calibration}$ changes within the specified range (to avoid forward biasing of the source-body junctions) for the worst-case mismatch condition.

IV. SIMULATION RESULTS

The proposed offset cancellation scheme is employed in a 1.8-V, 6-bit, 1-GSps full-Flash ADC using 0.18-µm CMOS technology. All devices are typical transistors with nominal threshold voltages. In order to verify the operation of the calibration scheme, intentionally a mismatch is applied to the inputs of preamplifier. Fig. 4 shows the preamplifier outputs under calibration. Before calibration, assuming worst-case mismatch condition, the value of the output-referred offset of the preamplifier is 183mV which has been reduced to 3mV after calibration. Body Voltages are also illustrated in Fig. 4. It is obvious that while one of the bodies remains unchanged the other one is reduced to compensate the effect of mismatch. V_{SB} is about 0.3V which is beyond the threshold of the source-body conduction. In order to measure the offset, Monte Carlo simulations have been performed for 300 runs. 1-sigma offset value before calibration is 28mV, while it has been remarkably reduced to 750µV after calibration. Simulation results of 25 results before and after calibration are illustrated in Fig. 5. Since the calibration network is disabled during normal operation of ADC, the total calibration power is 25µW which is come from calibration feedback circuit.

V. CONCLUSION

A new analog-based offset cancellation technique based on body-voltage trimming has been presented. The simple architecture of the offset cancellation network avoids any design complexity, capacitive loading or power-consuming reference ladder. Monte Carlo simulations of the comparator shows that the offset can be suppressed up to 98% using the proposed technique.

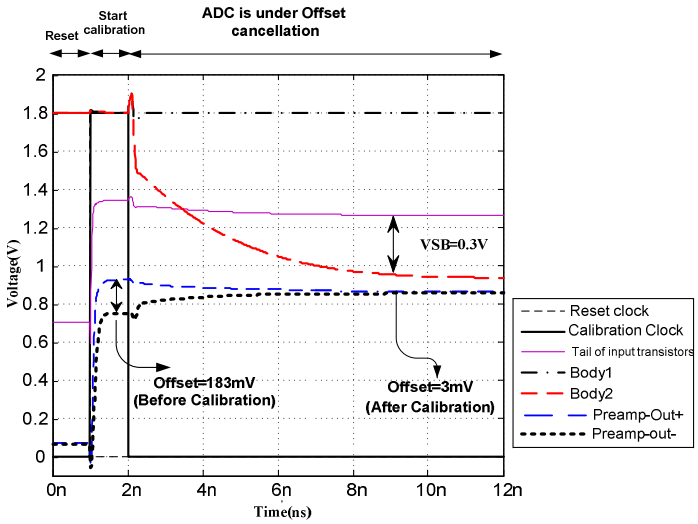

Figure 4. The offset cancellation scheme on preamplifier outputs

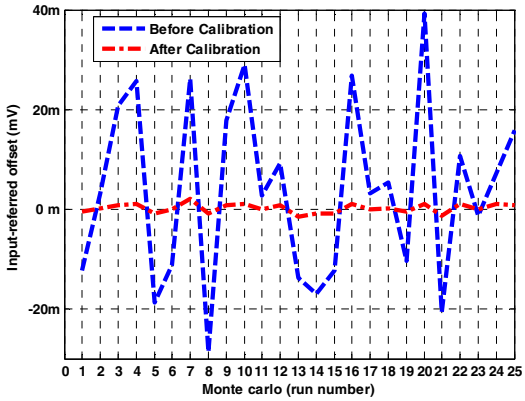

Figure 5. Monte Carlo simulation of offset in Comparator (Before and After Calibration)

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