Design and Tuning of a Modified Power-Based PLL for Single-Phase Grid-Connected Power Conditioning Systems

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Abstract—One of the most important aspects for the proper operation of the single-phase grid-tied power-conditioning systems is the synchronization with the utility grid. Among various synchronization techniques, phase locked loop (PLL)-based algorithms have found a lot of interest for the advantages they present. Typically, the single-phase PLLs use a sinusoidal multiplier as the phase detector (PD). These PLLs are generally referred to as the power-based PLL (pPLL). In this paper, the drawbacks associated with the pPLL technique (i.e., the sensitivity to the grid voltage variations, and the double-frequency oscillations that appear in the estimated phase/frequency) are discussed in detail, and some of the previously reported solutions are examined. Then, to overcome these drawbacks, a simple and effective technique, called the double-frequency and amplitude compensation (DFAC) method is proposed. The effectiveness of the proposed method is evaluated through a detailed mathematical analysis. A systematic design method to fine-tune the PLL parameters is then suggested, which guarantees a fast transient response, a high disturbance rejection capability, and a robust performance. Finally, the simulation and experimental results are presented, which highlight the effectiveness of the proposed PLL.

Index Terms—Frequency estimation, phase estimation, phase-locked loop (PLL), power-based PLL (pPLL), single phase grid-connected converters, synchronization.

I. INTRODUCTION

THE phase-angle and frequency of the utility grid are vital information for most single-phase grid-tied power-conditioning systems, such as active power filters [1], dynamic voltage restorers [2], [3], flexible ac transmission systems (FACTS) [4]–[6], uninterruptible power supplies (UPS) [7], and distributed power generation and storage systems [8].

To estimate the frequency and phase-angle of the single-phase signals various methods have been proposed in the literature [4]–[25]. Among these techniques, the phase locked loop (PLL)-based algorithms are the most widely accepted ones, due to their simplicity, robustness, and effectiveness [4]–[20]. Focusing on grid-connected power converter applications, a PLL is a closed-loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with the grid voltage fundamental component. In spite of their differences, all PLL techniques are composed of three basic parts, namely: 1) phase detector (PD), 2) loop filter (LF), and 3) voltage-controlled oscillator, as illustrated in Fig. 1.

The main difference among different PLLs usually lies in how the PD block is implemented. Typically, the single-phase PLLs use a sinusoidal multiplier as the PD. These PLLs are generally referred to as the power-based PLL (pPLL). In the following section, the drawbacks associated with the pPLL technique (i.e., the sensitivity to the grid voltage variations, and the double-frequency oscillations that appear in the estimated phase/frequency) are discussed in detail, and some of the previously reported solutions are examined. Then, to overcome these drawbacks, a simple and effective technique, called the double-frequency and amplitude compensation (DFAC) method is proposed. Through a detailed mathematical analysis it is shown that the proposed DFAC method successfully compensates for the undesired double-frequency oscillations, as well as for the input voltage amplitude variations, while keeping a fast dynamic response and robust performance for the PLL. It is worth remarking that, for three-phase PLLs, tackling the generation of the low-order oscillations in the estimated phase/frequency has been well addressed [26], [27].

An accurate tuning of the PLL parameters requires considering several factors such as the stability margin, the disturbance rejection ability, and the transient response to the phase-jump and frequency variation. Some suggestions to design the PLL...
parameters have been presented in the literature [7], [10]–[13], [28], [29]. In this paper, a systematic design procedure to fine-tune the PLL parameters is proposed. The suggested approach guarantees a fast transient response, a high disturbance rejection capability, and a robust performance.

This paper is organized as follows. Section II provides a brief review of the pPLL topology. The main drawbacks of the pPLL, and previously reported solutions are also discussed in this section. The proposed PD is presented in Section III. The small-signal modeling of the proposed PLL, here, referred to as DFAC–pPLL, and the stability analysis are addressed in Section IV. The proposed systematic design method is discussed in Section V. The simulation and experimental results are presented in Section VI. Finally, Section VII concludes this paper.

II. BACKGROUND

The basic scheme of the single-phase pPLL is depicted in Fig. 2 [7]. Throughout this section and the following section, for the sake of simplicity, the input voltage \(v_i\) is assumed to be a pure sine wave, i.e., \(v_i = V \cos \theta\), where \(V\) and \(\theta = \omega t + \phi\) are the input voltage amplitude and angle, respectively. \(\omega_{ff}\) is the nominal value of the frequency \(\omega\), and \(\phi\) is the phase-angle. The superscript "\(\hat{\cdot}\)" denotes the estimated quantities.

The pPLL, as seen, uses a sinusoidal multiplier followed by a low-pass filter (LPF) for the PD. Note that the PD block tries to emulate an active power calculation unit. If the PD block output signal (i.e., \(\hat{p}\)) is zero, then the input voltage \(v_i\) and the fictitious current \(i_s\) will be in quadrature relative to each other [7]. In this case, the estimated value of the voltage angle \(\hat{\theta}\) is equal to the real value \(\theta\).

Based on Fig. 2, the fictitious power \(p\) can be expressed as

\[
p = v_i i_s = V \cos \theta \sin \hat{\theta}.
\]

Applying the product-to-sum trigonometric identity, yields

\[
p = V \left( \frac{1}{2} \sin(\hat{\theta} - \theta) + \frac{1}{2} \sin(\hat{\theta} + \theta) \right).
\]

Supposing a small difference between \(\theta\) and \(\hat{\theta}\), (2) can be divided into two parts: a small dc term that has the information on the phase difference, and a high-amplitude double-frequency disturbance term that must be filtered out to keep up the phase jittering within an acceptable range [30].

To cancel out the undesired double-frequency component from the fictitious power \(p\), one can use either a first- (or second-) order LPF with a low cutoff frequency or a high-order LPF with a higher cutoff frequency. In addition to stability problems, using a high-order LPF imposes a high computational load on the control system [31]. On the other hand, using a low-order LPF with a low cutoff frequency, significantly degrades the transient performance of the PLL. Another approach is to use a notch filter tuned at twice the input voltage fundamental frequency. Because of the grid frequency variations, the notch filter should be adaptive, which increases the system cost and complexity.

Some improvements to the pPLL have been suggested in [16], [17]. In these techniques, referred to as orthogonal signal generation (OSG)-based techniques, the fundamental component of the input voltage is shifted by 90° to generate a fictitious phase signal, thus making it possible to represent the single-phase system as a pseudo two-phase (\(\alpha\beta\)) system. Applying the well-known park (\(\alpha\beta \rightarrow dq\)) transformation to the two phase (\(\alpha\beta\)) system, yields the phase error information without generating the undesired double-frequency component. It should be noticed that the main difference among different OSG-based techniques lies in how the fictitious orthogonal signal is generated. In spite of their differences, all OSG-based techniques suffer from some common drawbacks, such as high sensitivity to the grid frequency variations, and relatively high complexity [18].

The most recent improvement to the pPLL is that proposed by Thacker et al. [12]. In their method, a unity value for the input voltage amplitude is assumed that is realized by a peak voltage detection (PVD) scheme at the input of the PLL. Under this assumption, and in phase/frequency-locked conditions (i.e., \(\theta \cong \hat{\theta}\)), the unwanted double-frequency component is filtered out by subtracting a product term (i.e., \(\sin \hat{\theta} \cos \hat{\theta}\)) from the fictitious power \(p\), as shown in Fig. 3. Although this PLL exhibits some improvements over the pPLL technique, it suffers from a major drawback; regardless of the cost and the complexity imposed by the PVD, the exact and fast estimation of the input voltage amplitude may not always be possible. In this case, the PLL performance is significantly degraded.

The dependence of the PLL stability and dynamic performance on the input voltage amplitude is other drawback of the pPLL. It is shown that the voltage amplitude \(V\) contributes as a gain in the forward path of the PLL small-signal model [32]. Thus, under the voltage sag condition, which is commonly associated with the phase-angle jump [33], [34], the PLL transient
response is significantly degraded. In this situation, the PLL may also become unstable, if the phase margin is too low [35]. These drawbacks can be eliminated in part by compensating the PLL input signal with an amplitude estimation scheme, as reported in [4], [5], [12], and [14], but at the expense of higher complexity and cost.

To filter out the undesired steady-state double-frequency oscillations without degrading the stability and the transient performance of the PLL and, at the same time, to compensate for the input voltage amplitude variations, an effective method, called the DFAC method, is presented in the next section.

III. PROPOSED DFAC METHOD

Fig. 4 displays the basic scheme of the proposed phase detection unit, where \( v_d \) and \( v_q \) are obtained as expressed in the following equation:

\[
\begin{bmatrix}
  v_d(t) \\
  v_q(t)
\end{bmatrix} =
\begin{bmatrix}
  \cos \hat{\theta} & \sin \hat{\theta} \\
  -\sin \hat{\theta} & \cos \hat{\theta}
\end{bmatrix}
\begin{bmatrix}
  2v_r(t) \\
  0
\end{bmatrix}
\] (3)

Substituting \( v_i = V \cos \theta \) into (3), gives

\[
\begin{align*}
  v_d(t) &= V \cos(\theta - \hat{\theta}) + V \cos(\theta + \hat{\theta}) \\
  v_q(t) &= V \sin(\theta - \hat{\theta}) - V \sin(\theta + \hat{\theta})
\end{align*}
\] (4)

From (3) and (4), the mathematical expressions for \( \hat{v}_d \) and \( \hat{v}_q \) are derived.

To analyze the performance of the proposed DFAC method, the mathematical expressions for \( \hat{v}_d \) and \( \hat{v}_q \) are derived.

From Fig. 5, in the Laplace domain, we have

\[
\begin{align*}
  \hat{v}_d(s) &= \frac{\omega_p}{s + \omega_p} \times \ell \left[ v_d(t) - \hat{v}_d(t) \cos(2\hat{\theta}) + \hat{v}_q(t) \sin(2\hat{\theta}) \right] \\
  \hat{v}_q(s) &= \frac{\omega_p}{s + \omega_p} \times \ell \left[ v_q(t) + \hat{v}_d(t) \sin(2\hat{\theta}) + \hat{v}_q(t) \cos(2\hat{\theta}) \right]
\end{align*}
\] (11) (12)

where, \( \ell \) denotes the Laplace operator.

Multiplying both sides of (11) and (12) by \( (s + \omega_p) \), and rearranging them, gives

\[
\begin{align*}
  s\hat{v}_d(s) &= \omega_p \times \ell \left[ v_d(t) - (\cos(2\hat{\theta}) + 1)\hat{v}_d(t) + \sin(2\hat{\theta})\hat{v}_q(t) \right] \\
  s\hat{v}_q(s) &= \omega_p \times \ell \left[ v_q(t) + \sin(2\hat{\theta})\hat{v}_d(t) + (\cos(2\hat{\theta}) - 1)\hat{v}_q(t) \right]
\end{align*}
\] (13) (14)

Transforming (13) and (14) into the time domain, and rearranging the results into the matrix form, yields

\[
\begin{bmatrix}
  \hat{v}_d(t) \\
  \hat{v}_q(t)
\end{bmatrix} = \begin{bmatrix}
  -\cos(2\hat{\theta}) - 1 & \sin(2\hat{\theta}) \\
  \sin(2\hat{\theta}) & \cos(2\hat{\theta}) - 1
\end{bmatrix}
\begin{bmatrix}
  \hat{v}_d(t) \\
  \hat{v}_q(t)
\end{bmatrix}
\begin{bmatrix}
  \omega_p & 0 \\
  0 & \omega_p
\end{bmatrix}
\begin{bmatrix}
  v_d(t) \\
  v_q(t)
\end{bmatrix}
\] (15)
Substituting (8) and (9) into (15), and making some rearrangements, gives
\[
\begin{bmatrix}
\dot{\bar{v}}_d(t) \\
\dot{\bar{v}}_q(t)
\end{bmatrix}
= \omega_p \begin{bmatrix}
-\cos(2\hat{\theta}) - 1 & \sin(2\hat{\theta}) \\
\sin(2\hat{\theta}) & \cos(2\hat{\theta}) - 1
\end{bmatrix}
\times \begin{bmatrix}
\bar{v}_d(t) \\
\bar{v}_q(t)
\end{bmatrix}
+ \begin{bmatrix}
V \cos(\theta_e) \\
V \sin(\theta_e)
\end{bmatrix}
\] (16)

Based on (16), the state-space description of the DFAC block can be derived, as follows:
\[
\begin{aligned}
\dot{x}(t) &= A(t)x(t) + B(t)u(t) \\
y(t) &= C(t)x(t)
\end{aligned}
\] (17)

where
\[
\begin{aligned}
x(t) &= \begin{bmatrix}
\bar{v}_d(t) \\
\bar{v}_q(t)
\end{bmatrix} \\
u(t) &= \begin{bmatrix}
V \cos(\theta_e) \\
V \sin(\theta_e)
\end{bmatrix} \\
A(t) &= -B(t) = \omega_p \begin{bmatrix}
-\cos(2\hat{\theta}) - 1 & \sin(2\hat{\theta}) \\
\sin(2\hat{\theta}) & \cos(2\hat{\theta}) - 1
\end{bmatrix} \\
C(t) &= I.
\end{aligned}
\]

The state-space equation (17), describes a linear time-variant (LTV) system with two inputs and two outputs, which its solution takes a lot of time and space, and needs enormous patience. To simplify the solution, it is assumed that \( \omega \approx \hat{\omega} \). Hereby, the angle difference \( \theta_e \) becomes approximately equal to the phase difference \( \phi - \hat{\phi} \). Under this condition, and considering the inputs [i.e., \( V \cos(\theta_e) \), and \( V \sin(\theta_e) \)] as step functions, the expressions for \( \bar{v}_d(t) \) and \( \bar{v}_q(t) \) can be derived as
\[
\begin{aligned}
\bar{v}_d(t) &= A_d + \{ B_d \cos(\omega t) \cos(\omega f t) + C_d \sin(\omega t) \sin(\omega f t) \\
&+ D_d \sin(\omega t) \cos(\omega f t) \} e^{\omega_f t} \\
\bar{v}_q(t) &= A_q + \{ B_q \cos(\omega t) \cos(\omega f t) + C_q \sin(\omega t) \sin(\omega f t) \\
&+ D_q \sin(\omega t) \cos(\omega f t) \} e^{\omega_f t}
\end{aligned}
\]
(18)

where
\[
\omega_f = \sqrt{\omega^2 - \omega_p^2} \\
A_d = -B_d = D_q = V \cos(\theta_e) \\
C_d = E_q = -V \omega \cos(\theta_e) + \omega_p \sin(\phi + \hat{\phi}) / \omega_f \\
D_d = -A_q = B_q = -V \sin(\theta_e), \text{ and} \\
E_d = -C_q = V \sin(\phi + \hat{\phi}) + \omega \sin(\theta_e) / \omega_f.
\]

From (18) and (19), it can be seen that the fluctuating terms decay to zero with a time constant of \( 1 / \omega_p \), and \( \bar{v}_d(t) \) and \( \bar{v}_q(t) \) converge to \( V \cos(\theta_e) \) and \( V \sin(\theta_e) \), respectively. These results are clearly illustrated in Fig. 6 for three different values of the cutoff frequency \( \omega_p \), i.e., \( \omega_p = 10 \text{ Hz} \) (solid line), \( \omega_p = 30 \text{ Hz} \) (dashed line), and \( \omega_p = 60 \text{ Hz} \) (dotted line), and for \( \phi = \hat{\phi} = \pi / 6 \text{ rad}, \omega = \hat{\omega} = 120 \text{ rad/s}, \text{ and } V = 100 \text{ V} \). As expected, using the proposed DFAC method, the perfect cancellation of the double-frequency components is achieved.

On the other hand, the negative effect of the input voltage amplitude variations on the PLL stability and transient performance is damped by calculating the input voltage amplitude, as follows, and then dividing \( \bar{v}_q \) by the estimated amplitude \( \hat{V} \) (see Fig. 5)
\[
\hat{V} = \sqrt{\bar{v}_d^2 + \bar{v}_q^2}.
\]
(20)

To avoid instability problems, the estimated amplitude \( \hat{V} \) is limited by a saturation block. The upper and lower limits should be set according to the allowable range of the input voltage amplitude variations. In this paper, the lower and upper limits are set to 0.2 and 1.5 pu, respectively.

**IV. SMALL-SIGNAL MODEL AND STABILITY ANALYSIS**

Fig. 7 illustrates the basic scheme of the proposed DFAC-PLL. The input voltage \( v_i \) is considered to be harmonic polluted (as a result of the proliferation of nonlinear loads in power systems), and is represented by
\[
v_i(t) = V \cos(\omega t + \phi) + f(3\omega, 5\omega, 7\omega, \ldots).
\]
(21)

Applying the transformation matrix (3) to (21), gives
\[
v_q(t) = V \sin(\theta - \hat{\theta}) - V \sin(\theta + \hat{\theta}) + g(2\omega, 4\omega, 6\omega, \ldots).
\]
(22)
The aim of this section is to design the PLL parameters (i.e., $k_p$, $k_i$, and $\omega_p$) such that the system stability is guaranteed, and at the same time, a proper transient performance, and a high disturbance rejection capability is achieved. Some suggestions to improve the ride-through capability of the PLL is also presented in this section.

A. Stability

The main focus in this section is to establish a design criterion, based on the extended symmetrical optimum method [36], so that the maximum possible stability margin for the PLL is achieved.

Considering $k_i/k_p = \omega_c$, the open-loop transfer function of the DFAC-pPLL can be derived as

$$G_{ol}(s) = \frac{k_p \omega_p (s + \omega_c)}{s^2 + \omega_c^2}.$$  \hfill (28)

From (28), the phase margin (PM) can be obtained as

$$\text{PM} = \tan^{-1}(\omega_c/\omega_p) - \tan^{-1}(\omega_c/\omega_p)$$

where, $\omega_c$ is the crossover frequency, and is given by

$$\omega_c = k_p \cos(\phi_p)/\sin(\phi_p).$$  \hfill (30)

Differentiating (29) with respect to the crossover frequency $\omega_c$, i.e., $\partial(\text{PM})/\partial(\omega_c)$, and equating the result to zero, yields

$$\omega_c = \sqrt{\omega_p^2 - \omega_c^2}.$$  \hfill (31)

Substituting (31) into (30), gives

$$\omega_c = \frac{k_p}{\omega_c}$$

which means that the PM is maximized when the proportional gain $k_p$ is equal to the crossover frequency $\omega_c$. From (31), and assuming $\omega_p = k^2 \omega_c$, where $k$ is a constant value, we get

$$\begin{cases} \omega_c = \omega_c/k \\ \omega_p = k \omega_c. \end{cases}$$  \hfill (33)

Substituting (33) into (29), PM can be rewritten as

$$\text{PM} = \tan^{-1} \left( \frac{k^2 - 1}{2k} \right).$$

Fig. 9 displays the phase margin versus factor $k$. As shown, the higher the factor $k$ is, the higher is the phase margin. Recommended value for a proper phase margin is [37]

$$30^\circ < \text{PM} < 60^\circ.$$  \hfill (35)

To meet this, we need

$$1.732 < k < 3.732.$$  \hfill (36)

B. Transient Performance

The main emphasis in this section is to improve the ride-through capability of the PLL through minimizing its settling time for both phase and frequency jumps.
Substituting (32) and (33) into (28), the open-loop transfer function \( G_{ol} \) can be rewritten as

\[
G_{ol}(s) = \frac{k\omega_n^2 s + \omega_n^3}{s^2(s + k\omega_c)}. \tag{37}
\]

The transfer function (37) has two poles at the origin (i.e., type-2 system). Thus, the zero steady-state error is guaranteed for both phase jump (step input) and frequency jump (ramp input) [28].

From Fig. 8, the error transfer function, i.e., \( \theta_e(s)/\theta(s) \), can be derived as

\[
G_e(s) = \frac{\theta_e(s)}{\theta(s)} = \frac{1}{1 + G_{ol}(s)}. \tag{38}
\]

Substituting (37) into (38), yields

\[
G_e(s) = \frac{s^2(s + k\omega_c)}{(s + \omega_c)(s^2 + (k-1)\omega_c s + \omega_n^2)}. \tag{39}
\]

Considering \( \zeta = (k-1)/2 \), and \( \omega_c = \omega_n \), (39) can be rewritten as

\[
G_e(s) = \frac{s^2(s + (2\zeta + 1)\omega_n)}{(s + \omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)}. \tag{40}
\]

The inverse Laplace transform of \( \theta_e(s) = G_e(s)\theta(s) \), for step and ramp inputs, yield the time-domain tracking errors for phase \( \theta_e^\phi(t) \) and frequency \( \theta_e^\omega(t) \) jumps, respectively, given as shown (41) and (42) at the bottom of this page.

\[
\theta_e^\phi(t) = \begin{cases} 
\frac{\Delta \phi}{\zeta - 1}\left[ e^{-\omega_n t} - e^{-\zeta\omega_n t} \cos \left( \omega_n t \sqrt{1 - \zeta^2} \right) \right] & \zeta < 1 \\
\frac{\Delta \phi}{\zeta - 1}\left[ e^{-\omega_n t} (1 + \omega_n t - \omega_n^2 t^2) \right] & \zeta = 1 \\
\frac{\Delta \phi}{\zeta - 1}\left[ e^{-\omega_n t} - \frac{1}{2} e^{-(\zeta - \sqrt{\zeta^2 - 1})\omega_n t} - \frac{1}{2} e^{-(\zeta + \sqrt{\zeta^2 - 1})\omega_n t} \right] & \zeta > 1
\end{cases} \tag{41}
\]

\[
\theta_e^\omega(t) = \begin{cases} 
\frac{\Delta \omega}{1 - \zeta}\omega_n \left[ e^{-\omega_n t} + e^{-\zeta\omega_n t} \left\{ -\zeta \cos \left( \omega_n t \sqrt{1 - \zeta^2} \right) + \sqrt{1 - \zeta^2} \sin \left( \omega_n t \sqrt{1 - \zeta^2} \right) \right\} \right] & \zeta < 1 \\
\frac{\Delta \omega}{\omega_n} e^{-\omega_n t} (\omega_n t + \omega_n^2 t^2) & \zeta = 1 \\
\frac{\Delta \omega}{1 - \zeta}\omega_n \left[ e^{-\omega_n t} - \frac{\sqrt{\zeta^2 - 1}}{2} e^{-(\zeta - \sqrt{\zeta^2 - 1})\omega_n t} - \frac{\zeta - \sqrt{\zeta^2 - 1}}{2} e^{-(\zeta + \sqrt{\zeta^2 - 1})\omega_n t} \right] & \zeta > 1.
\end{cases} \tag{42}
\]
the PLL stability for the selected value of the damping factor $\zeta$. Substituting $\zeta = 0.7$ (which is corresponding to $k = 2.4$) into (34), yields

$$\text{PM}|_{k=2.4} = 44.76^\circ$$

which guarantees the PLL stability.

C. Disturbance Rejection

As mentioned earlier, the input voltage harmonics (i.e., the odd harmonics as 3rd, 5th, 7th, etc.) appear as disturbance inputs (i.e., the even harmonics as 2nd, 4th, 6th, etc.) to the PLL linearized model. Thus, it is necessary to provide a sufficient attenuation at the concerned frequencies.

From Fig. 8, the disturbance transfer function relating the estimated angle $\hat{\theta}$ to the disturbance input $D(s)$ can be derived as

$$G_D(s) = \frac{\hat{\theta}(s)}{D(s)} = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{(2\zeta + 1)\omega_n^2 s + \omega_n^3}{(s + \omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)}.$$  

Fig. 11 illustrates the Bode plot of the transfer function (44) for three different values of the natural frequency $\omega_n$, namely, $\omega_n = 5$ Hz (solid line), $\omega_n = 15$ Hz (dashed line), and $\omega_n = 30$ Hz (dotted line), and for $\zeta = 0.7$. As shown, the transfer function (44) exhibits a low-pass filtering behavior. The lower the natural frequency is, the higher is the attenuation at the disturbance frequencies, and hence, the better is the filtering property.

Providing a sufficient attenuation at twice the input voltage fundamental frequency (i.e., $2\omega$), guarantees the high disturbance rejection capability. Fig. 12 displays the PLL attenuation at $2\omega$ versus the natural frequency $\omega_n$. The proper attenuation (which depends on the application where the PLL is used) is selected to be $-20$ dB in this paper, yielding the natural frequency $\omega_n$ (and hence the crossover frequency $\omega_c$) equals to 24.71 Hz.

Considering $\omega_c = 24.71$ Hz (155.26 rd/s), and $k = 2.4$, the PLL parameters $k_p$, $k_i$, and $\omega_p$ can be obtained as

$$\begin{align*}
k_p &= \omega_c = 155.26 \\
k_i &= \frac{\omega_c^2}{k} = 10044 \\
\omega_p &= k\omega_c = 59.3 \text{ Hz}.
\end{align*}$$

D. Ride Through

Another important feature of a PLL for grid-connected power conditioning systems is the ride-through capability, meaning that, the PLL has to remain synchronized with the grid voltage during the abnormal conditions such as the severe voltage sags. Voltage sags are the most common power quality disturbances in the utility grid [39]. They are transitory in nature, and mainly caused by switching of large loads, energizing of transformers, connection of large induction motors, and short-circuit faults. When a voltage sag occurs, thanks to the action of the amplitude compensation block, a fast estimation (about one cycle of the fundamental frequency, as shown in Fig. 13) of the input voltage amplitude is achieved, making the proposed DFAC-pPLL insensitive to the grid voltage amplitude variations during the steady-state condition.

In the case of line outages, or when the grid faults cause the input voltage amplitude reduces to almost zero, the PLL may not be able to work properly. The reason is that, even under such conditions, the loop filter tries to track the reference signal. To assure the ride-through capability, the structure shown in Fig. 14 is recommended [7], [40]. Here, the grid voltage is
continuously monitored by a line quality algorithm, which can be a voltage amplitude monitoring algorithm in its simplest form. Once an unacceptable grid condition is detected, the loop filter is disconnected from the PD so that the output signal of the PLL remains on its nominal condition. Obviously, the threshold values for detecting the unacceptable grid condition depend on the application where the PLL is used, and can be chosen in accordance with the standards EN 50160 [38], IEEE 1547.1-2005 [41], UL 1741 [42], and IEC 61727 [43], or the national grid codes.

VI. PERFORMANCE EVALUATION

In the following, the performance of the proposed DFAC-pPLL has been evaluated through extensive simulations in MATLAB/Simulink environment, and experiments based on a TMS320F28335 floating-point 150-MHz digital signal controller from Texas Instruments. The sampling frequency has been fixed to 10 kHz, and the nominal frequency has been set to 60 Hz. To generate the desired input voltage in experimental verifications, a programmable ac voltage source has been utilized.

A. Phase Jump

Figs. 15 and 16 depict the simulation and experimental results, respectively, when a phase jump of $40^\circ$ occurs in the input voltage. It can be seen that the phase error decays to zero in about 40 ms (i.e. less than 2.5 cycles), and the overshoot is limited to $15^\circ$. Notice that the simulation and experimental results are in perfect agreement.

B. Frequency Jump

Figs. 17 and 18 illustrate the simulation and experimental results, respectively, when the input voltage undergoes a frequency jump of 5 Hz. As shown, the estimated frequency is locked to the real one in about 40 ms (i.e., less than 2.5 cycles). The phase-error peak is about $10^\circ$ in this condition.
C. Voltage Sag

Figs. 19 and 20 show the simulation and experimental results, respectively, when the input voltage undergoes a voltage sag of 30%. As shown, the phase-error settling time is less than one-and-a-half cycles. During the transient, the peak-to-peak value of the phase error is limited to $4^\circ$.

D. Harmonic Distortion

Figs. 21 and 22 illustrate the simulation and experimental results, respectively, when 15% third-harmonic component is injected into the input voltage. As shown, the harmonic distortion causes a peak-to-peak phase-error of about $1.7^\circ$ in the steady state. It is worth mentioning that this error can be further reduced by selecting a lower crossover frequency $\omega_c$ (and hence higher attenuation at the disturbance frequencies), but at the expense of degrading the transient behavior of the PLL.

E. Noise Immunity

The degree of the noise immunity of the DFAC-pPLL is investigated in this section. For this reason, the voltage $v_i$ is contaminated by a zero-mean white Gaussian noise of variance 0.05. Considering a unity value for the input signal amplitude, the signal-to-noise ratio (SNR) at the input terminal is [44]

$$\text{SNR}_{\text{in}} = 10 \log \left( \frac{V^2}{2\sigma^2} \right) = 10 \text{ dB}$$  \hspace{1cm} (46)

where $\sigma^2$ is the noise variance.

Fig. 23(a) illustrates the noise-corrupted input signal (dark line) and output signal (light line) of the PLL. It can be seen that
Fig. 22. Experimental results for 15% third-harmonic injection: Ch1 denotes the input voltage (26 V/div), Ch2 denotes phase error (1.5°/div).

Fig. 23. Degree of noise immunity of the proposed DFAC-pPLL: SNR_{in} = 10 dB (a) input (dark line) and output (light line) signals, (b) input (dark line) and output (light line) noises.

the proposed PLL yields high degree of noise immunity. The output noise is about one-tenth of the input noise [see Fig. 23(b)].

F. Comparison

Table I provides a comparison between the results obtained from the DFAC-pPLL, and the ones obtained from pPLL, park-PLL, and Enhanced PLL (EPLL). The parameters of these three PLLs (i.e. pPLL, park-PLL, and EPLL) are set equal to the values suggested in [7], yielding almost the same bandwidth for the EPLL (40 Hz), and the park-PLL (45 Hz) as compared to the DFAC-pPLL (42 Hz). The pPLL bandwidth is much lower (about 24 Hz), which is unavoidable, due the the high attenuation required at twice the input voltage fundamental frequency. The results shown in Table I highlight the promising performance of the proposed DFAC-pPLL.

Table I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>pPLL</th>
<th>Park-PLL</th>
<th>EPLL</th>
<th>DFAC-pPLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>+40° phase-angle jump</td>
<td>7 cycles</td>
<td>3 cycles</td>
<td>2.5 cycles</td>
<td>2.4 cycles</td>
</tr>
<tr>
<td>Overshoot</td>
<td>23°</td>
<td>14°</td>
<td>15°</td>
<td>15°</td>
</tr>
<tr>
<td>+5 Hz frequency jump</td>
<td>7 cycles</td>
<td>3 cycles</td>
<td>2.5 cycles</td>
<td>2.4 cycles</td>
</tr>
<tr>
<td>Peak phase error</td>
<td>30°</td>
<td>9°</td>
<td>2.5 cycles</td>
<td>10°</td>
</tr>
<tr>
<td>Voltage sag of 30%</td>
<td>5 cycles</td>
<td>2 cycles</td>
<td>2.5 cycles</td>
<td>1.2 cycles</td>
</tr>
<tr>
<td>Setting time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15% 3rd harmonic injection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak-to-Peak phase error</td>
<td>≈ 0°</td>
<td>3°</td>
<td>5°</td>
<td>1.7°</td>
</tr>
<tr>
<td>Phase margin</td>
<td>31°</td>
<td>35.3°</td>
<td>61.3°</td>
<td>44.76°</td>
</tr>
<tr>
<td>Noise immunity</td>
<td>perfect</td>
<td>good</td>
<td>fair</td>
<td>good</td>
</tr>
<tr>
<td>Computational load</td>
<td>2.58 μs</td>
<td>3.8 μs</td>
<td>3.04 μs</td>
<td>3.96 μs</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

To overcome the drawbacks associated with the pPLL, a simple and effective method, called DFAC method, was proposed in this paper. Through a detailed mathematical analysis it was shown that the suggested method successfully compensates for the undesired double-frequency oscillations, as well as the input voltage amplitude variations, while keeping a fast dynamic response and robust performance for the PLL. A systematic design procedure to fine-tune the PLL parameters was then proposed, which guarantees a fast transient response, a high disturbance rejection capability, and a robust performance. To confirm the promising performance of the DFAC-pPLL, extensive simulation and experimental verifications were provided.

REFERENCES


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