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An offset cancellation technique for comparators using body-voltage trimming

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Abstract A novel offset cancellation technique based on body-voltage trimming is presented to be used in the comparators employed in high-speed analog-to-digital converters (ADCs) such as Flash ADCs. The proposed offset cancellation is achieved by body-voltage adjustment using a low-power simple analog control feedback circuit without any additional capacitive loading at the comparator output or complicated digital calibration scheme. The accuracy of the proposed technique is higher than its digital calibration counterparts due to its analog nature. Simulation results in a 1.8 V 0.18 μm CMOS technology show that using the proposed technique the standard deviation of the comparator offset is significantly reduced from 36.2 to 7.1 mV operating at 1 GHz with only 32 μW of power dissipation in the offset cancellation circuit.

Keywords Offset cancellation technique · Clocked dynamic comparator · body-voltage trimming

1 Introduction

A voltage comparator is a principal building block in many analog-to-digital converters (ADCs) with significant impact on the resolution and/or speed of the ADC [1]. The ADCs often require the comparators to be low-power, low offset, high-speed with small area. While high-speed and low-power operations are benefited from technology scaling, the reduction of feature size leads to a larger mismatch of transistors. Therefore, many offset cancellation or calibration techniques have recently been presented in order to improve the accuracy of the comparators and consequently the performance of the ADC [2–5].

Most common offset cancellation techniques are based on using pre-amplifiers with input/output offset storage (IOS/OOS) techniques [1]. However, often a high-gain, wide-bandwidth and thus power-hungry preamplifier is needed. In [2], a digital calibration technique was proposed, which calibrates the comparator offset through unbalancing the output load of the comparator using arrays of MOS capacitors at each output. The number of MOS capacitors increases proportional to the increase in the resolution, thus affecting the speed of the comparator and calibration accuracy. Another calibration technique is proposed in [3] in which a pair of calibrating transistors is shunt with the comparator input transistors. A resistive ladder generates the voltages which are applied to the gate of the shunt transistors using multiplexers. Although, this technique can achieve large calibration range but the accuracy of the reference voltage has to be better than the calibration resolution. In [4], an offset calibration is presented based on unbalancing the output loads using a single MOSCAP at each output. Using single MOSCAP at the comparator output has less effect on the speed; however, since during each calibration clock, one reference voltage from the thermometer reference ladder has to be applied until the essential control voltage is detected, several clock cycles are required for the comparator to significantly reduce the offset in the worst mismatch condition. In [5] a digitally-controlled bulk voltage trimming calibration is proposed. A calibration DAC is used to generate voltages above power supply in order to be applied to the body of one of the input transistors. This will increase the threshold voltage, decreasing its current. Calibration cycle

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continues until both input currents equalize. Nevertheless, generating voltages above power supply will decrease the reliability of the operation of transistors in deep submicron technologies, while making use of resistor DAC will lead to static power consumption and extra offset. More importantly, in digital calibration techniques the accuracy is limited by the accuracy of the calibration DAC [2]. Similar to [5], in [6] a digital offset calibration technique based on bulk voltage trimming is presented. However, instead of using extra power supply and a resistor ladder to generate the variable bulk voltage, a bulk voltage generator is proposed which employs simple logic and binary-scaled capacitor array. Hence, it is claimed that the calibration does not consume any quiescent current and the offset calibrating range is increased by a factor of two over previous technique [6]. However, the body parasitic capacitances reduce the accuracy of the calibration. Besides, since there is a discontinuity in the voltage values which are applied to the bodies, the accuracy of the technique is limited. To overcome this problem, our proposed offset cancellation scheme offers continuous variation of the body-voltage for offset cancellation which profoundly increases the accuracy of offset cancellation.

In this work, a new high-resolution offset cancellation technique based on body-voltage trimming is proposed which does not require accurate reference voltages or additional capacitor array at comparator outputs. The idea is based on trimming the threshold voltages of the devices by changing the body-voltage using a simple low-power analog feedback circuit. The initial idea of this offset cancellation control feedback network was proposed in [7]. But in this work we have developed a modified control feedback network which has significantly improved the performance in suppressing the effect of offset when compared with the idea presented in [7]. As confirmed by simulation results, the proposed technique can be applied in design of many high-resolution, moderate-/high-speed ADCs.

The rest of this paper is organized as follows. In Sect. 2 the formula for the offset of the preamplifier is derived and the description of the proposed offset cancellation scheme is given in Sect. 3. Circuit design issues are addressed in Sects. 4 and 5 presents the simulation results followed by conclusions in Sect. 6.

2 The comparator structure and offset analysis

In this section, first the structure of the comparator used in this work will be explained. Then, a discussion about the value of the input-referred offset voltage and its sources will be presented. Finally, two scenarios will be presented for reducing the offset voltage, one of which to be used as a principle of the proposed technique.

A typical comparator consisting of a preamplifier followed by a dynamic latch is employed in this work and shown in Fig. 1. Both the preamplifier and the latch employed in the comparator, have the advantages of low-power and high-speed operation and are widely used in flash ADCs [4–6]. The operation of the comparator is as follows. When the clock is at V_{DD}, the outputs of the latch are reset to ground (by transistors M_{r1}–M_{r2}), also transistors M_{s1}–M_{s2} disconnect the latch from the preamplifier. These transistors have been added in order to reduce the effect of kickback noise. Besides, the preamplifier and latch tail transistors (M_{tail1} and M_{tail2}) are cut-off. After the reset phase, when the clock becomes low, the tail transistors turn on and the preamplifier input transistors force the input-dependent current into diode-connected devices (M_3–M_4). While latch reset transistors (M_{r1}–M_{r2}) are cut-off, transistors M_{s1} and M_{s2} are turned on, connecting the intermediate stage transistors (M_5–M_6) to the latch. The intermediate stage passes the preamplifier differential voltage ($\Delta V_{pre,outn/p}$) to the cross-coupled inverters, making the latch regenerate. The gain of the preamplifier is chosen in such a way that the input-referred offset voltage of the latch is reduced to a value smaller than the acceptable value for the ADC while providing the required bandwidth. In this work, the preamplifier gain is set at three.

The total input-referred offset of the preamplifier-latch comparator ($V_{os\text{-}total}$) is obtained from [1]

$$V_{os-total} = V_{os,\,preamp} + V_{os,\,latch}/A_0 \tag{1}$$

where $V_{os,\,preamp}$ and $V_{os,\,latch}$ are the input-referred offset voltage of the preamplifier and latch, respectively and A_0 is the gain of the preamplifier. Due to the fact that the effect of the latch offset is greatly reduced by the gain of the preamplifier, the preamplifier offset has prominent effect on the total equivalent input-referred offset voltage; hence cancelling it will lead to significant reduction in the total input-referred offset.

In obtaining a formula for the input-referred offset of the preamplifier, the mismatch between input transistors has the most contribution to the overall offset. Thus, for convenience, the small effect of the mismatch of the diode-connected load transistors (Transistors M_3–M_4 in Fig. 1) is neglected and only the effect of the threshold mismatch (ΔV_t) and current factor mismatch ($\Delta\beta$) of the input transistors have been considered. Ignoring offset cancellation network (shown in Fig. 1), it can be shown that the variance (σ^2) of the input-referred offset voltage of the preamplifier (ΔV_{eq}) is obtained from [8]

$$\sigma^2(\Delta V_{eq}) = \sigma^2(\Delta V_t) + \left[\frac{(V_{gst})}{2}\sigma\left(\frac{\Delta\beta}{\beta}\right)\right]^2 \tag{2}$$

where V_{gst} and β are the gate over-drive voltage and the current factor of the input transistors, respectively. Substituting the mismatch formulas from [8] in (2), the offset voltage can be rewritten as

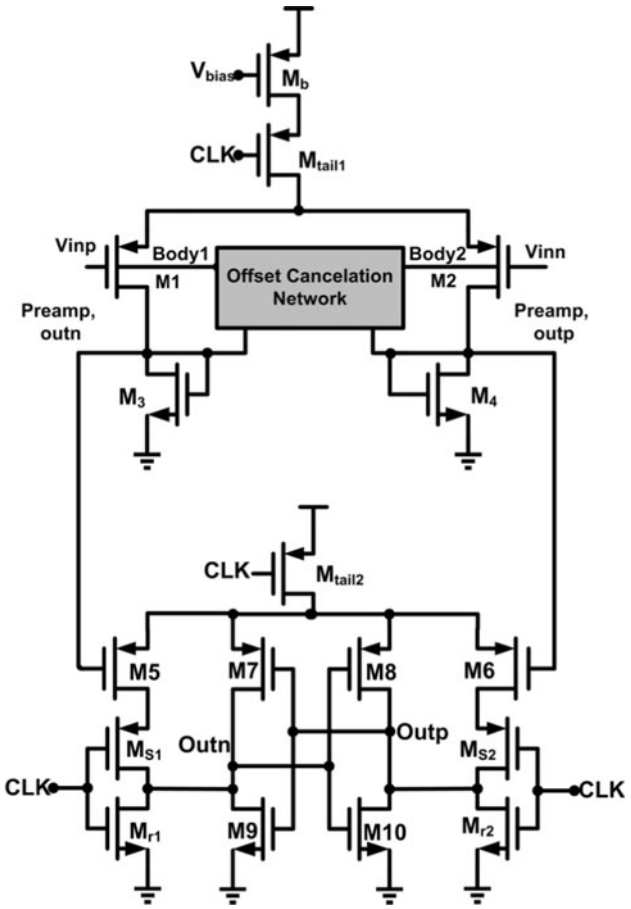

Fig. 1 The schematic of the comparator: preamplifier and dynamic latch

$$\sigma^2(\Delta V_{eq}) \approx \frac{1}{W.L}\left[A_{V_t}^2 + \frac{A_\beta^2}{4}(V_{gst})^2\right] \quad (3)$$

where A_{V_t} and A_β are process-dependent parameters along with W and L being the width and the length of the input transistors, respectively. In this calculation, the effect of the distance (D) in the formulas presented in [8] has been neglected due to its minor contribution to the overall mismatch [9].

Equation (3) indicates that in a given technology, larger transistors are needed to reduce the offset, however, more parasitic capacitances will appear and more power is needed. Hence V_{gst} is the parameter which can be used in reducing the offset.

Substituting V_{gst} [in (3)] in terms of input common-mode voltage (V_{cm}), it can be shown that the input-referred offset voltage of the preamplifier (ΔV_{eq}) is approximately dependant on the square root of ($V_{cm} - V_{Th}$), where V_{Th} is the threshold voltage of the input transistors. Based on this, the main idea behind the proposed offset cancellation technique is to use body-voltage trimming in order to change the threshold voltage of the one of the input PMOS transistors (M_1/M_2) in such a way that the differential current (i_{diff}), generated due to the mismatch effect, will be cancelled.

In an n-well technology, employing PMOS devices makes it possible for input transistors to be placed in different n-wells for adjusting their body-voltages individually. However, this technique can be also used in comparators with NMOS input pair with deep n-well (or p-well) fabrication processes.

As we know, the threshold voltage of a PMOS transistor, $|V_{Thp}|$, can be expressed as follows [5]

$$|V_{Thp}| = |V_{Th_0,\,p}| + |\gamma|\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right) \quad (4)$$

where $|V_{Th_0}, p|$ is the threshold voltage at $V_{SB} = 0$, ϕ_f is the Fermi voltage and γ is the body-effect coefficient.

In order to demonstrate the effectiveness of changing the threshold voltage in offset cancellation scheme, the effect of varying the body-voltage of one of the preamplifier input devices (e.g. transistor M_2) on both the threshold voltage of the device and the output voltage of the amplifier has been investigated as shown in Fig. 2. It can be seen that when V_{SB} is swept from -0.2 V to nearly 0.4 V, $|V_{Thp}|$ can vary about 175 mV resulting in 52 mV change in the preamplifier output voltage.

It is obvious that adjusting the body-voltages of the input devices would be an effective approach in offset cancellation scheme to cover the effect of both threshold mismatch (ΔV_t) and current factor mismatch ($\Delta\beta$).

It seems that both increasing and decreasing the threshold voltage can lead to offset reduction. Here, we will compare these two scenarios from different viewpoints.

2.1 Increasing threshold voltage

The first scenario is that the body-voltage of the input transistor which provides less current (due to the mismatch; $\Delta\beta$ or ΔV_t) is fixed at V_{DD}, while the other one (body of the transistor with more current) is raised above V_{DD}. In this case, the threshold voltage of the input transistor which provides more current will be increased, leading to the decrease in its drain current. The offset cancellation will continue until both currents equalize. In [5], similar approach has been used. It is claimed that a voltage higher than V_{DD} can generally be accommodated in current CMOS processes, in which multiple voltage supply levels are generally available [5]. Although in this approach the reverse-biasing of source-body junctions are assured, however, a question may arise that to what extent the voltage can be increased above V_{DD} without causing reliability concerns.

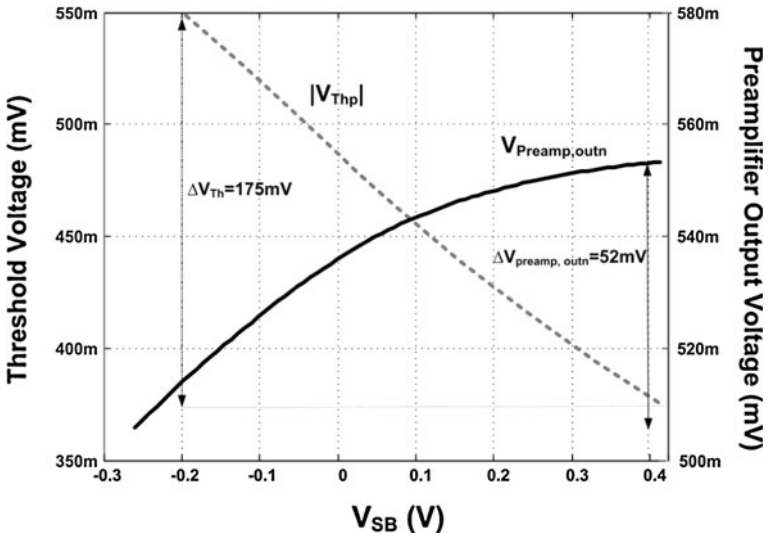

Fig. 2 Absolute threshold voltage of transistor M_2 (*dashed gray line*) and the related preamplifier output (*black line*) versus V_{SB} in nominal 0.18 μm CMOS process and temperature corner

2.2 Decreasing threshold voltage

The second scenario is to reduce the body-voltage of the input transistor (with less current) so that due to the reduction of threshold voltage, its drain current increases. The body-voltage of the other transistor is fixed to V_{DD}. In this approach, there is no concern for reliability issues but we have to make sure that the source-body parasitic diodes remain reverse-biased and the body leakage current is far below the allowed value so that the normal operation of the transistors is guaranteed.

Our proposed offset cancellation technique is based on the second scenario, however, special systematic design considerations have been made to ensure reverse-biasing of the source-body junction diodes.

3 Proposed offset cancellation scheme

The block diagram of the proposed offset cancellation scheme is illustrated in Fig. 3, which consists of the pre-amplifier-latch comparator, offset and polarity detector, two multiplexers (MUX) and an offset cancellation control feedback network.

Offset cancellation is performed in foreground during which the normal operation of the ADC is interrupted. The main concept of the proposed technique is to cancel the offset of the preamplifier through adjusting the body-voltages of the PMOS-input transistors using a simple low-power analog feedback network. According to what described in the second scenario (i.e. decreasing the value of the threshold voltages by reducing the voltages of the body terminals), the body-voltage of the input transistor with less current is slightly decreased to reduce the threshold voltage and consequently to increase the drain current. This is done via slightly discharging a pre-charged capacitor connected to the body terminal of the corresponding device until the differential mismatch current of two input transistors is cancelled. Circuit design considerations for ensuring reverse-biasing of source-body junctions and other related issues will be discussed in details in Sect. 4.

Before calibration starts, during a short reset period, both bodies of the input transistors are charged to V_{DD} in order to remove previous adjustments. During the offset cancellation cycle, the common-mode voltage V_{cm} is applied to both input transistors of the preamplifier. Due to the mismatch, the outputs of the preamplifier differ. First, the polarity of the offset is detected. Then, one of the two input transistors which provides less current (in comparison with the other transistor), is detected and through multiplexers, its body is connected to ground through a resistor and a switch whose gate is controlled by a zero-crossing detector (ZCD). The body of the other transistor is connected to V_{DD}.

The principle of the operation of the control feedback is as follows: while preamplifier outputs ($V_{preamp,outn}$ and $V_{preamp,outp}$) differ, based on offset polarity, the larger output is connected to the non-inverting input of the ZCD and the other output is connected to the inverting input of the ZCD. Thus, at the beginning of the offset cancellation, ZCD generates a pulse which is applied to the gate of the ground-connected switch. The corresponding body, whose voltage should reduce, is connected through multiplexer to the switch. When the body-voltage is reduced from V_{DD}, the threshold voltage of the transistor decreases (as illustrated in Fig. 2); hence the transistor drain current is increased and the corresponding output voltage will increase proportionally. This procedure continues until the voltage difference between two outputs becomes sufficiently

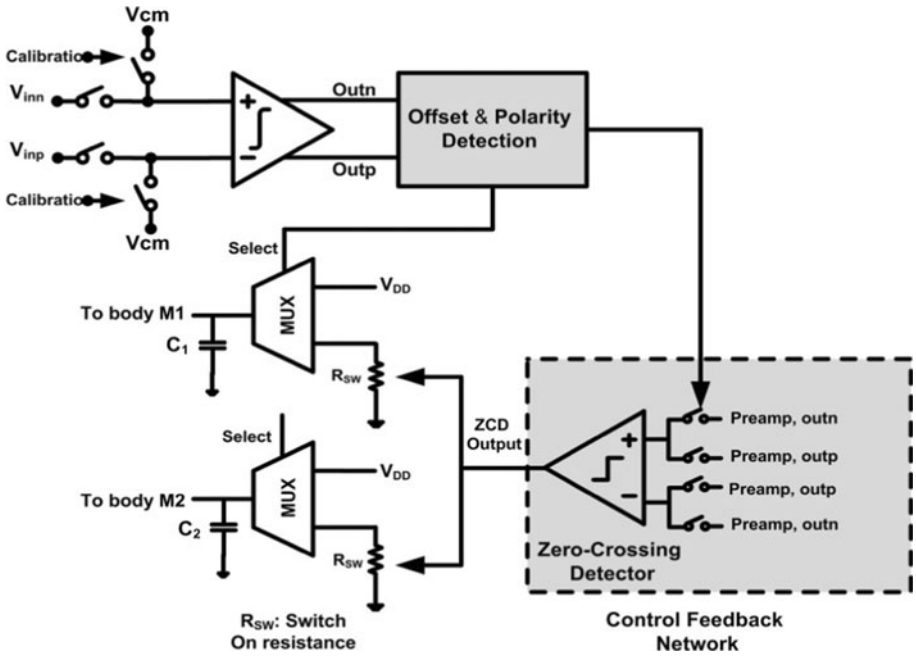

Fig. 3 *Block diagram* of the proposed offset cancellation scheme

small where the ZCD generates a zero output. Then, the switch connected to the body will turn off and the body capacitor holds its voltage until the next calibration cycle. Fig. 4 demonstrates how the offset cancellation is performed for a practical example. In this example, an intentionally inserted output offset voltage of 14 mV is reduced to 100 μV after a narrow ZCD pulse reduces the body-voltage of one of the input devices from 1.8 V down to 1.738 V. Note that the time constant according to which the body-voltage decreases is defined by the capacitor value and the on-resistance of the switch as will be discussed in Sect. 4.3.1.

4 Circuit implementation

4.1 Comparator

The structure of the comparator is discussed in Sect. 2. As discussed before, any mismatch between the input transistors contribute the most in the preamplifier total offset as far as they control the currents to the loads. According to the equations derived for the input-referred offset voltage of the preamplifier (2 and 3), $V_{cm} - V_{Th}$ affects ΔV_{eq} in approximately square root dependence. In order to reduce this dependency, a simple and effective way is to use a saturated MOS transistor (M_b in Fig. 1) stacked to the switch transistor (M_{tail1}) [10]. Since M_b is biased in saturation, its current slightly varies with the variation of its drain-source voltage; therefore, it keeps the effective voltage of the input devices nearly constant when input common-mode voltage (V_{cm}) is changed. Using this technique, the input-referred offset voltage (Eq. 3) would be a function of the device size and threshold voltage, almost independent of input common-mode voltage.

4.2 Offset cancellation network

Figure 5 demonstrates the offset cancellation components. It consists of a ZCD, two multiplexers, logic circuits for offset polarity detection and two body capacitors.

4.2.1 Zero-crossing detector (ZCD)

A simplistic approach for realizing a ZCD is to use an open-loop opamp [11] as shown in Fig. 5. The following two-stage opamp is designed in such a way that a 0.5 mV input voltage difference is transferred to 1.8 V differential output. As a result the gain of the opamp must be nearly 72 dB. The offset and limited slewing of the ZCD are the non-ideal effects and will be discussed in Sect. 4.3.

4.2.2 Multiplexers and body capacitors

Two multiplexers, implemented by four transmission gates (TGs) are used for connecting the corresponding body to the ground-connected switch while leaving the other body terminal connected to V_{DD}. The size of TG transistors is determined in a way that the desired discharging time constant for body capacitor switch combination is achieved.

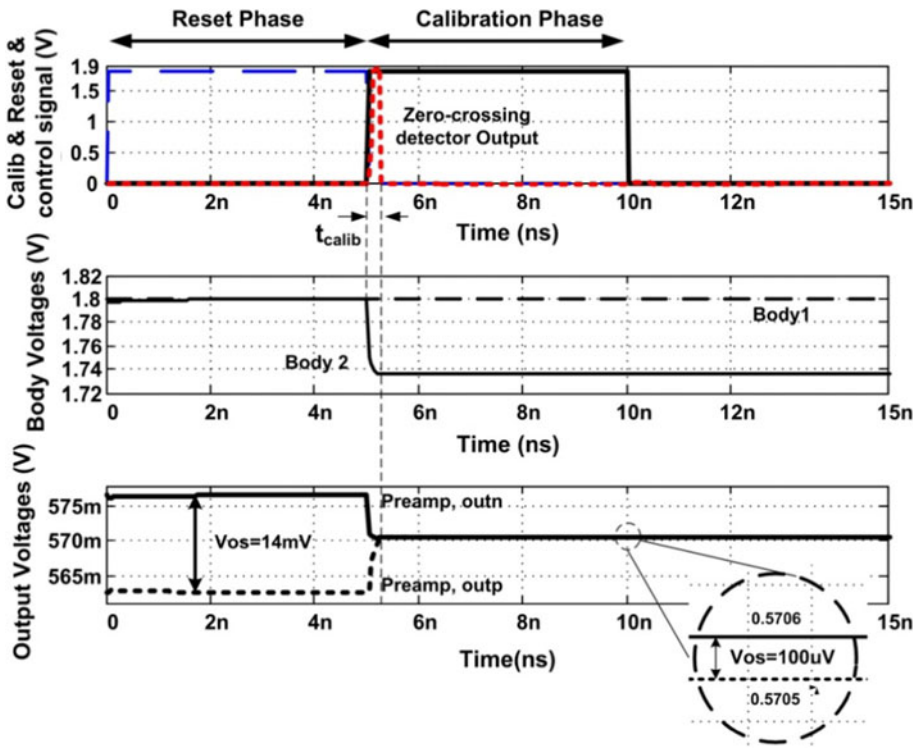

Fig. 4 Signal behaviour of preamplifier outputs under offset cancellation

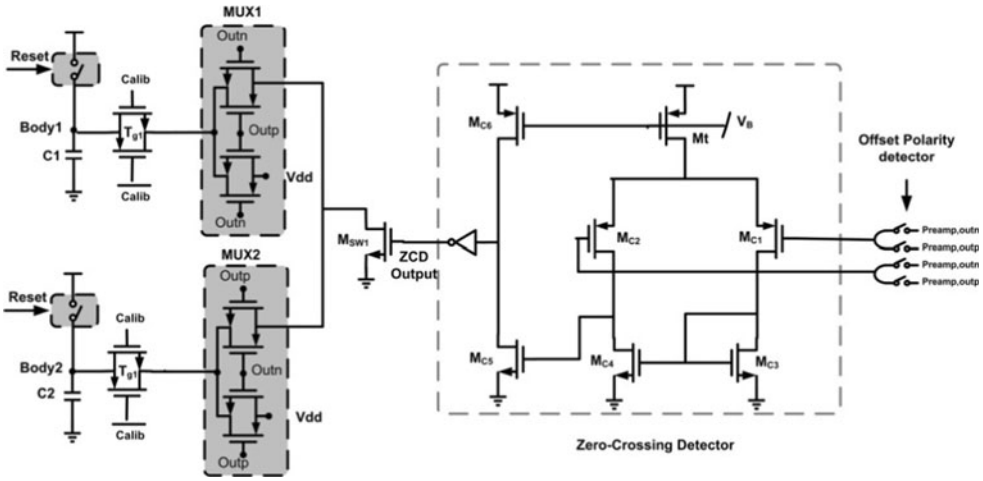

Fig. 5 The schematic of the offset cancellation network

As will be discussed further, by using TGs the errors induced in body-voltage due to the charge-injection of the switches is remarkably reduced.

In selecting the value of body capacitors two important factors should be considered:

First, the time interval between calibration cycles depends on the value of body capacitors. The bigger the capacitor is selected, the longer time capacitor holds the adjusted body-voltage (i.e. the longer time after which the offset cancellation should be repeated). Second, increasing the size of the capacitor, will lead to an increase in the area. Besides, since the value of the capacitor multiplied by the on-resistance of switches comprises the discharging time constant of the body capacitor switch combination, by assuming a logical value for the switch transistor sizes, an upper value for the capacitor size is determined which should be considered in designing the value of the body capacitors.

4.3 The influence of circuit non-idealities on the offset cancellation scheme

In the proposed offset cancellation technique, there exist some important design criteria which should be carefully

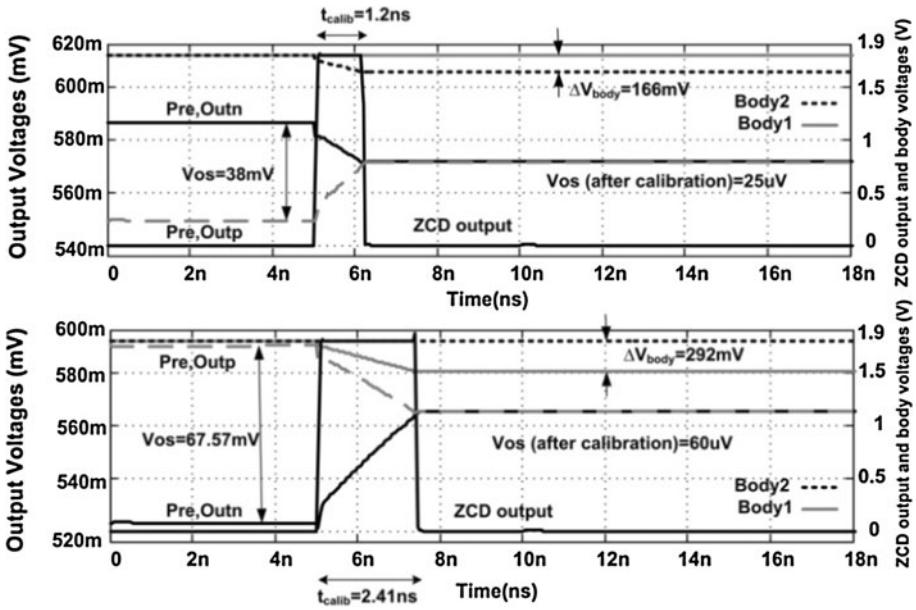

Fig. 6 Two different offset cases showing the time requires for offset cancellation

analyzed and considered. These criteria include: ensuring reverse-biasing condition of source-body junction, non-idealities of switches and ZCD. Hence these issues are discussed in this section. Not only the reverse-biasing condition of source-body junctions must be satisfied, but also the non-idealities of switches and ZCDs must be considered. Hence these issues are discussed in this Section.

4.3.1 Ensuring reverse-biasing of source-body junction

To ensure the reverse-biasing condition of the source-body junction, in this work we have taken design solutions which promise that V_{SB} will change in the possible allowed range (e.g. $V_{SB} < 0.4$ V).

As mentioned, in the proposed scheme, the body discharges during the time ZCD output is high and consequently the ground-connected switch is on. As mentioned before, the discharging rate is defined by the value of the body capacitor and on-resistance of the switches (Muxs switches plus discharging switch). The value of the body holding capacitor is determined according to the fact that they would be able to hold the calibration voltage till the next calibration phase. For high-speed ADCs, the leakage voltage due to the leakage current is ignorable (simulation results confirm this matter). Based on the leakage current, the sampling frequency of the ADC and the size of the capacitor, the frequency at which the calibration process must be repeated are chosen. After determining the capacitor value, the size of the switch must be determined in a way that during the calibration phase (i.e., the maximum time during which the switch might remain on), the maximum capacitor voltage loss from supply voltage will satisfy the condition V_{SB} <0.4 V. As illustrated in Fig. 6, depending on the amount of offset between preamplifier outputs, the time it takes for the output voltages to get very close to each other differs. For instance, for initial offset voltage of 38 mV, it takes 1.2 ns for the outputs to reach each other (according to the designed body-discharging rate) and for the initial offset of 67.57 mV, 2.41 ns is required to achieve an output offset of 60 μV. Therefore, the calibration phase is designed in such a way that with the specified discharging rate of the body-voltage, i.e. τ_{disch}, maximum drop of the body-voltage would be limited to the level which satisfies the condition V_{SB} <0.4 V in order not to turn on the body-source diode. After the calibration clock falls to ground, the switch is turned off and the capacitor will hold its voltage until the next calibration cycle. For very large values of the offset, although the proposed scheme does not remove the entire offset, but it reduces the value of the offset significantly. Simulation results confirm that even for worst-case offset voltages, the value of V_{SB} is far below the margin [see Fig. 7(a)].

In our design, the value of 0.5 pF has been selected for the body capacitors, and calibration phase will be repeated every 40 cycles of ADC operation (for $f_s = 1$ Gs/s). Considering 5 ns for the calibration phase (see Fig. 4), the on-resistance of the switches and consequently their size is determined by solving the following equation,

$$V_s - V_{Body} = V_s - V_{DD} \cdot \exp(-(t = 5ns)/\tau_{disch}) = 0.4 \text{ V} \quad (5)$$

where τ_{disch} is the discharging time constant of the switch-body capacitor. Overestimation is considered in designing the value of parameters, since the simulation results confirm that even in worse-case mismatch conditions, the time

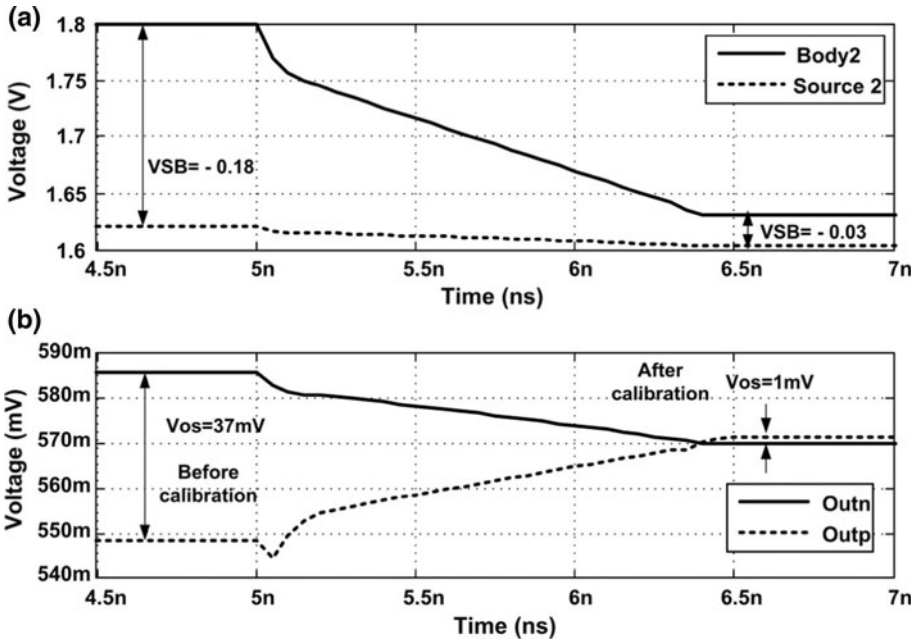

Fig. 7 The effect of switch-induced errors on the offset cancellation scheme **a** voltages of the body and the source terminals of M2, **b** output voltages

it takes till both preamplifier outputs match (during which the switch is on) is less than the calibration phase. In our design, the maximum value of the output offset which is entirely removable using the proposed offset cancellation scheme is equal to 98 mV.

4.3.2 Switch-induced error voltages

Switch non-idealities including charge-injection, clock feed through and leakage are among the most error sources of this offset cancellation scheme.

Our simulations show that underestimating these effects will degrade the accuracy of the offset cancellation scheme as shown in Fig. 7(b). However, using CMOS transmission gate as the switch with proper sizing and employing dummy switches [12] these non-ideal effects have been alleviated.

4.3.3 Zero-crossing detector non-idealities

Another important source of error is the offset of the ZCD. ZCD output controls turning on and off of the switch through which the body capacitor voltage is controlled. It is evident that the accuracy of the offset cancellation scheme directly depends on the accuracy of the ZCD. Not only the offset of the ZCD but also its speed affect the accuracy of the entire scheme. The latter is important since any delay in turning off the switch will lead to inaccuracy. There is a trade-off between the speed and offset of the ZCD amplifier; however, the speed requirement of the ZDC amplifier is not as stringent as the main comparator since it is not located at the main signal path.

Owing to the ZCD non-idealities, similar to the effect of charge-injection, although offset is reduced but the accuracy of cancelling offset is affected by the accuracy of the ZCD.

5 Simulation results and discussions

In order to verify the operation of the offset calibration scheme, the comparator is simulated in a 0.18 μm CMOS technology with a supply voltage of 1.8 V. All devices are typical transistors with nominal threshold voltages. Initially, different values of mismatch are intentionally applied to the inputs of the preamplifier and the changes in the source-body-voltage of the detected input transistor (the one which provides less current) is measured. As illustrated in Fig. 8, even for input-referred offset voltages in the order of 23.3 mV (equal to 70 mV output offset voltage), the source-body of the corresponding input transistor is set at about 0.1 V (with no harm for the source-body junction diode). The results of the Monte Carlo analysis also confirm that in more than 75 % of different mismatch events, V_{SB} remains negative while for the rest of other mismatch events V_{SB} is remained much below the allowed range (i.e. V_{SB} <0.4 V); this means that our proposed solution for ensuring reverse-biasing is promising.

The time it takes for the offset cancellation network to cancel/reduce the offset, depends approximately in a linear manner on the value of the preamplifier input-referred offset voltage. This is shown in Fig. 9. Depending on the size of the body capacitors (which is selected based on the time it should hold the adjusted voltage till the next

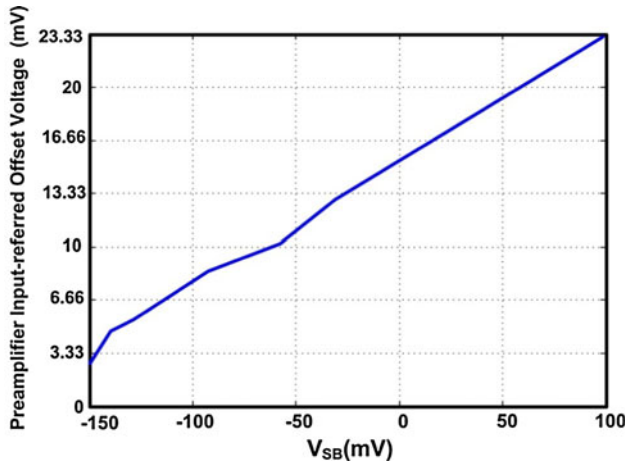

Fig. 8 Preamplifier input-referred offset voltage versus source-body variation of the corresponding input transistor

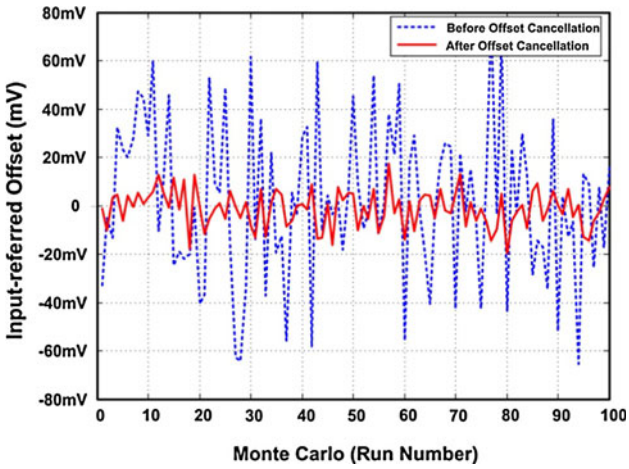

Fig. 10 Monte Carlo simulation of the offset in comparator (before and after offset cancellation)

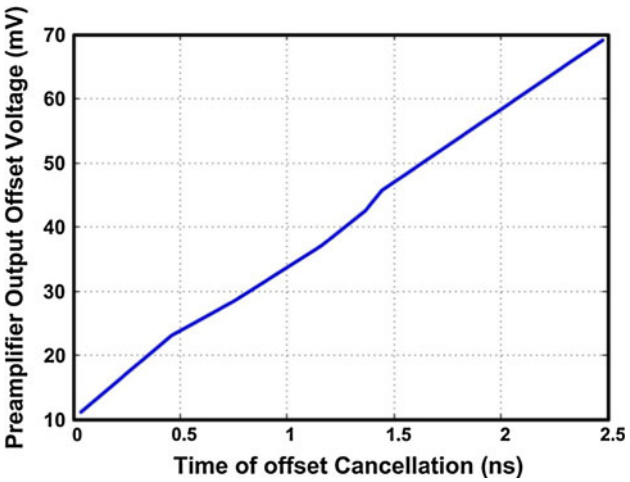

Fig. 9 preamplifier input-referred offset voltage versus time of offset cancellation

calibration cycle), offset cancellation time is determined. For instance, in our design ($C_{body} = 0.5$ pF), less than 500 ps is required to cancel the offset values in the orders of a few mV. It is evident that using smaller capacitors, with more frequent calibration cycles, it is possible to have smaller calibration time.

Finally in order to show the effectiveness of the proposed offset cancellation technique, Monte Carlo simulations have been performed for 300 runs. The Monte Carlo simulation is performed considering the effect of mismatches in preamplifier, latch and offset cancellation network, particularly the ZCD. 1-sigma offset value of the comparator before offset cancellation is 36.2 mV, while it has been effectively reduced to 7.1 mV after offset cancellation. Simulation results of 100 results before and after calibration are illustrated in Fig. 10. The total calibration power is 32 μW. It should be noted that the calibration network can be disabled during the normal operation of the ADC in order to save energy. Table 1 summarizes the performance of the proposed offset cancellation scheme.

Table 1 Performance summary

Technology	180 nm CMOS	
Principle of offset cancellation scheme	Body-voltage trimming	
Supply voltage	1.8 V	
Power	Comparator: 275 μW at 1 GHz	
	Offset cancellation network: 32 μW	
Standard deviation of the offset (σ_{os})	Before offset cancellation (mv)	After offset cancellation (mV)
TT at 25°	36.2	7.1
SS at 0°	32.6	6.2
FF at 90°	41	8.5

6 Conclusions

A new analog-based offset cancellation technique based on body-voltage trimming has been presented. The simple architecture of the offset cancellation network avoids any design complexity, capacitive loading or power-consuming reference ladder. Besides, the proposed offset cancellation technique offers monotonic continuous body-voltage tuning which makes it distinctive from its digital counterpart. The simulation results show that the comparator can operate at a speed higher than 1 GHz consuming 275 μW from 1.8 V power supply plus 32 μW power in calibration

network. Monte Carlo simulations of the comparator sampling at 1 GHz shows that the offset can be suppressed up to 98 % using the proposed technique in a 0.18 μm CMOS technology. The proposed technique is applicable in many high-speed ADCs such as Flash ADCs.

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