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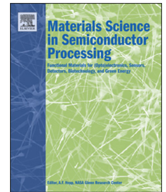

Analytical modeling of a p-n-i-n tunneling field effect transistor

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ABSTRACT

This paper presents an analytical model for the potential distribution of a p-n-i-n tunneling field effect transistor (TFET). Using the potential distribution, the tunneling drain current is derived analytically by integrating the band-to-band tunneling generation rate over the device volume. According to our knowledge, there is no analytical analysis for this structure in the literature, and this is the first analytical model proposed for a p-n-i-n TFET structure. The proposed analytical model is validated via numerical results obtained from device simulations based on non-local band-to-band tunneling model.

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1. Introduction

Tunneling field effect transistors (TFETs) have been considered as one of the most promising candidates to replace MOSFETs in the future electronics. This is because subthreshold swing (SS) of TFETs can be smaller than 60 mV/dec at room temperature, which is the physical limit of the MOSFETs [1–3]. Moreover, TFETs are superior to the MOSFETs in terms of short channel effects (SCEs) thanks to their low off-current (I_{off}) [4], which is essential for low power applications. However the low on-current (I_{on}) is a problem yet.

Analytical modeling of TFETs is pursued in the literature because of providing physical insight into the device operation and facilitates circuit-level modeling. But due to the absence of simple analytical model of the off-current in a TFET, the general principle of the off-current is not well understood. In [4] an analytical model has been presented which includes the impact of the drain voltage on the TFET drain current. The model has been developed for both a pure line-tunneling TFET and a pure point-tunneling TFET. Using Kane's model for band-to-band tunneling (BTBT) and introducing quasi-Fermi level approximations, an analytical model for the drain off-current of the TFET has been developed in [5]. The temperature dependency of the off-current has been demonstrated in [6,7]. Moreover, an analytical equation is obtained for the drain current of a structure, which has its gate placed on the source not covering the channel at all. As a result, the impact of field-induced quantum confinement under the gate and exponential integral function has been introduced for the derivation of the analytical formula of drain current in TFET [8]. By solving the two-dimensional (2-D) Poisson's equation in [9], a 2-D analytic potential model has been presented for the double-gate (DG) tunnel FETs (TFETs). Then, from the potential profile, the electric field is derived and the drain current expression has been extracted by analytically integrating the band-to-band tunneling (BTBT) generation rate over the tunneling region. p-n-i-n TFET is also studied in the literature [10]. In p-n-i-n TFET, a δ-doped n^+ region is inserted at the source-channel junction. It is shown that this region improves the tunneling rate, hence increasing the drain current.

In this paper, an analytical model is derived for the potential distribution in a p-n-i-n TFET under the subthreshold regime, and the effect of n^+ region is analytically investigated. Based on the potential distribution, an

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analytical expression is derived for the drain current. Finally, the validity of the model is shown by comparing the analytical results with numerical results obtained from Atlas device simulation software.

This paper is organized as follows. In Section 2, the device structure is explained. In Section 3, analytical modeling of the p-n-i-n TFET is proposed and the drain current is computed. Section 4 compares the analytical and numerical results. Finally, Section 5 concludes the paper.

2. Device structure

The tunnel FET structure studied in this paper is Si TFET that has four regions as p^+-n^+-i-n^+. This structure is a reversed biased gated p-i-n diode in which a δ-doped n^+ region is inserted at the beginning of the channel. This δ-doped region modifies energy band diagram of the device and hence enhances the electron tunneling from the source valance band to the channel conduction band. The gate oxide and contact have a small overlap with the source region [10]. The δ-doped n^+ width is varied between $W=0$ nm and 5 nm in order to pursue the best performance. Fig. 1 depicts the tunnel FET structure studied in this paper and Table 1 summarizes the device parameters.

In the next section, an analytical model is derived for the potential distribution along the channel. Using the potential distribution, an analytical model is derived for the drain current based on a band-to-band tunneling (BTBT) model [11,12]. The gate and the drain voltages are swept from 0 to 3 V, and the transfer characteristics, the output characteristics and I_{on}/I_{off} ratio are studied to optimize the device characteristics. In order to validate the analytical model, simulations are performed using an Atlas Silvaco device simulator, and the obtained results are discussed.

3. Analytical model

3.1. Potential distribution

As depicted in Fig. 2, the potential barriers V_{IN} and V_{PI} are formed at the channel-drain and source-channel junctions, respectively. Since the p and n regions are degenerately doped, Boltzmann's approximation cannot accurately describe carrier statistics in these regions. Therefore, expressions for V_{IN} and V_{PI} use the approximation of Fermi–Dirac distribution $F_{\frac{1}{2}}(\eta)=4\eta^{3/2}/3\sqrt{\pi}$ [6,7,13]

$$V_{IN}=(3\pi^2 N_A)^{\frac{2}{3}}\frac{\hbar^2}{2qm_e}+\frac{kT}{q}\log\left(\frac{N_C}{N_I}\right) \tag{1}$$

$$V_{PI}=(3\pi^2 N_A)^{\frac{2}{3}}\frac{\hbar^2}{2qm_h}+E_g-\frac{kT}{q}\log\left(\frac{N_C}{N_I}\right) \tag{2}$$

$$V_{bi}+V_{DS}=V_{IN}+V_{PI} \tag{3}$$

In the channel region the expression for the electric field is

$$\varepsilon(x)=\frac{1}{\varepsilon}\int \rho dx \tag{4}$$

where ρ is the charge density as depicted in Fig. 3. It must be noted that due to small width of n^+ region, this region is depleted. The n^+ region is added to the space-charge region as shown in Fig. 3. In Fig. 3, $x=0$ is the beginning of the channel region, L is the gate length and W is the n^+

Table 1
Device parameters

N_D (cm^{-3})	1×10^{19}	N_I (cm^{-3})	1×10^{16}
W (nm)	1–15	N_s and N_D (cm^{-3})	2×10^{20}
t_{OX} (nm)	2.5	$L_{channel}$ (nm)	100
t_{Si} (nm)	60	L_S and L_D (nm)	50
t_{BOX} (nm)	100	Gate	n-poly

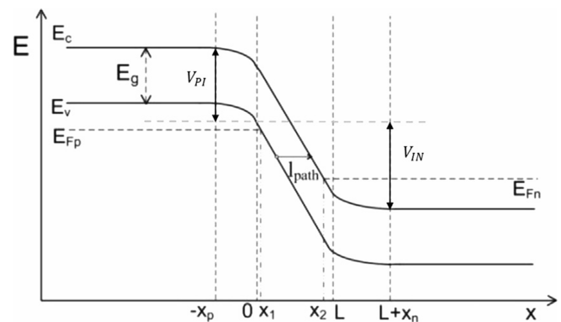

Fig. 2. Band diagram of a TFET in on state.

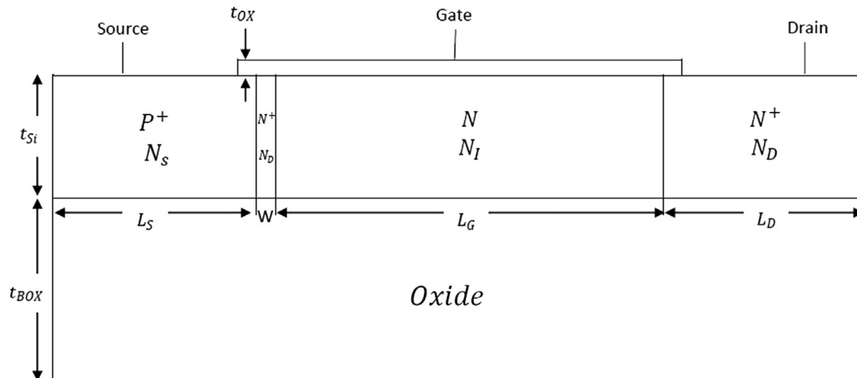

Fig. 1. Device structure of the p-n-i-n tunnel FET.

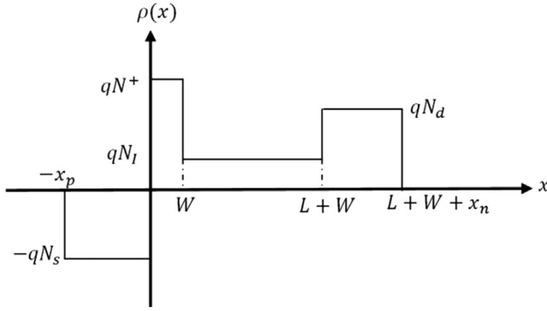

Fig. 3. Rectangular approximation of the space charge distribution.

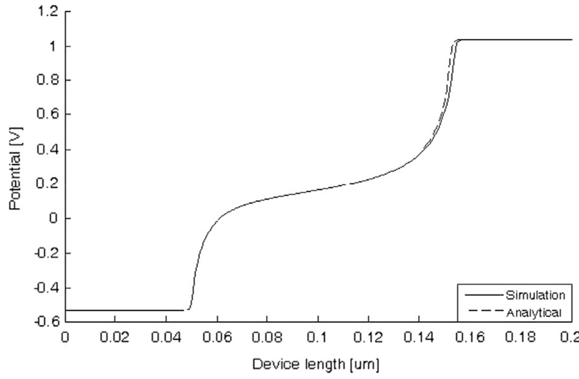

Fig. 4. Potential versus device length for V_{DS}=0.5 V and V_{gs}=0 V.

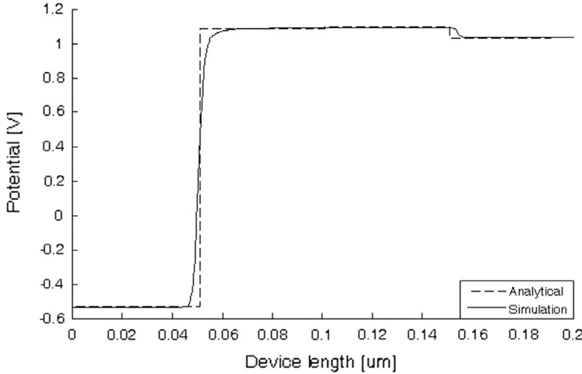

Fig. 5. Potential versus device length for V_{DS}=0.5 V and V_{gs}=2.5 V.

region width. The electric field and potential are calculated from (5)–(9). Fig. 4 shows potential distribution when V_g=0, and Fig. 5 shows potential diagram when V_g=2.5 V both are drawn by simulation and analytic.al model from which it is observed that the results are nearly the same

$$\varepsilon(x)=\begin{cases} \frac{-qN_s}{\varepsilon_s}(x_p+x) & -x_p\le x<0 \\ -\varepsilon_M+\frac{qN^+}{\varepsilon_s}x & 0\le x<w \\ -\varepsilon_W+\frac{qN_I}{\varepsilon_s}(-w+x) & w\le x<w+L \\ -\varepsilon_L+\frac{qN_D}{\varepsilon_s}(x-(L+w)) & L+w\le x<L+w+x_n \end{cases} \tag{5}$$

$$\varepsilon_M=\frac{qN_sx_p}{\varepsilon_s} \tag{6}$$

$$\varepsilon_W=\frac{qN_sx_p}{\varepsilon_s}-\frac{qN^+w}{\varepsilon_s} \tag{7}$$

$$\varepsilon_L=\frac{qN_sx_p}{\varepsilon_s}-\frac{qN^+w}{\varepsilon_s}-\frac{qN_IL}{\varepsilon_s} \tag{8}$$

Depletion region lengths in p and n regions are x_p and x_n, respectively. The potential distribution is derived from:

$$\begin{aligned} V_{bi}+V_{DS} &= -\int_{-x_p}^{L+w+x_n}\varepsilon(x)dx \\ &= -\int_{-x_p}^{0}-\frac{qN_s}{\varepsilon_s}(x_p+x)dx \\ &\quad-\int_0^w\left(-\varepsilon_M+\frac{qN^+}{\varepsilon_s}x\right)dx \\ &\quad-\int_w^{w+L}\left(-\varepsilon_W+\frac{qN_I}{\varepsilon_s}(x-w)\right)dx \\ &\quad-\int_{L+w}^{L+w+x_n}\left(-\varepsilon_L+\frac{qN_D}{\varepsilon_s}(x-(L+w))\right)dx \end{aligned} \tag{9}$$

From the charge neutrality condition, we have:

$$x_n=\frac{N_sx_p-N^+w-LN_I}{N_D} \tag{10}$$

Finally in (11), a quadratic equation is derived for x_p by which one can obtain x_p [6]

$$\begin{aligned} &\left(N_s+\frac{N_s^2}{N_D}\right)x_p^2+\left(2N_sw+2N_sL-\frac{2N_sN^+w}{N_D}-\frac{2N_sN_IL}{N_D}\right)x_p \\ &+\left(N^+w^2-2N^+wL-N_IL^2+\frac{N^{+2}w^2}{N_D}+\frac{2N^+wLN_I}{N_D}+\frac{N_I^2L^2}{N_D}\right) \\ &-\frac{2\varepsilon_s}{q}(V_{bi}+V_{DS})=0 \end{aligned} \tag{11}$$

The tunneling path (l_{path}) is defined as the physical path between two points corresponding to equal energies in the conduction and valence bands, respectively. l_{path} is derived from (12), which shows that n$^+$ region affects l_{path} through x_p [7]

$$l_{path}=\frac{\varepsilon_sE_g}{q^2N_sx_p} \tag{12}$$

3.2. Band-to-band tunneling drain current

In order to compute the drain current analytically, we upgrade the model developed in [6] and [7] to take into account the δ-doped region. The band-to-band tunneling generation rate is described by the widely used Kane's model, which determines the generation rate per unit volume, G_{Kane}, of carriers tunneling from the source valence band to the channel conduction band [4,7]:

$$G_{Kane}=A_{Kane}\varepsilon^D exp\left(-B_{Kane}E_g^{3/2}/\varepsilon\right) \tag{13}$$

where A_{Kane} and B_{Kane} are material-dependent constants, ε is the local electric field, E_g is the band gap, and D is a parameter distinguishing the direct (D=2) from the indirect (D=2.5) tunneling process [4,5]. The source–drain

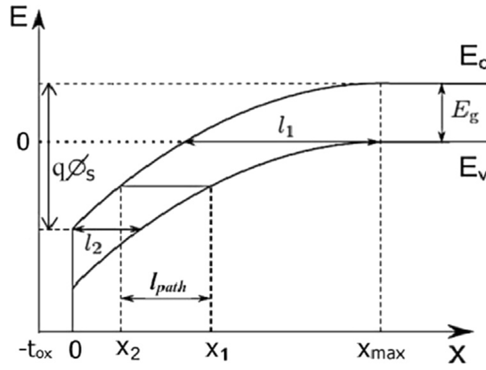

Fig. 6. Band diagram of a TFET.

tunnel current of a TFET is then given by:

$$I_{ds,tun} = q\int_{TFET\ volume} G_{Kane}dv \quad (14)$$

where V is the three-dimensional device volume where tunnel paths start (or where tunnel paths end) [4,7]

$$I_{ds} = \frac{-A_{kane}LW_dE_g^{D-\frac{3}{2}}}{2q^{D-1}B_{Kane}}(H(l_2)-H(l_1)) \quad (15)$$

where W_d is the width of the device, l_1 (l_2) is the longest (shortest) allowed tunneling path. Fig. 6 shows the corresponding energy band diagram showing l_1 and l_2. Finally, the integral of Eq. (14) is reduced to an elementary analytical formula by assuming that the exponent is varying more rapidly than the polynomial factors upon a variation of l_{path} [4]:

$$H(l) = \left(\frac{qN_s}{\varepsilon_s l_{path}}\left(\frac{l_{path}^2}{2}+\frac{E_g\varepsilon_s}{q^2N_s}\right)\right)\frac{1}{l^{D-1}}\left(1-\frac{(2E_g\varepsilon_s/q^2N_s)}{l^2}\right) \times \exp\left(-\left(B_{Kane}q\sqrt{E_g}\right)l\right) \quad (16)$$

$$l_1 = \sqrt{C_1} \quad \text{if} \quad \Delta_{vh,s} \le 0 \quad (17)$$

$$l_1 = \sqrt{\frac{C_1q}{E_g}}\left(\sqrt{\frac{E_g+\Delta E_{vh,s}}{q}}-\sqrt{\frac{\Delta E_{vh,s}}{q}}\right) \quad \text{if} \quad \Delta_{vh,s} > 0 \quad (18)$$

$$l_2 = \sqrt{\frac{2\varepsilon_s}{qN_s}}\left(-\sqrt{\varnothing_{max}-\frac{E_g}{q}}+\sqrt{\varnothing_{max}}\right) \quad (19)$$

$$\varnothing_{max} = \left(-t_{ox,eff}\sqrt{\frac{qN_s}{2\varepsilon_s}}+\sqrt{t_{ox,eff}^2\frac{qN_s}{2\varepsilon_s}+(V_{gs}-V_{FB})}\right)^2 \quad (20)$$

where ε_{ox} is the dielectric constant of the oxide, $\Delta E_{vh,s} = E_{v,s}-E_{F,h,s}$ is the energy difference between the bottom of the valence band and the hole Fermi level in the source, ε_s is the dielectric constant of the source, $t_{ox,eff}$ is the effective oxide thickness [$t_{ox,eff} = t_{ox}(\varepsilon_s/\varepsilon_{ox})$], V_{gs} is the gate–source voltage, and V_{FB} is the flat band voltage.

4. Results and discussion

Device simulations have been performed by using a Silvaco Atlas device simulator [17]. The source region is grounded. In simulations nonlocal band-to-band tunneling [14], Shockley–Read–Hall recombination, band gap narrowing, and Lombardi mobility model have been adopted. When the tunneling path (l_{path}) is too long, the band-to-band tunneling is prohibited which is dictated by the exponential dependence in (13). As a result, the tunneling current becomes low. n^+ δ-doped region decreases l_{path} and as a result, the tunneling current increases. On the other hand, when the width of this region is too large, the off state current may increase and as a result, a low I_{on}/I_{off} ratio is obtained which is unacceptable.

Therefore the optimum value of n^+ region width is pursued to obtain high on-current and simultaneously low off-current. For l_{path} less than 4 nm, the generation rate G is significant, as large number of electrons can tunnel from the valence band of the source region into the conduction band of the intrinsic channel region [15]. Hence, the BTBT current in this case is high. For l_{path} value as much as 6 nm, BTBT current remains moderately high. On the other hand, for l_{path} larger than 6 nm, BTBT current becomes insignificant and other current components of the off-current dominates over BTBT current [15,16].

In Figs. 7–11, drain currents for different widths of n^+ region W=1–5 nm are drawn. As shown, the analytical drain current and the simulation based drain current closely match for different values of W.

We depict W=1–5 nm all in one figure (Fig. 12), additionally we add W=0 and 0.5 nm to it to find optimized W. Simulation and analytical model show that without n^+

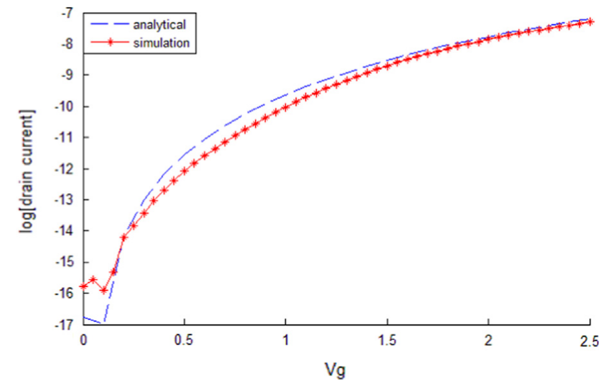

Fig. 7. Drain current versus V_{GS} for W=1 nm, with V_{DS}=0.5 V.

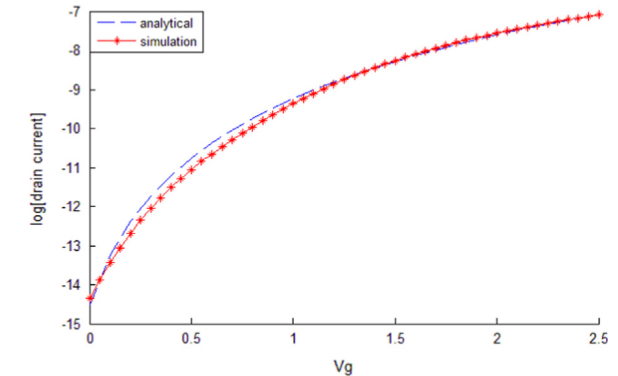

Fig. 8. Drain current versus V_{GS} for W=2 nm, with V_{DS}=0.5 V.

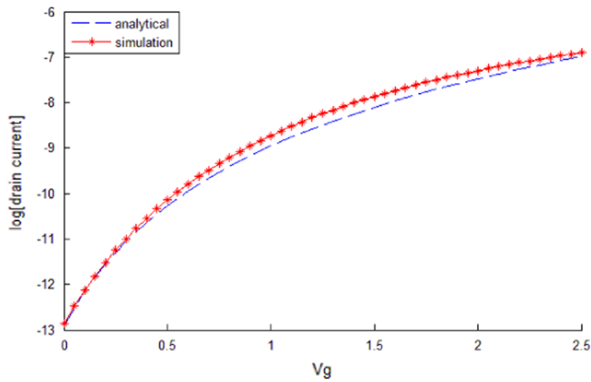

Fig. 9. Drain current versus V_{GS} for W=3 nm, with V_{DS}=0.5 V.

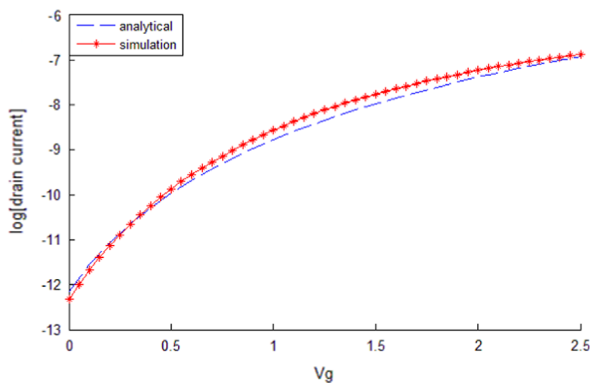

Fig. 10. Drain current versus V_{GS} for W=4 nm, with V_{DS}=0.5 V.

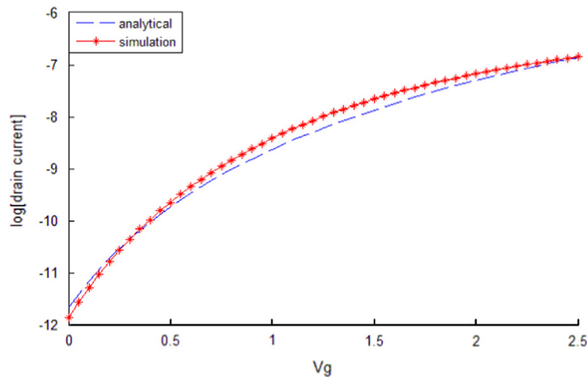

Fig. 11. Drain current versus V_{GS} for W=5 nm, with V_{DS}=0.5 V.

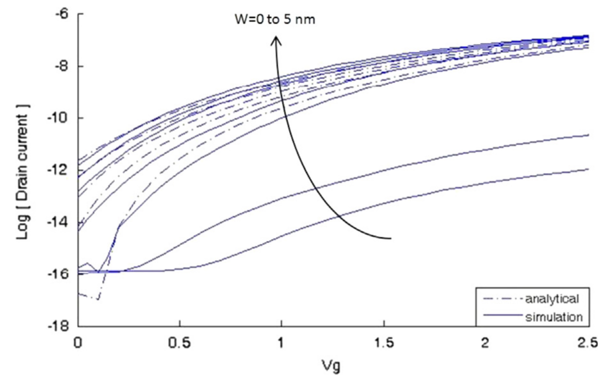

Fig. 12. Drain current versus V_{GS} for W=0, 0.5, 1, 2, 3, 4, and 5 nm, with V_{DS}=0.5 V.

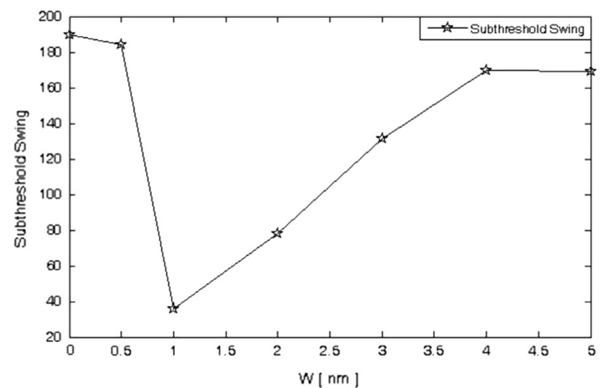

Fig. 13. Subthreshold swing for the different widths of n$^+$ region (W=0, 0.5, 1, 2, 3, 4, and 5).

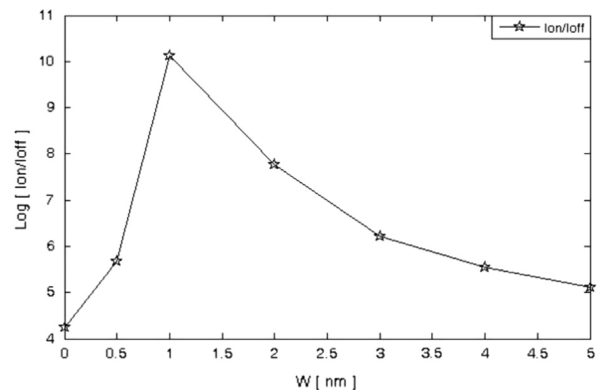

Fig. 14. I_{on}/I_{off} ratio for the different widths of n$^+$ region (W=0, 0.5, 1, 2, 3, 4, and 5).

region (W=0) I_{on} is extremely reduced which results in reduced I_{on}/I_{off} ratio. As it is seen in Fig. 10 when W is increased up to W=1 nm I_{off} remains constant, whereas I_{on} increases. Moreover when $W>1$ nm I_{on} is constant, while I_{off} increases, therefore optimum condition is W=1 nm.

Subthreshold swing and I_{on}/I_{off} ratio are depicted in Figs. 13 and 14, respectively. From these figures, it can be concluded that for W=1 nm the optimized l_{path} is obtained, in the sense of subthreshold swing and I_{on}/I_{off} ratio. Finally, when W=1 nm, subthreshold swing of 36 mV/dec and I_{on}/I_{off} ratio of 10^{10} are achieved.

5. Conclusions

This paper proposes an analytical model for the potential distribution and the drain current of p-n-i-n TFET. It is shown that with a W=1 nm δ-doped region, subthreshold swing as low as 36 mV/dec is achieved. This is well below 60 mV/dec MOSFETs physical limit. Furthermore, I_{on}/I_{off} ratio as high as 10^{10} is achieved, which is comparable

with the conventional MOSFETs. Moreover, we have derived the current distribution of a TFET by considering Kane's model for band-to-band tunneling in channel region. It is concluded that when the width of n^+ region is 1 nm, the optimized subthreshold swing and I_{on}/I_{off} ratio are obtained. Our analytical model result closely matches the simulation results from Silvaco Atlas.

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