IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Generalised single-phase *N*-level voltage-source inverter with coupled inductors

ISSN 1755-4535
Received on 2nd September 2014
Revised on 18th April 2015
Accepted on 21st May 2015
doi: 10.1049/iet-pel.2014.0674
www.ietdl.org

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Abstract: A generalised single-phase *N*-level voltage-source inverter is presented in this study. The number of output voltage levels is increased by using split-wound coupled inductors instead of several DC voltage sources and split and/or clamp capacitors of the conventional multilevel converters. As an example, the operation of the nine-level inverter is analysed and a proper switching strategy is proposed. With this modulation strategy, no DC components exist in the inductor voltages and currents, which is very helpful for minimisation of the inductors. Voltage steps are only one-quarter of the DC voltage source, leading to much reduced d*v*/d*t*. Moreover, this inverter compared with other inverters with the same number of voltage levels requires fewer switches and passive components. This study uses simulation and experimental results to illustrate the operation of the proposed inverter.

1 Introduction

Nowadays, multilevel inverter topologies have attracted a lot of attentions in the field of energy control for high-power and medium-voltage applications [1–3].

The advantages of multilevel inverters include [4]:

- reduced voltage stresses on switching devices and load, which enhances the lifetime of switches and reduces the electromagnetic interference;
- higher quality of the output waveforms; and
- increased effective switching frequency, which reduces the size and cost of the output filter.

The most common multilevel inverter topologies are the cascaded H-bridge, diode-clamped and flying capacitor structures [1, 4, 5]. The cascaded inverter is an appropriate solution where several DC sources are available. The two other inverters use a number of extra capacitors in their structure in order to create voltage steps. The main problem with these structures is the voltage balancing between these capacitors. In recent years, other alternative approaches to the conventional topologies are also proposed in the literature [6–41], among which the multilevel inverters with coupled inductors are the most recent [26–34]. These topologies utilise the coupled inductors to improve the output quality of the inverter by increasing the effective switching frequency and the number of output voltage levels, while eliminating the need for several DC sources and/or several bulky capacitors. A half-bridge three-level inverter has been proposed in [27], which consists of two power switches, two diodes and two (one pair of) coupled inductors, while split DC-link capacitors are still needed. The need for split DC-link capacitors can be avoided by doubling the number of power semiconductors and coupled inductors. The augmented topology can generate a five-output waveform [28, 29]. The main advantage of proposed topologies in [27–29] is the elimination of dead-time, since inductors are placed in series with switches of converter legs.

More recently, Floricau *et al.* [31], Floricau *et al.* [32] and Floricau [33] presented five-level hybrid inverters, which combine the coupled inductors with the conventional multilevel topologies. Owing to the presence of split capacitors, the risk of unbalanced voltages exists if the inverters are not properly modulated. Presented topology in [26] with only one DC source and no split capacitors may be the most desirable topology with coupled inductors, which can provide five-level waveforms with only six power switches and two (one pair of) coupled inductors. However, a common problem with all multilevel inverters with coupled inductors is that the number of achievable voltage levels is limited to five.

In this paper, a multilevel voltage-source inverter with coupled inductors is proposed, which can be easily extended to any number of voltage levels, while the number of switches does not increase considerably. In addition, it requires only one DC source and does not have any split and/or clamp capacitors in its topology, which eliminates the problem of capacitor voltage balancing with the conventional topologies. Moreover, a switching strategy is proposed which lets two semiconductor switches work at reference voltage frequency, while providing low-harmonic content outputs. As a result, the switching losses, as well as, the electromagnetic interference (EMI) emissions are low. With this modulation method, no DC components exist in the inductor currents, which is necessary to minimise the size of inductors. Additionally, this inverter compared with other inverters with the same number of voltage levels, requires fewer switches and passive components. In the following sections, the converter and its principles of operation are explained in detail. Afterwards, design expressions and considerations are presented. Finally, simulation and experimental results are presented to support the theoretical achievements.

2 Proposed single-phase *N*-level inverter

Fig. 1 shows the power circuit of the proposed single-phase *N*-level inverter. If in the proposed inverter circuit, a pair of coupled inductors is used, the maximum number of voltage levels is five and if two pairs of coupled inductors are used, it can generate nine levels. In general, if the total number of coupled inductor pairs is k, then the maximum number of possible voltage levels is $(2^{k+1}+1)$.

In this paper, as a matter of convenience and without loss of generality, the single-phase nine-level inverter, presented in Fig. 2, is attended. In this figure, E is the DC voltage. L_1 and L_2 are coupled inductors and the mutual inductance between these two inductors is M_1; this pair of coupled inductors is placed between nodes 2 and 3. L_3 and L_4 are other two coupled inductors placed between nodes 4 and 5. Care must be taken that the two pairs L_1L_2 and L_3L_4 are not coupled together, at all. As depicted, the

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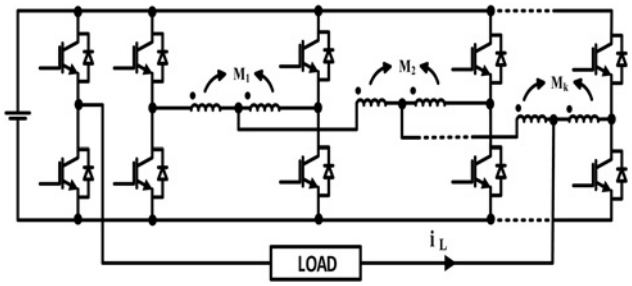

Fig. 1 *Proposed single-phase N-level inverter with coupled inductors*

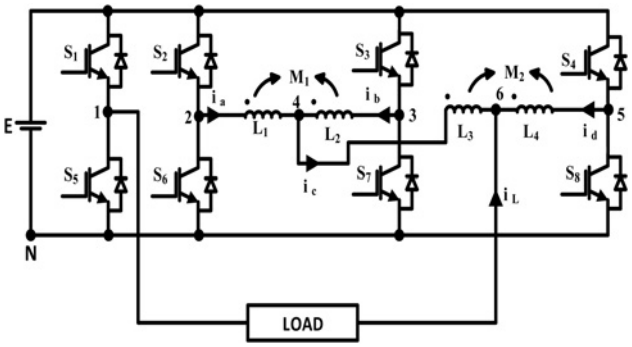

Fig. 2 *Proposed single-phase nine-level inverter with coupled inductors*

output terminals of this inverter are nodes 1 and 6. Apparently, the proposed topology can be simply implemented by adding pairs of coupled inductors between the legs of conventional voltage-source inverters.

3 Role of coupled inductors

To reveal the principle behind the proposed multilevel inverter, in the first step, the role of the coupled inductors must be analysed. Two coupled inductors with the same number of turns are considered, as shown in Fig. 3, where the self, leakage and mutual inductance of these two inductors are L, L_σ and M, respectively.

Since the number of turns of both inductors is equal, the self and leakage inductances of these two inductors are the same. With writing the voltage equations of coupled inductors, the following equations are given [26]

$$V_{an} = V_a - V_n = L\frac{\mathrm{d}i_a}{\mathrm{d}t} - M\frac{\mathrm{d}i_b}{\mathrm{d}t} = (L_\sigma + M)\frac{\mathrm{d}i_a}{\mathrm{d}t} - M\frac{\mathrm{d}i_b}{\mathrm{d}t} \quad (1)$$

$$V_{bn} = V_b - V_n = L\frac{\mathrm{d}i_b}{\mathrm{d}t} - M\frac{\mathrm{d}i_a}{\mathrm{d}t} = (L_\sigma + M)\frac{\mathrm{d}i_b}{\mathrm{d}t} - M\frac{\mathrm{d}i_a}{\mathrm{d}t}. \quad (2)$$

On the other hand, according to Kirchhoff's current law, one can obtain

$$i_a + i_b - i_\mathrm{L} = 0\ . \quad (3)$$

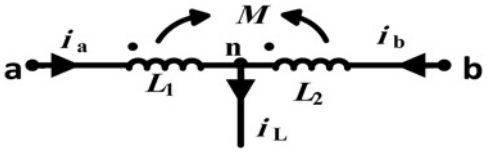

Fig. 3 *Pair of coupled inductors*

Now, from (1) to (3), the following equation can be concluded

$$V_{an} + V_{bn} = V_a + V_b - 2V_n = L_\sigma\frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t}. \quad (4)$$

which can be rearranged for the voltage of node n

$$V_n = \frac{V_a + V_b - L_\sigma(\mathrm{d}i_\mathrm{L}/\mathrm{d}t)}{2}. \quad (5)$$

Indeed, the leakage inductance is very small and its effect can be safely neglected in most cases. With this assumption, (5) simplifies to

$$V_n = \frac{V_a + V_b}{2}. \quad (6)$$

This result shows that the common node voltage of coupled inductors is the average of two voltages of none of the common nodes. According to (6), the voltages of nodes 4 and 6 of the proposed inverter of Fig. 2 are

$$V_{4N} = \frac{V_{2N} + V_{3N}}{2} \quad (7)$$

$$V_{6N} = \frac{V_{4N} + V_{5N}}{2}. \quad (8)$$

As a result, the output voltage of the proposed inverter will be obtained using the following equation

$$V_{16} = V_{1N} - V_{6N} = V_{1N} - \frac{V_{2N} + V_{3N} + 2V_{5N}}{4}. \quad (9)$$

Hereafter, the switches in one leg are assumed to switch complementarily. The numbers '1' and '0' will be used to denote the ON and OFF states of power switches, respectively. For Fig. 2 and according to (9), all switching states together with the relevant voltage of coupled inductors and the output voltage can be obtained as summarised in Table 1.

According to Table 1, this inverter is able to produce nine distinct levels in the output voltage waveform. It is also clear from Table 1 that the switch S_1 is always ON when $V_{16} \geq 0$ and is kept OFF when $V_{16} \leq 0$. As a result, S_1 and S_5 are switched at the fundamental frequency of the reference signal. Therefore the switching losses of S_1 and S_5 are very low in the proposed inverter.

Table 1 Switching states and output voltage and inductors voltages of the proposed inverter

S_1	S_2	S_3	S_4	V_{4N}	V_{6N}	V_{23}	V_{45}	V_{16}
0	0	0	0	0	0	0	0	0
0	0	0	1	0	$E/2$	0	$-E$	$-E/2$
0	0	1	0	$E/2$	$E/4$	$-E$	$E/2$	$-E/4$
0	0	1	1	$E/2$	$3E/4$	$-E$	$-E/2$	$-3E/4$
0	1	0	0	$E/2$	$E/4$	E	$E/2$	$-E/4$
0	1	0	1	$E/2$	$3E/4$	E	$-E/2$	$-3E/4$
0	1	1	0	E	$E/2$	0	E	$-E/2$
0	1	1	1	E	E	0	0	$-E$
1	0	0	0	0	0	0	0	E
1	0	0	1	0	$E/2$	0	$-E$	$E/2$
1	0	1	0	$E/2$	$E/4$	$-E$	$E/2$	$3E/4$
1	0	1	1	$E/2$	$3E/4$	$-E$	$-E/2$	$E/4$
1	1	0	0	$E/2$	$E/4$	E	$E/2$	$3E/4$
1	1	0	1	$E/2$	$3E/4$	E	$-E/2$	$E/4$
1	1	1	0	E	$E/2$	0	E	$E/2$
1	1	1	1	E	E	0	0	0

IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2257–2264
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Table 2 Nine-level output voltage ranges

Case	Output voltage range	Case	Output voltage range
1	$3E/4 < V_{16ref} < E$	5	$-E/4 < V_{16ref} < 0$
2	$E/2 < V_{16ref} < 3E/4$	6	$-E/2 < V_{16ref} < -E/4$
3	$E/4 < V_{16ref} < E/2$	7	$-3E/4 < V_{16ref} < -E/2$
4	$0 < V_{16ref} < E/4$	8	$-E < V_{16ref} < -3E/4$

4 Proposed switching strategy

However, there are many more possible switching states for the proposed inverter with coupled inductors, a simple switching of the upper and lower switches is proposed here to produce nine-level output voltage waveform with balanced inductor currents and no DC offset. However, not considered here, but it is possible to include more criteria such as low-order harmonic attenuation in the output waveforms. According to the previous section, the control of switches S_1 and S_5 is directly obtained from the sign of the reference voltage V_{16ref}; when $V_{16ref} > 0$, the switch S_1 is ON (S_5 is OFF) and vice versa, which is very easy to implement. However, the switching states of S_2, S_3 and S_4 cannot be selected without a careful study. To decide the switching states of (S_2, S_3, S_4), bearing in mind that the output voltage has nine levels, eight distinct output voltage ranges can be defined for this inverter. These ranges are shown in Table 2.

It is evident that in each case, numbered from 1 to 8 and within every switching period, the output voltage must alternate between two upper and lower limits of that range. For example, in case 1, V_{16} must be either $+E$ or $+3E/4$. According to Table 1, the switching states of (S_2, S_3, S_4) can be (0, 0, 0) $\leftrightarrow$ (0, 1, 0) or (0, 0, 0) $\leftrightarrow$ (1, 0, 0), where the note '$x \leftrightarrow y$' means alternating between x and y.

Similarly, the switching states for all cases are derived and presented in Table 3.

Evidently, for each case, two or four different switching transitions are possible that offers some kind of flexibility to choose between them. As a result, a great many combinations of that switching states can be found that can generate the nine-level output voltage V_{16}; however, for some of these combinations, the voltages of inductor windings (V_{23} and V_{45}) may contain DC components. These DC components cause the currents of coupled inductors increase to quite a large value, which is harmful to safe operation of this inverter. Therefore an important issue that must be considered in dealing with the coupled inductors is that the average voltages of the inductor windings (V_{23} and V_{45}) must be zero during an AC period to avoid the DC voltage drop and consequently saturation of the coupled inductors or significant unbalance of the inductor winding currents. Otherwise, the inverter does not have a safe performance and the converter may have the risk of overcurrent [26, 31]. Additionally, in order to minimise the size and weight of the coupled inductors, the currents in the coupled inductors should increase and decrease in opposite directions during consecutive switching states within every case, where possible. On the basis of these analyses to minimise the inductor currents, appropriate switching states are presented in Table 4, where both switching states must be used during a sampling period (T_s).

Table 3 Possible switching states for different cases

V_{16}	Case	S_1	(S_2, S_3, S_4)	V_{23}	V_{45}
$E \leftrightarrow 3E/4$	1	1	(0,0,0) $\leftrightarrow$ (0,1,0)	$0 \leftrightarrow -E$	$0 \leftrightarrow E/2$
		1	(0,0,0) $\leftrightarrow$ (1,0,0)	$0 \leftrightarrow E$	$0 \leftrightarrow E/2$
$3E/4 \leftrightarrow E/2$	2	1	(0,1,0) $\leftrightarrow$ (0,0,1)	$-E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
		1	(0,1,0) $\leftrightarrow$ (1,1,0)	$-E \leftrightarrow 0$	$E/2 \leftrightarrow E$
		1	(1,0,0) $\leftrightarrow$ (0,0,1)	$E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
		1	(1,0,0) $\leftrightarrow$ (1,1,0)	$E \leftrightarrow 0$	$E/2 \leftrightarrow E$
$E/2 \leftrightarrow E/4$	3	1	(0,0,1) $\leftrightarrow$ (0,1,1)	$0 \leftrightarrow -E$	$-E \leftrightarrow -E/2$
		1	(0,0,1) $\leftrightarrow$ (1,0,1)	$0 \leftrightarrow E$	$-E \leftrightarrow -E/2$
		1	(1,1,0) $\leftrightarrow$ (0,1,1)	$0 \leftrightarrow -E$	$E \leftrightarrow -E/2$
		1	(1,1,0) $\leftrightarrow$ (1,0,1)	$0 \leftrightarrow E$	$E \leftrightarrow -E/2$
$E/4 \leftrightarrow 0$	4	1	(0,1,1) $\leftrightarrow$ (1,1,1)	$-E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$
		1	(1,0,1) $\leftrightarrow$ (1,1,1)	$E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$
$0 \leftrightarrow -E/4$	5	0	(0,0,0) $\leftrightarrow$ (0,1,0)	$0 \leftrightarrow -E$	$0 \leftrightarrow E/2$
		0	(0,0,0) $\leftrightarrow$ (1,0,0)	$0 \leftrightarrow E$	$0 \leftrightarrow E/2$
$-E/4 \leftrightarrow -E/2$	6	0	(0,1,0) $\leftrightarrow$ (0,0,1)	$-E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
		0	(0,1,0) $\leftrightarrow$ (1,1,0)	$-E \leftrightarrow 0$	$E/2 \leftrightarrow E$
		0	(1,0,0) $\leftrightarrow$ (0,0,1)	$E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
		0	(1,0,0) $\leftrightarrow$ (1,1,0)	$E \leftrightarrow 0$	$E/2 \leftrightarrow E$
$-E/2 \leftrightarrow -3E/4$	7	0	(0,0,1) $\leftrightarrow$ (0,1,1)	$0 \leftrightarrow -E$	$-E \leftrightarrow -E/2$
		0	(0,0,1) $\leftrightarrow$ (1,0,1)	$0 \leftrightarrow E$	$-E \leftrightarrow -E/2$
		0	(1,1,0) $\leftrightarrow$ (0,1,1)	$0 \leftrightarrow -E$	$E \leftrightarrow -E/2$
		0	(1,1,0) $\leftrightarrow$ (1,0,1)	$0 \leftrightarrow E$	$E \leftrightarrow -E/2$
$-3E/4 \leftrightarrow -E$	8	0	(0,1,1) $\leftrightarrow$ (1,1,1)	$-E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$
		0	(1,0,1) $\leftrightarrow$ (1,1,1)	$E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$

Table 4 Appropriate switching states for different cases

Case	S_1	(S_2, S_3, S_4)	V_{23}	V_{45}
1	1	(0,0,0) $\leftrightarrow$ (0,1,0)	$0 \leftrightarrow -E$	$0 \leftrightarrow E/2$
	1	(0,0,0) $\leftrightarrow$ (1,0,0)	$0 \leftrightarrow E$	$0 \leftrightarrow E/2$
2	1	(0,1,0) $\leftrightarrow$ (0,0,1)	$-E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
	1	(1,0,0) $\leftrightarrow$ (0,0,1)	$E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
3	1	(1,1,0) $\leftrightarrow$ (0,1,1)	$0 \leftrightarrow -E$	$E \leftrightarrow -E/2$
	1	(1,1,0) $\leftrightarrow$ (1,0,1)	$0 \leftrightarrow E$	$E \leftrightarrow -E/2$
4	1	(0,1,1) $\leftrightarrow$ (1,1,1)	$-E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$
	1	(1,0,1) $\leftrightarrow$ (1,1,1)	$E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$
5	0	(0,0,0) $\leftrightarrow$ (0,1,0)	$0 \leftrightarrow -E$	$0 \leftrightarrow E/2$
	0	(0,0,0) $\leftrightarrow$ (1,0,0)	$0 \leftrightarrow E$	$0 \leftrightarrow E/2$
6	0	(0,1,0) $\leftrightarrow$ (0,0,1)	$-E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
	0	(1,0,0) $\leftrightarrow$ (0,0,1)	$E \leftrightarrow 0$	$E/2 \leftrightarrow -E$
7	0	(1,1,0) $\leftrightarrow$ (0,1,1)	$0 \leftrightarrow -E$	$E \leftrightarrow -E/2$
	0	(1,1,0) $\leftrightarrow$ (1,0,1)	$0 \leftrightarrow E$	$E \leftrightarrow -E/2$
8	0	(0,1,1) $\leftrightarrow$ (1,1,1)	$-E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$
	0	(1,0,1) $\leftrightarrow$ (1,1,1)	$E \leftrightarrow 0$	$-E/2 \leftrightarrow 0$

In this case, the voltage V_{23} changes polarity in every T_s. Moreover, the dwell times for switching conditions that generate $+E$ and $-E$ to V_{23} must be equal in all cases. For example, the dwell times for (0,1,0) and (1,0,0) in cases 1 and 5 must be equal. Additionally, the dwell times for switching conditions that generate $+E/2$ ($-E/2$) to V_{45} must be twice the dwell times for switching conditions that generate $-E$ ($+E$) to V_{45} in cases 2, 3, 6 and 7. Otherwise, fundamental or low-order harmonics will appear in the inductor currents under no-load and it will also increase the inductor currents when the inverter is loaded. It is clear from Table 4 that only the switching state of one power switch changes and two other switches have constant states in cases 1, 4, 5 and 8, but in cases 2, 3, 6 and 7 the switching states of two switches change. In addition, all cases have three switching conditions. For example, these three switching conditions are (0,1,0), (0,0,1) and (1,0,0) for cases 2 and 6. In this modulation scheme, the consecutive switching conditions are called H_1, H_2 and H_3. The proposed switching scheme is based on sampling the reference voltage. In this method, after sampling the reference voltage and identifying the voltage range (cases 1–8), the suitable switching is applied to the converter. Assuming that the sampling period T_s is sufficiently small, the reference voltage can be considered constant during T_s. Now, the next step is to decide the proper switching sequence. For this modulation strategy, two switching sequences are possible, as illustrated in Fig. 4.

Both switching sequences, 'A' and 'B', are formed by using three switching conditions: H_1, H_2 and H_3. As illustrated, x, y and z are allocated dwell times for H_1, H_2 and H_3 of a given case in every sampling period, respectively. The switching cycle A (B) is for cases 1, 4, 5 and 8 (2, 3, 6 and 7). To summarise, in order to minimise the inductor currents, the following two requirements should be considered in determining the dwell times:

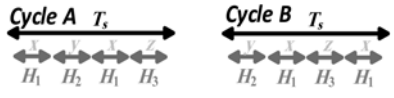

Fig. 4 *Four-segment switching sequences for the proposed modulation strategy*

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Table 5 Four-segment switching sequence

Case	Switching segments and dwell times			
	1	2	3	4
1	(0,0,0) $T_s/6$	(0,1,0) $T_s/3$	(0,0,0) $T_s/6$	(1,0,0) $T_s/3$
2	(0,1,0) $T_s/3$	(0,0,1) $T_s/6$	(1,0,0) $T_s/3$	(0,0,1) $T_s/6$
3	(1,0,1) $T_s/3$	(1,1,0) $T_s/6$	(0,1,1) $T_s/3$	(1,1,0) $T_s/6$
4	(1,1,1) $T_s/6$	(0,1,1) $T_s/3$	(1,1,1) $T_s/6$	(1,0,1) $T_s/3$
5	(0,0,0) $T_s/6$	(0,1,0) $T_s/3$	(0,0,0) $T_s/6$	(1,0,0) $T_s/3$
6	(0,1,0) $T_s/3$	(0,0,1) $T_s/6$	(1,0,0) $T_s/3$	(0,0,1) $T_s/6$
7	(1,0,1) $T_s/3$	(1,1,0) $T_s/6$	(0,1,1) $T_s/3$	(1,1,0) $T_s/6$
8	(1,1,1) $T_s/6$	(0,1,1) $T_s/3$	(1,1,1) $T_s/6$	(1,0,1) $T_s/3$

- during any sampling period, the dwell times for switching conditions that generate $+E$ and $-E$ to V_{23} must be equal and
- the dwell times for switching conditions that generate $+E/2$ ($-E/2$) to V_{45} must be twice the dwell times for conditions that generate $-E$ ($+E$) to V_{45} in cases 2, 3, 6 and 7.

To this end, in both switching cycles, 'A' and 'B', the dwell times for H_2, H_3 (y and z) are the same and the dwell time y is twice x. In addition, x is equal to $T_s/6$.

Table 5 gives the four-segment switching sequences for $V_{16\text{ref}}$ for all eight cases. In Table 5, segments 1 and 3 are H_1 and segments 2 and 4 are H_2 and H_3, respectively, in cases 1, 4, 5 and 8, whereas segments 2 and 4 are H_1 and segments 1 and 3 are H_2 and H_3, respectively, in cases 2, 3, 6 and 7.

The power devices S_1, S_5 are rated for the load current (i_L) and they are controlled at low frequency; as a result, these switches have only conduction losses and the switching losses are neglected, because the control of power devices S_1 and S_5 is done at reference voltage frequency. The power devices S_2, S_3, S_6 and S_7 are rated for one-quarter of the load current ($i_L/4$), whereas switches S_4 and S_8 carry half of the load current and all these semiconductor switches are controlled at high frequency. Therefore the high-switching frequency devices have both conduction and switching losses. The junction temperature of each switch is a direct consequence of conduction and switching losses. As a result, a better temperature distribution is achieved.

5 Design of the coupled inductors

According to Fig. 2, the current of the inductors will be obtained using the following equations [26, 27]

$$i_c = -0.5i_L + i_{\text{ripple1}} \tag{10}$$

$$i_d = -0.5i_L - i_{\text{ripple1}} \tag{11}$$

$$\begin{aligned} i_a &= 0.5i_c + i_{\text{ripple2}} = 0.5\left(-0.5i_L + i_{\text{ripple1}}\right) + i_{\text{ripple2}} \\ &= -0.25i_L + 0.5i_{\text{ripple1}} + i_{\text{ripple2}} \end{aligned} \tag{12}$$

$$\begin{aligned} i_b &= 0.5i_c - i_{\text{ripple2}} = 0.5\left(-0.5i_L + i_{\text{ripple1}}\right) - i_{\text{ripple2}} \\ &= -0.25i_L + 0.5i_{\text{ripple1}} - i_{\text{ripple2}}. \end{aligned} \tag{13}$$

where i_{ripple1} and i_{ripple2} are

$$i_{\text{ripple1}} = \frac{1}{2M_2}\int V_{45}\,\mathrm{d}t \tag{14}$$

$$i_{\text{ripple2}} = \frac{1}{2M_1}\int V_{23}\,\mathrm{d}t \tag{15}$$

As a result, inductors L_3 and L_4 and switches S_4 and S_8 carry about half of the load current if i_{ripple1} is low. Moreover, L_1, L_2, S_2, S_3, S_6 and S_7 carry one-quarter of the load current. Thus, the presented inverter is suitable for low–medium-power applications (such as

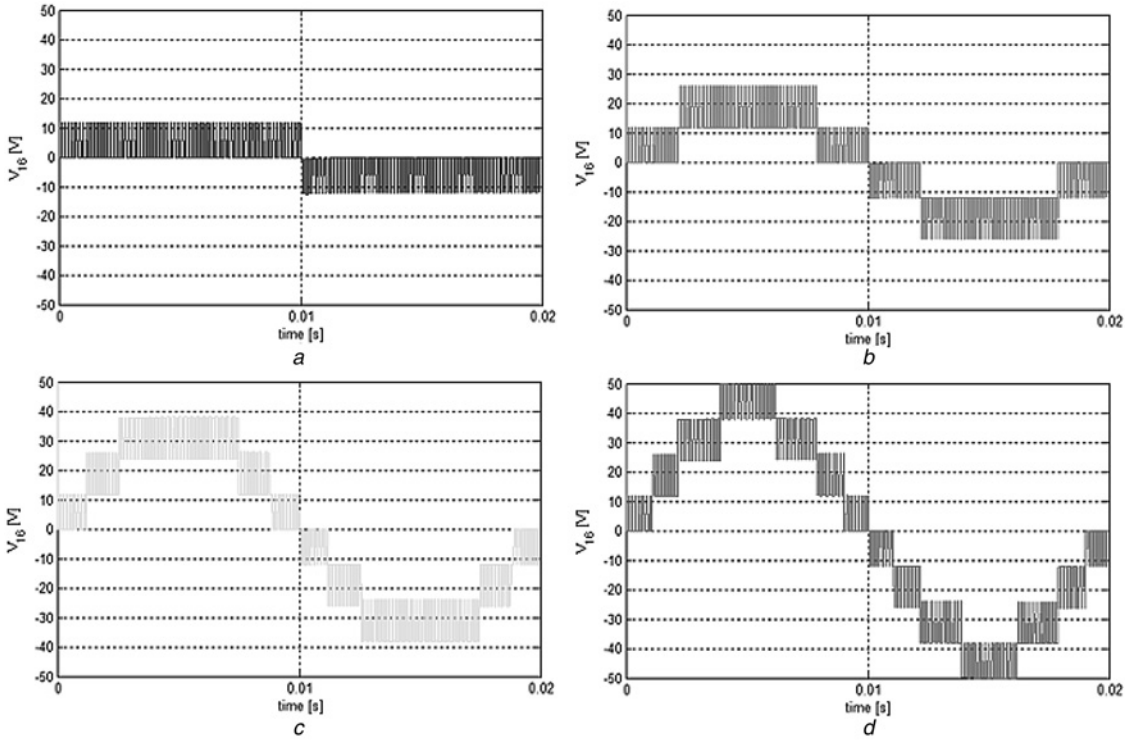

Fig. 5 *Simulation results of the output voltage when*

a $M_a = 0.2$
b $M_a = 0.4$
c $M_a = 0.7$
d $M_a = 0.8$

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motor drives), to increase the output current, while the switched current through the high-frequency power devices is reduced to 50% of load current and less.

Since, the maximum voltage of the inductor windings is E, the maximum ripple current in the coupled inductors can be approximated as

$$i_{\text{ripple1(max)}} = \frac{1}{2M_2}\int_0^{T_s} E\,\mathrm{d}t = \frac{ET_s}{2M_2} \tag{16}$$

$$i_{\text{ripple2(max)}} = \frac{1}{2M_1}\int_0^{T_s} E\,\mathrm{d}t = \frac{ET_s}{2M_1}. \tag{17}$$

Therefore, for tolerable ripple currents $i_{\text{ripple1(max)}}$ and $i_{\text{ripple2(max)}}$, the inductances $L_1 = M_1$ and $L_2 = M_2$ are

$$M_1 \geq \frac{T_s E}{2i_{\text{ripple2(max)}}} \tag{18}$$

$$M_2 \geq \frac{T_s E}{2i_{\text{ripple1(max)}}}. \tag{19}$$

The energy storages required in inductors are then calculated as

$$j_1 = \frac{1}{2}2M_1 i_a^2 \cong M_1\left(\frac{i_L}{4}\right)^2 = \frac{M_1 i_L^2}{16} \tag{20}$$

$$j_2 = \frac{1}{2}2M_2 i_c^2 \cong M_2\left(\frac{i_L}{2}\right)^2 = \frac{M_2 i_L^2}{4}. \tag{21}$$

Now, based on the core characteristics and (20) and (21), one can simply select the appropriate core size. Roughly, the core size of inductor M_2 is about twice the core size of inductor M_1. The following formula gives the number of turns required for inductance (nH), in which A_L is the core permeance, given in nH/('turns')

$$N = \left(\frac{L\,(nH)}{A_L}\right)^{0.5}. \tag{22}$$

6 Simulation results

To confirm the validity of the steady-state performance of the proposed inverter, the nine-level converter with a RL load ($R = 4.5$ Ω in series with $L = 2$ mH) is simulated. The DC-link voltage and the sampling frequency are 50 V and 5 kHz, respectively, for both simulation and experimental tests. Moreover, mutual inductances M_1 and M_2 are 600 µH. In this inverter, if the modulation index (M_a) is in the ranges of 0–0.25, 0.25–0.5, 0.5–0.75 and 0.75–1, the output voltages have 3, 5, 7 and 9 levels, respectively. The modulation index is defined in (23)

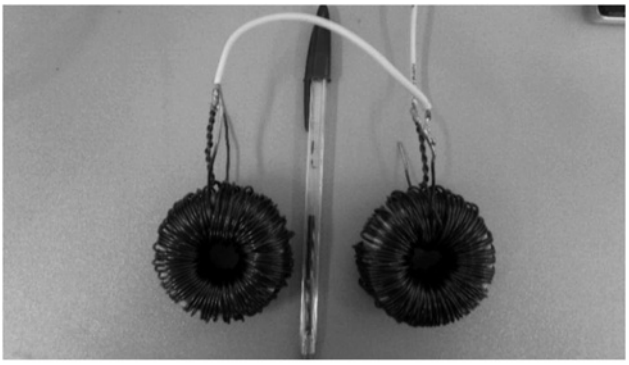
$$M_a = \frac{V_{16\text{ref, peak}}}{V_{\text{dc}}} \tag{23}$$

Fig. 5 shows simulation results for the output voltage (V_{16}) when the modulation indexes are 0.2, 0.4, 0.7 and 0.8. It is clear from Figs. 5*a* to *d* that the output voltages have 3, 5, 7 and 9 levels, respectively. Moreover, in all these simulations, the height of output voltage steps is one-quarter of the DC-link voltage. Compared with the H-bridge inverter, this is a substantial reduction of the dv/dt in the inverter output voltage.

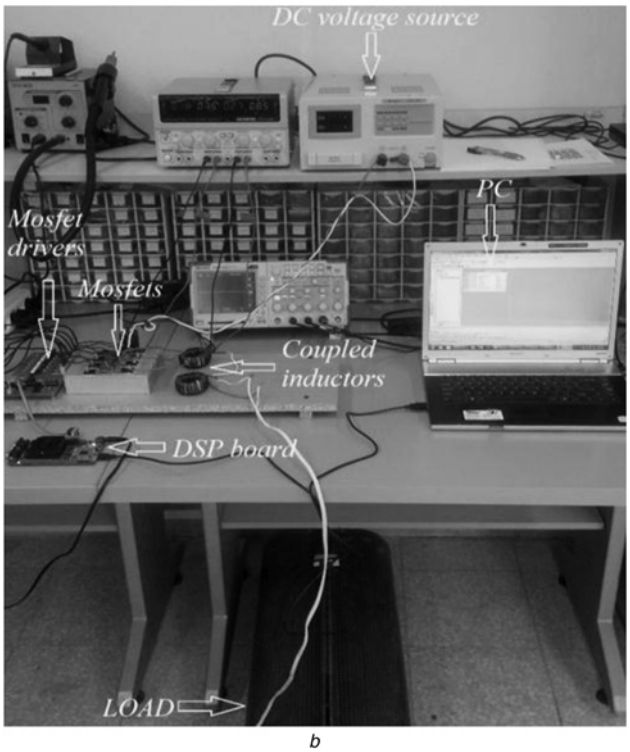
7 Experimental results

The proposed inverter together with the proposed switching strategy has also been experimentally tested. In these experiments, eight IRFP460A metal–oxide semiconductor field-effect transistors are used as the power switches $S_1 - S_8$ what are rated at 500 V and 20 A. The control signals are generated using the TMS320F28335 digital signal processor (DSP). The dead-time for all legs has been set to 1 µs. The photographs of coupled inductors and the experimental setup are shown in Fig. 6.

Figs. 7–11 show experimental results of the proposed inverter under an inductive load ($R = 4.5$ Ω in series with $L = 2$ mH) when the modulation index is 0.8. Fig. 7 shows the output voltage (V_{16}) and the load current (i_L). It is clear that the output voltage is of nine-level when the modulation index is 0.8. Fig. 8 shows the harmonic spectrum of output voltage and load current. It is clear that the output voltage does not have any DC component and the total harmonic distortion of the output voltage and current are 14.8 and 10.9%, respectively. It is clear that the harmonics of the current waveform are lower than the voltage waveform.



a



b

Fig. 6 *Photograph of*

a Coupled inductors
b Experimental test rig

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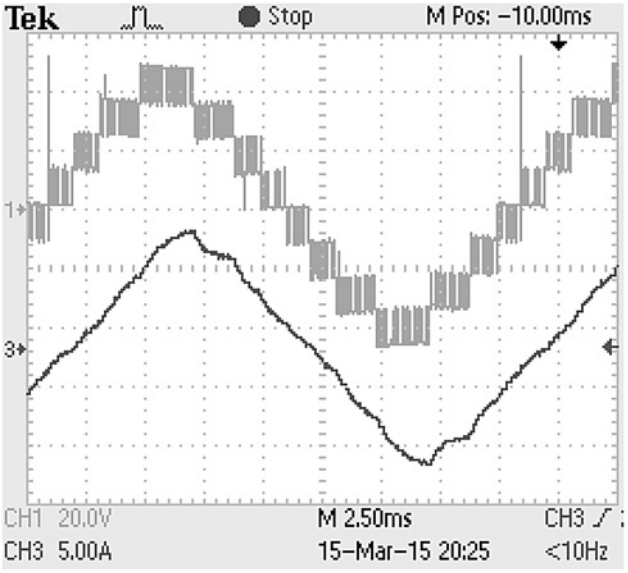

Fig. 7 *Output voltage and load current under RL load when M_a is 0.8*

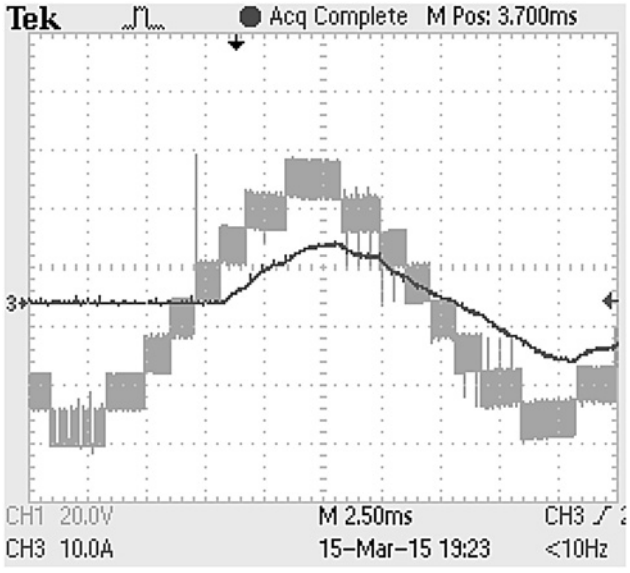

Fig. 10 *Output voltage and load current when the load is changed from no-load to RL load*

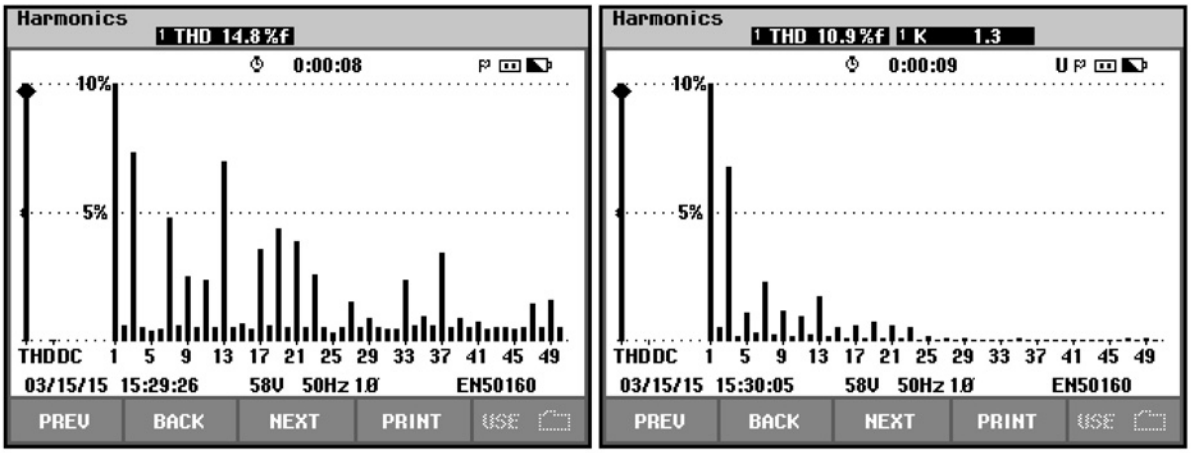

Fig. 8 *Harmonic spectrum of the output waveforms*

a V_{16}
b i_L

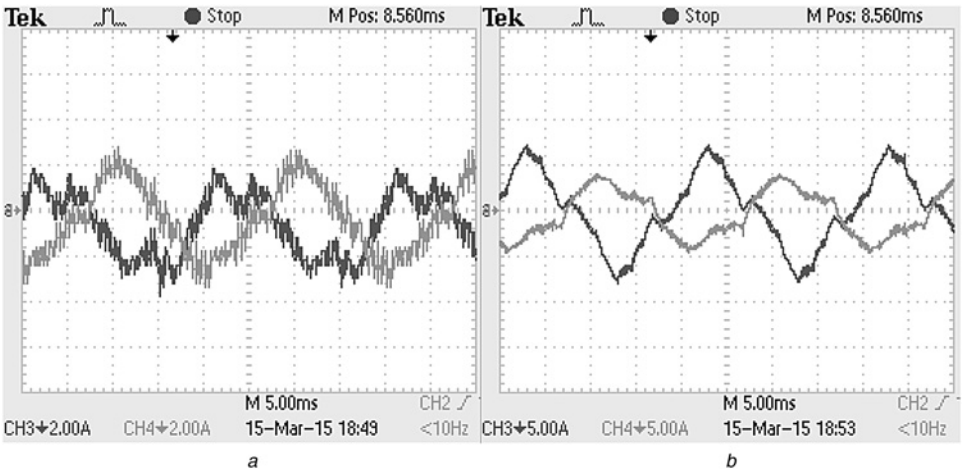

Fig. 9 *Experimental results under RL load when $M_a = 0.8$*

a i_a and i_b (2 A/div)
b i_c and i_d (5 A/div)

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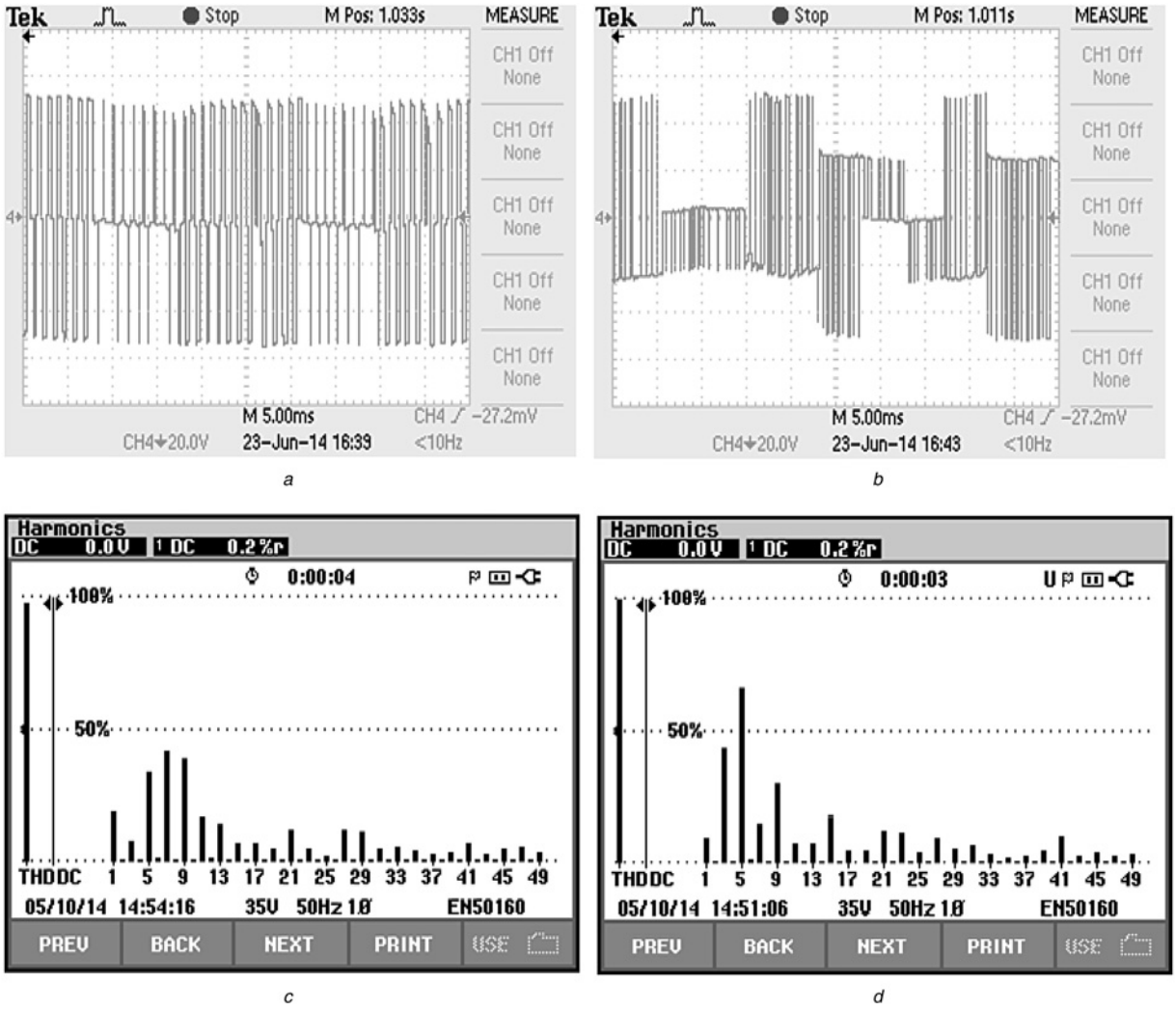

Fig. 11 *Experimental results of inductor voltages*

a V_{23}
b V_{45}
c Harmonic spectrum of V_{23}
d Harmonic spectrum of V_{45}

Fig. 9 shows experimental results for the currents of inductor windings under RL load condition with the modulation index of 0.8. It is clear from Fig. 9 that the currents in the two coupled inductors have no DC components. Moreover, the peak of i_a and i_b is 2.5 A and the maximum value of i_c and i_d is about 5 A. Although, the peak of i_L is 10 A. When the converter is loaded, the no DC component exists in these currents, which can be seen in Fig. 9.

As a transient action, the load is suddenly changed from no-load to RL load ($R = 4.5\ \Omega$ and $L = 2$ mH). The output voltage and the load current are shown in Fig. 10. A fast and smooth current transient is obvious, also the output voltage is unaffected.

As previously mentioned, the average voltage of the inductor windings must be zero to avoid the saturation of the coupled inductors. Figs. 11*a* and *b* illustrate the voltages of the inductor windings V_{23} and V_{45}, respectively, and Figs. 11*c* and *d* show the harmonic spectra of V_{23} and V_{45}, respectively. Evidently, the voltages V_{23} and V_{45} do not have any DC component.

8 Conclusion

This paper proposed a single-phase N-level voltage-source inverter based on coupled inductors with the associated modulation strategy. This inverter can output N-level voltage with only one DC source. The low-harmonic content on the output voltage produces a major reduction concerning the volume and the cost of the output filter. The presented inverter is very suitable for low–medium-power applications. Verification results of an example nine-level inverter confirm the proper operation of the proposed topology together with the switching strategy.

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