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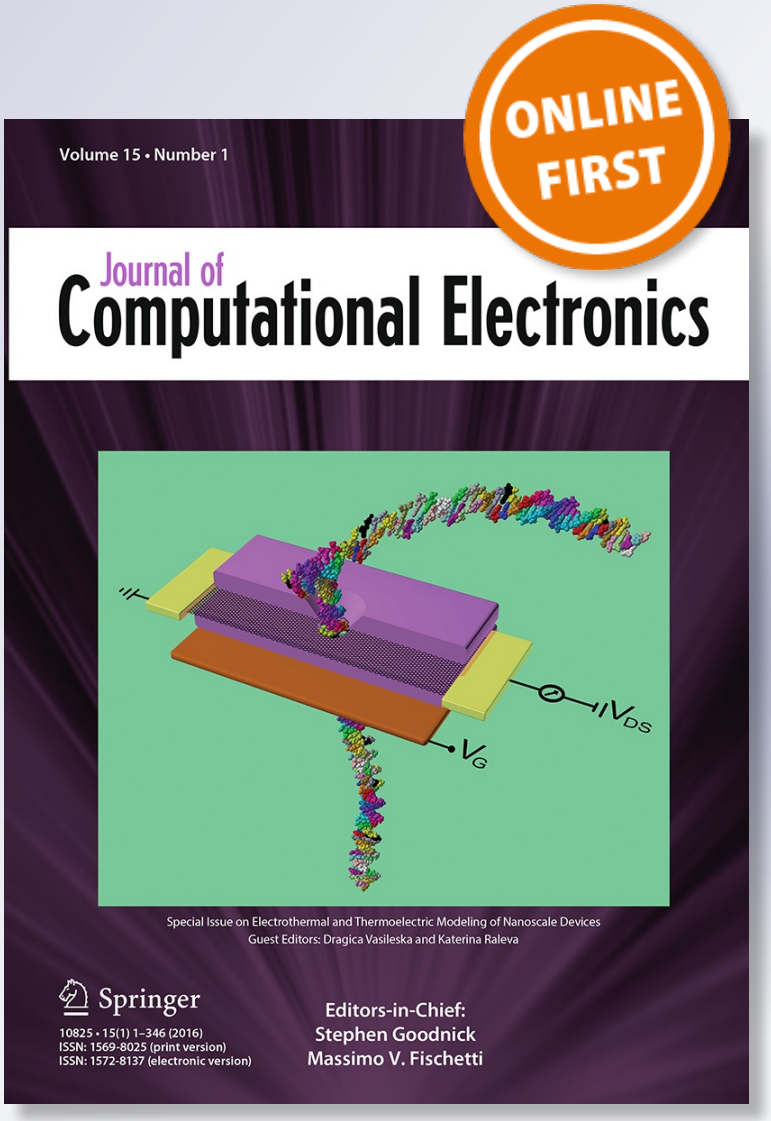

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Analytical modeling of subthreshold swing in undoped trigate SOI MOSFETs

Hamdam Ghanatian[1] · **Seyed Ebrahim Hosseini**[1]

Abstract A new analytical model for the subthreshold swing of nanoscale undoped trigate silicon-on-insulator metal–oxide–semiconductor field-effect transistors (MOSFETs) is proposed, based on the channel potential distribution and physical conduction path concept. An analytical model for the potential distribution is obtained by solving the three-dimensional (3-D) Poisson's equation, assuming a parabolic potential distribution between the lateral gates. In addition, mobile charges are considered in the model. The proposed analytical model is investigated and compared with results obtained from 3-D simulations using the ATLAS device simulator and experimental data. It is demonstrated that the analytical model predicts the subthreshold swing with good accuracy for different lengthes, thicknesses, and widths of channel.

Keywords Analytical model · Trigate SOI MOSFET · 3-D Poisson's equation · Parabolic potential distribution · Subthreshold swing · Conduction path · Mobile charges

1 Introduction

Device architectures based on silicon-on-insulator (SOI) technology, i.e., ultrathin-body SOI, double-gate (DG) and trigate (TG) SOI MOSFETs, are candidates for extension of complementary metal–oxide–semiconductor (CMOS) scaling beyond the limits set by bulk transistors [1–6]. These devices can operate in the fully depleted (FD) regime, enabling reduced short-channel effects and leakage current while retaining good scaling capability [7–13]. TG transistors are more interesting for scaling compared with DG transistors because the 3-D structure of the TG SOI MOSFET offers improved gate control over the entire channel, alleviating short-channel issues compared with DG SOI MOSFETs [14,15]. TG MOSFETs are being used by Intel because of their high I_{on}/I_{off} ratio [16]. The body of these transistors is usually undoped, because this reduces the body scattering effect, leading to increased carrier mobility and drift current [17].

To obtain an analytical solution based on the gradual channel approximation (GCA) [18] for DG transistors, the 3-D Poisson's equation can be reduced to a one-dimensional (1-D) equation because of their symmetric structure. However, due to the asymmetric structure of TG SOI MOSFETs, it is more challenging to find an analytical solution directly and further approximations are required [19–21]. In [22], to obtain an analytical model for the potential distribution along the channel of a TG MOSFET, the two-dimensional (2-D) Poisson's equation was solved separately in symmetric and asymmetric DG MOSFETs and the total potential for the TG MOSFET obtained by adding the potentials obtained for the symmetric and asymmetric DG MOSFETs based on a perimeter-weighted approximation. Using this potential, other parameters such as the subthreshold swing were calculated numerically. In that study, the 3-D Poisson's equation was not solved and mobile charges were neglected. In [23], the 3-D Poisson's equation was solved for a TG FinFET using the 1-D Poisson's equation and 3-D Laplace equation. The potential was obtained as a complex series, requiring many terms for accurate results.

In this paper, an alternative, simple analytical model for the potential distribution is investigated based on solving

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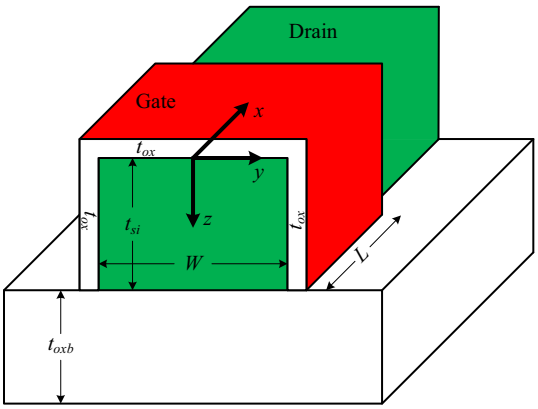

Fig. 1 Schematic cross-sectional view of a trigate SOI MOSFET. t_{ox} and t_{oxb} are the thicknesses of the gate and buried oxides, respectively

the 3-D Poisson's equation in an undoped TG SOI MOSFET in the subthreshold regime with consideration of mobile charges. The model is explicit and dependent on the drain voltage. The resulting body potential is verified by comparison with results obtained from 3-D numerical device simulations. Then, by using the physical concept of a virtual cathode, an analytical model for the subthreshold swing is obtained.

The paper is organized as follows: Section 2 provides a description of the device structure and a detailed explanation of the analytical model for the potential distribution and subthreshold swing. A comparison between analytical results and simulation data is given in Sect. 3. Finally, some conclusions are provided in Sect. 4.

2 Description of model

A schematic cross-sectional view of the TG SOI MOSFET is shown in Fig. 1. The potential distribution along the channel, $\varphi(x, y, z)$, is derived by solving the 3-D Poisson's equation:

$$\frac{\mathrm{d}^2\varphi(x,y,z)}{\mathrm{d}x^2}+\frac{\mathrm{d}^2\varphi(x,y,z)}{\mathrm{d}y^2}+\frac{\mathrm{d}^2\varphi(x,y,z)}{\mathrm{d}z^2} = \frac{qn_\mathrm{i}}{\varepsilon_\mathrm{Si}}\mathrm{e}^{\frac{q(\varphi(x,y,z)-\varphi_F(x))}{kT}} \quad 0\le z\le t_\mathrm{Si}, -W/2\le y\le W/2, 0\le x\le L, \tag{1}$$

with the following boundary conditions:

$$\varphi(0, y, z) = V_\mathrm{bi}, \tag{2}$$
$$\varphi(L, y, z) = V_\mathrm{bi} + V_\mathrm{DS}, \tag{3}$$

where kT/q is the thermal voltage, n_i is the intrinsic carrier concentration and ε_Si is the dielectric constant of silicon, V_bi is the built-in voltage, and $V_\mathrm{bi} = (kT/q)\ln(N_\mathrm{D}/n_\mathrm{i})$, in which N_D is the source/drain doping concentration. V_DS is the drain–source voltage, and φ_F is the nonequilibrium quasi-Fermi level referenced to the Fermi level in the source with the boundary conditions

$$\varphi_\mathrm{F}(0) = 0, \tag{4}$$
$$\varphi_\mathrm{F}(L) = V_\mathrm{DS}. \tag{5}$$

In the subthreshold regime, the quasi-Fermi potential in most of the channel retains the value it has at the source end [23]. Mobile charges are considered because of the undoped body; This factor is reflected in Eq. 1 by the exponential term. The potential distribution between the lateral gates is assumed to be parabolic [24,25]:

$$\varphi(x, y, z) \approx a_0(x, z) + a_1(x, z)y + a_2(x, z)y^2. \tag{6}$$

For low drain voltage, the potential distribution is parabolic in the z-direction [26]. At $y = 0$, the potential distribution is

$$\varphi(x, 0, z) = a_0(x, z) \approx C_0(x) + C_1(x)z + C_2(x)z^2. \tag{7}$$

The potential at front and lateral interfaces, $\varphi_\mathrm{f}(x)$, is

$$\varphi(x, 0, 0) = \varphi_\mathrm{f}(x) = a_0(x, 0) = C_0(x). \tag{8}$$

The potential at the back interface, $\varphi_\mathrm{sb}(x)$, is

$$\varphi(x, 0, t_\mathrm{Si}) = \varphi_\mathrm{sb}(x) = a_0(x, t_\mathrm{Si}) = C_0(x) + C_1(x)t_\mathrm{Si} + C_2(x)t_\mathrm{Si}^2. \tag{9}$$

Because of the symmetry in the y-direction,

$$\varphi\left(x, -\frac{W}{2}, z\right) = \varphi\left(x, \frac{W}{2}, z\right). \tag{10}$$

According to Eq. 10, $a_1(x, y)$ is zero, so

$$\varphi\left(x, \pm\frac{W}{2}, z\right) = \varphi_\mathrm{f}(x) = a_0(x, z) + a_2(x, z)\frac{W^2}{4}. \tag{11}$$

Using Gauss's law in the z-direction, at the channel-oxide interface, the coefficients C_1 and C_2 are obtained (see Appendix A) as

$$C_1(x) = \left.\frac{\mathrm{d}\varphi}{\mathrm{d}z}\right|_{y=0,z=0} = \frac{\varepsilon_\mathrm{ox}}{\varepsilon_\mathrm{Si}}\frac{\varphi_\mathrm{f}(x) - V'_\mathrm{gs}}{t_\mathrm{ox}}, \tag{12}$$
$$C_1(x) + 2C_2(x)t_\mathrm{Si} = \left.\frac{\mathrm{d}\varphi}{\mathrm{d}z}\right|_{y=0,z=t_\mathrm{Si}} = \frac{\varepsilon_\mathrm{ox}}{\varepsilon_\mathrm{Si}}\frac{V'_\mathrm{sub} - \varphi_\mathrm{sb}}{t_\mathrm{oxb}}, \tag{13}$$

where $V'_\mathrm{gs} = V_\mathrm{gs} - V_\mathrm{FB}$, $V'_\mathrm{sub} = V_\mathrm{sub} - V_\mathrm{FB}$, V_gs and V_sub are the top and bottom gate voltages, respectively, and ε_ox is the dielectric constant of the oxide. V_FB is the top

and bottom gate flat-band voltage. The flat-band voltage is $V_{FB} = -(kT/q)\ln(N_A/n_i)$ for mid-gap gate material. N_A is the channel doping concentration. The channel is practically undoped ($\approx 10^{15}\,\mathrm{cm}^{-3}$). Using Eqs. 12 and 13, $C_2(x)$ can be obtained and expressed through $\varphi_f(x)$ as

$$C_2(x) = \frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}V'_{sub} - \varphi_f(x)\left[\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right)+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}\right]+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right)V'_{gs}}{(2t_{Si}+\frac{\varepsilon_{ox}t_{Si}^2}{\varepsilon_{Si}t_{oxb}})}. \tag{14}$$

Considering Eq. 11, $a_2(x,z)$ can be expressed as (see Appendix A)

$$a_2(x,z) = \frac{4}{W^2}(\varphi_f(x) - a_0(x,z)). \tag{15}$$

Substituting these coefficients into Eq. 6, the 3-D potential distribution is obtained as

$$\begin{aligned}\varphi(x,y,z) = {} & \varphi_f(x) + \left(\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_f(x)-V'_{gs}}{t_{ox}}\right)z \\ & + \left(\frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}V'_{sub} - \varphi_f(x)\left[\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right)+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}\right]+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right)V'_{gs}}{(2t_{Si}+\frac{\varepsilon_{ox}t_{Si}^2}{\varepsilon_{Si}t_{oxb}})}\right)z^2 \\ & - \frac{4}{W^2}\left(\left(\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_f(x)-V'_{gs}}{t_{ox}}\right)z + \frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}V'_{sub} - \varphi_f(x)\left[\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right)+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}\right]+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right)V'_{gs}}{(2t_{Si}+\frac{\varepsilon_{ox}t_{Si}^2}{\varepsilon_{Si}t_{oxb}})}z^2\right)y^2. \end{aligned} \tag{16}$$

Equation 16 can be written based on $\varphi_f(x)$ as

$$\varphi(x,y,z) = \varphi_f(x)C + D, \tag{17}$$

where

$$C = 1 + k_1 z - k_4 z^2 - k_5 z y^2 + k_8 z^2 y^2, \tag{18}$$

$$D = -k_2 z + k_3 z^2 + k_6 z y^2 - k_7 z^2 y^2. \tag{19}$$

The coefficients $k_1, k_2, \ldots, k_8$ are given in Appendix A.

The differential equation for the surface potential is obtained by inserting Eq. 17 into Eq. 1 to yield

$$\frac{\mathrm{d}^2\varphi_f(x)}{\mathrm{d}x^2} - \alpha\varphi_f(x) = \beta + \frac{qn_i}{C\varepsilon_{Si}}\mathrm{e}^{\frac{q(C\varphi_f(x)+D)}{kT}}, \tag{20}$$

in which

$$\alpha = \frac{2k_5 z - 2k_8 z^2 + 2k_4 - 2k_8 y^2}{1 + k_1 z - k_4 z^2 - k_5 z y^2 + k_8 z^2 y^2}, \tag{21}$$

$$\beta = \frac{-2k_6 z + 2k_7 z^2 - 2k_3 + 2y^2 k_7}{1 + k_1 z - k_4 z^2 - k_5 z y^2 + k_8 z^2 y^2}. \tag{22}$$

Using the first two terms of the Tailor expansion (see Appendix A) for the exponential term in Eqs. 20, one obtains

$$\frac{\mathrm{d}^2\varphi_f(x)}{\mathrm{d}x^2} - \alpha'\varphi_f(x) = \beta', \tag{23}$$

where

$$\beta' = \beta + \frac{qn_i}{C\varepsilon_{Si}} + \frac{q^2 n_i D}{C\varepsilon_{Si}kT}, \tag{24}$$

$$\alpha' = \alpha + \frac{q^2 n_i}{\varepsilon_{Si}kT}. \tag{25}$$

The boundary conditions for solving Eq. 20 can be expressed based on $\varphi_f(x)$ by considering Eqs. 2, 3, and 17:

$$\varphi_f(0) = \frac{V_{bi} - D}{C}, \tag{26}$$

$$\varphi_f(L) = \frac{V_{bi} + V_{DS} - D}{C}. \tag{27}$$

By solving Eq. 20 with the suitable boundary conditions Eqs. 26 and 27, the surface potential is obtained as

$$\varphi_f(x) = -\sigma + M\exp\left(\left(\alpha'\right)^{1/2}x\right) + N\exp\left(-\left(\alpha'\right)^{1/2}x\right), \tag{28}$$

where

$$N = \frac{\frac{V_{bi}+V_{DS}-D}{C} + \sigma - \left(\frac{V_{bi}-D}{C}+\sigma\right)\exp(\Gamma)}{\exp(-\Gamma) - \exp(\Gamma)}, \tag{29}$$

$$M = \frac{V_{bi}-D}{C} + \sigma - \frac{\frac{V_{bi}+V_{DS}-D}{C} + \sigma - \left(\frac{V_{bi}-D}{C}+\sigma\right)\exp(\Gamma)}{\exp(-\Gamma) - \exp(\Gamma)}, \tag{30}$$

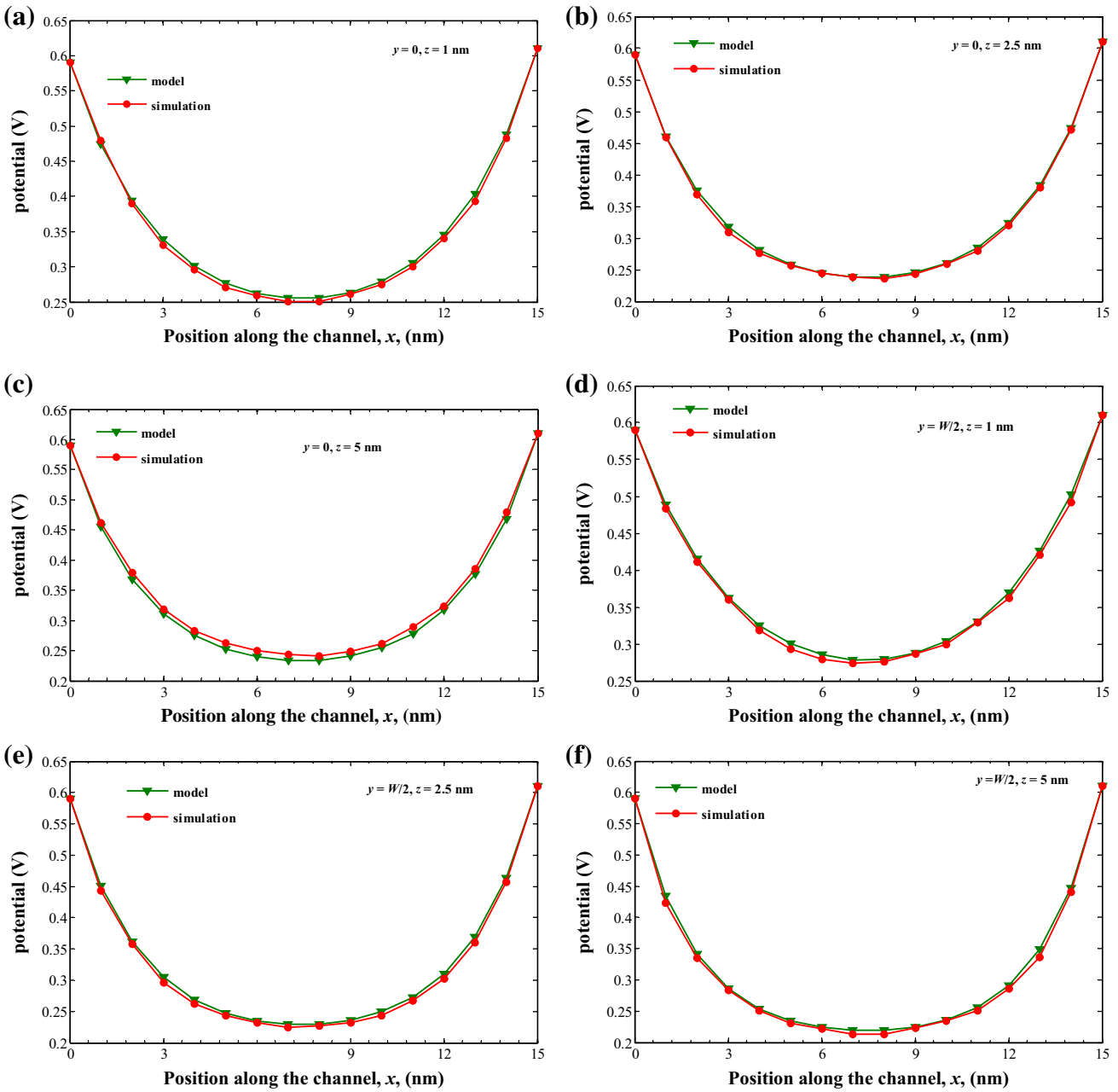

Fig. 2 Potential distribution in a trigate SOI MOSFET with gate, drain, and substrate bias of 0.2, 0.02, and 0 V, respectively. The parameters of the transistor structure are $t_{oxb} = 100\,\text{nm}$, $t_{ox} = 1\,\text{nm}$, $t_{Si} = 5\,\text{nm}$, $W = 5\,\text{nm}$, and $L = 15\,\text{nm}$. The potential is shown at different *cut lines*: **a** $y = 0$, $z = 1\,\text{nm}$; **b** $y = 0$, $z = 2.5\,\text{nm}$; **c** $y = 0$, $z = 5\,\text{nm}$; **d** $y = W/2$, $z = 1\,\text{nm}$; **e** $y = W/2$, $z = 2.5\,\text{nm}$; **f** $y = W/2$, $z = 5\,\text{nm}$

where $\sigma = \beta'/\alpha'$ and $\Gamma = L(\alpha')^{1/2}$. Inserting the surface potential into Eq. 17, the 3-D potential distribution is obtained.

The subthreshold slope depends on the carrier concentration at the minimum potential. So, to derive an analytical model for the subthreshold slope, the location of the minimum potential along the channel, known as the virtual cathode [23], is required. Equation 31 should be solved to find this point along the x-axis.

$$\frac{\mathrm{d}\varphi(x, y, z)}{\mathrm{d}x} = 0. \tag{31}$$

Solving Eq. 31, the position of the minimum potential is derived as

$$x_{\min}(y, z) = \frac{\ln(\frac{N}{M})}{2\sqrt{\alpha'}}. \tag{32}$$

The subthreshold swing (SS) can then be calculated as [27]

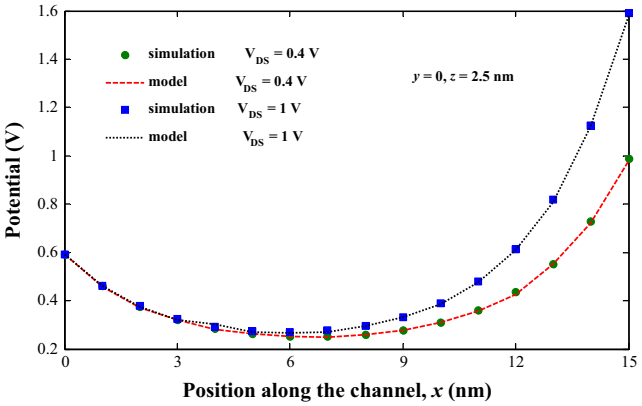

Fig. 3 Potential distribution along the channel at $y = 0$ and $z = 2.5\,\text{nm}$; W, t_{Si}, and L are 5, 5, and 15 nm, respectively. The drain voltage applied is 0.4 and 1 V, and the gate voltage is 0.2 V

$$\text{SS} = \frac{kT}{q}\ln(10)\left[\frac{\mathrm{d}\varphi_{\min}(x,y,z)}{\mathrm{d}V_{\text{gs}}}\right]^{-1}. \tag{33}$$

An analytical model for the subthreshold swing can then be obtained as follows:

$$\frac{\mathrm{d}\varphi(x,y,z)}{\mathrm{d}V_{\text{gs}}} = \frac{\mathrm{d}\varphi_{\text{f}}(x)}{\mathrm{d}V_{\text{gs}}}C + \frac{\mathrm{d}D}{\mathrm{d}V_{\text{gs}}}; \tag{34}$$

$\mathrm{d}\varphi_{\text{f}}(x)/\mathrm{d}V_{\text{gs}}$ and $\mathrm{d}D/\mathrm{d}V_{\text{gs}}$ are calculated in Appendix B.

3 Results and discussion

Figure 2 shows the potential distribution within the channel at different cross-sections, comparing the results obtained from the analytical model with the simulation results. The front gate, back gate (substrate), and drain voltages are 0.2, 0, and 0.02 V, respectively. The channel is undoped (donor concentration $10^{15}\,\text{cm}^{-3}$), the n^+ source and drain are highly doped, and the dimensions of the TG structure are as follows: buried-oxide thickness (t_{oxb}) of 100 nm, gate oxide thickness (t_{ox}) of 1 nm, channel thickness (t_{Si}) of 5 nm, channel width (W) of 5 nm, and channel length (L) of 15 nm, with mid-gap gate material applied. The simulation tool used in this study is Silvaco ATLAS [28]. The analytical model is the classical model in which quantum confinement [29] is neglected. The results of the analytical model were verified by the simulation results with good accuracy.

Figure 3 illustrates the potential distribution along the channel at the position $z = 2.5\,\text{nm}$ ($t_{\text{Si}}/2$) and $y = 0$ ($W/2$) with drain voltage of 0.4 and 1 V and gate voltage of 0.2 V. The results of the analytical model coincide with the simulation results at different drain voltages.

The obtained model is valid for different channel lengths. Figure 4 shows the potential distribution along the channel

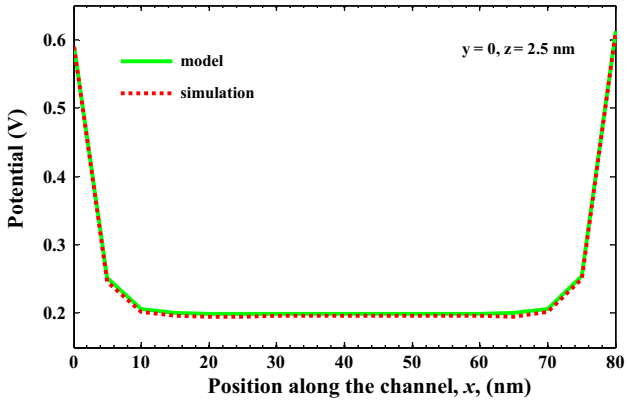

Fig. 4 Potential distribution in a long-channel trigate SOI MOSFET at cut line $y = 0$ and $z = 2.5\,\text{nm}$. The gate, drain, and substrate biases are 0.2, 0.02, and 0 V, respectively. The parameters of the transistor structure are $t_{\text{oxb}} = 100\,\text{nm}$, $t_{\text{ox}} = 1\,\text{nm}$, $t_{\text{Si}} = 5\,\text{nm}$, $W = 5\,\text{nm}$, and $L = 80\,\text{nm}$

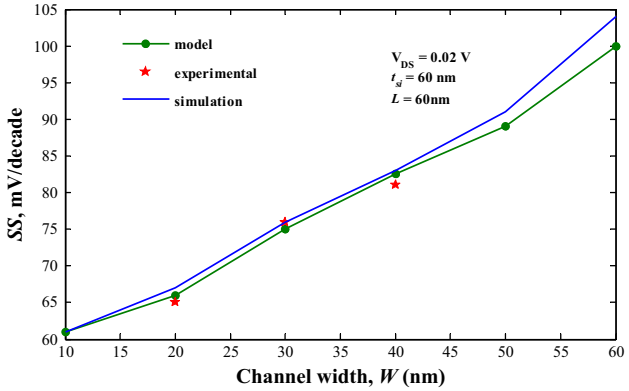

Fig. 5 Relationship between SS and channel width of a TG MOSFET with $t_{\text{Si}} = 60\,\text{nm}$, $L = 60\,\text{nm}$, and $V_{\text{DS}} = 0.02\,\text{V}$

in a trigate MOSFET with $L = 80\,\text{nm}$, $t_{\text{Si}} = 5\,\text{nm}$, and $W = 5\,\text{nm}$, at the cut line $y = 0$, $z = 2.5\,\text{nm}$. The gate and drain voltages are 0.2 and 0.02 V, respectively. A good match between the simulation data and model is observed.

Based on [30], the potential at the center ($y = 0$) is higher compared with anywhere else, like the surface potential ($y = \pm W/2$). Therefore, the center of the channel is a leaky path and y is fixed at zero in Eq. 33.

In the z-direction, because the voltage is applied at the top gate without any bias at the back gate, the conduction path moves toward the top gate [22]. Therefore, in Eq. 33, z is zero, approximately. The results of the simulation, model, and experimental data, extracted from [14], for SS are compared in Fig. 5. The drain voltage V_{DS} is 0.02 V, with $L = 60\,\text{nm}$, $t_{\text{Si}} = 60\,\text{nm}$, and $t_{\text{ox}} = 1.5\,\text{nm}$, to compare with experimental data. With decreasing W, the gate control over the channel increases and the SS is reduced. At $W = 10\,\text{nm}$, the SS approaches the ideal value of $(kT/q)\ln 10$ (about 60 mV/dec at 300 K).

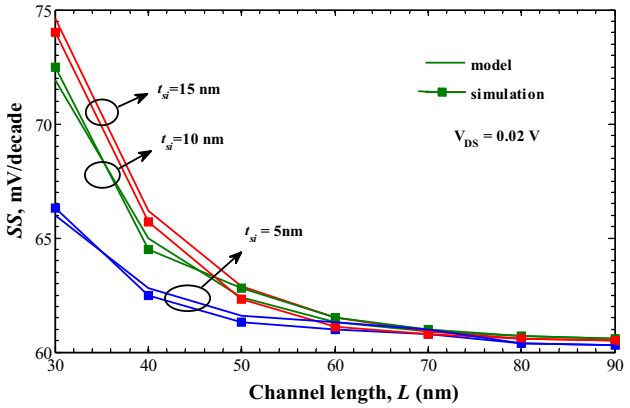

Fig. 6 Variation of SS with channel length L at low drain voltage $V_d = 0.02\,\text{V}$ with $t_{Si} = 5\,\text{nm}$, 10 nm, and 15 nm and $W = 10\,\text{nm}$

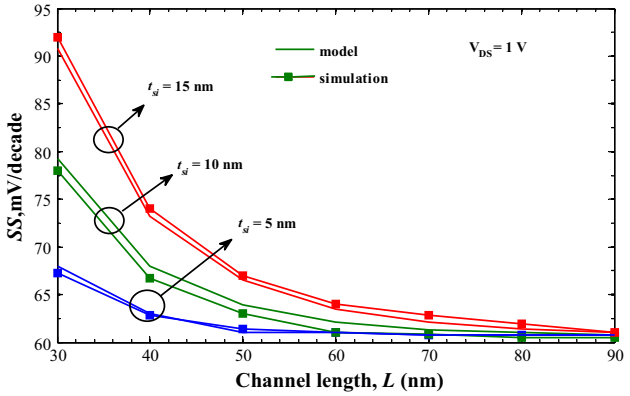

Fig. 7 SS versus L as t_{Si} varies from 5 to 15 nm with V_{DS} of 1 V and channel width of 10 nm

In Fig. 6, the values of SS calculated from the model and simulation are plotted against L for $t_{Si} = 15\,\text{nm}$, $t_{Si} = 10\,\text{nm}$, and $t_{Si} = 5\,\text{nm}$. With decrease of the channel length, L, due to increasing short-channel effects, the SS increases. In addition, changing the channel thickness, t_{Si}, affects the SS, whereas increasing t_{Si} causes the gate to lose control over the channel, so the SS increases.

Figure 7 presents plots of the SS of a TG SOI MOSFET with $W = 10\,\text{nm}$ for different channel lengths, calculated at $V_{DS} = 1\,\text{V}$ using the analytical model in Eq. 33 (continuous lines) or numerical calculations (symbols). At high drain voltage, the conduction path in the z-direction is closer to the gate oxide and silicon interface compared with low drain voltage [22]. In this figure the conduction path is about 1 % of the silicon thickness, t_{Si}, whereas at low voltages, it is about 5 % of t_{Si} at high drain voltage. The good agreement between the analytical and numerical values of SS demonstrates the validity of the presented model.

4 Conclusions

Assuming a parabolic potential distribution between the two lateral gates and solving the 3-D Poisson's equation, an analytical model for the potential distribution in a nanoscale undoped trigate SOI MOSFET is obtained. The model offers good accuracy to predict the potential distribution through the transistor body. By applying the 3-D potential model and considering the conduction path, an analytical model for the subthreshold swing is derived. The presented model is verified by simulation and measurement data.

Appendix A

Potential distribution

(a.1) C_2 coefficient:

$$C_0(x) = \varphi_f(x), \tag{35}$$

$$C_1(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\varphi_f(x) - V'_{gs}}{t_{ox}}, \tag{36}$$

$$\varphi_{sb}(x) = C_0(x) + C_1(x)t_{Si} + C_2(x)t_{Si}^2, \tag{37}$$

$$C_1(x) + 2C_2(x)t_{Si} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{sub} - \varphi_{sb}}{t_{oxb}}. \tag{38}$$

Inserting (35), (36), and (37) into (38), the coefficient C_2 is obtained as a function of $\varphi_f(x)$ as follows:

$$C_1(x) + 2C_2(x)t_{Si} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}(V'_{sub} - \varphi_f(x) + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}(\varphi_f(x) - V'_{gs}) + t_{Si}^2 C_2(x)). \tag{39}$$

(a.2) $a_2(x, z)$:

Using Eq. 7 in Eq. 15, a_2 is obtained as

$$a_2(x,z) = \left(\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\varphi_f(x) - V'_{gs}}{t_{ox}}\right) z + \frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}} V'_{sub} - \varphi_f(x)\left[\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1 + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right) + \frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{oxb}}\right] + \frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\left(1 + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{oxb}}\right) V'_{gs}}{(2t_{Si} + \frac{\varepsilon_{ox}t_{Si}^2}{\varepsilon_{Si}t_{oxb}})} z^2. \tag{40}$$

(a.3) Coefficients $k_1, k_2, \ldots, k_8$

The coefficients $k_1, k_2, \ldots, k_8$ are as follows:

$$k_1 = \frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}, \tag{41}$$

$$k_2 = \frac{\varepsilon_{ox} V'_{gs}}{\varepsilon_{Si} t_{ox}}, \tag{42}$$

$$k_3 = \frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{oxb}} V'_{sub} + \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{oxb}}\right) V'_{gs}}{(2t_{Si} + \frac{\varepsilon_{ox} t_{Si}^2}{\varepsilon_{Si} t_{oxb}})}, \tag{43}$$

$$k_4 = \frac{\left[\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{oxb}}\right) + \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{oxb}}\right]}{(2t_{Si} + \frac{\varepsilon_{ox} t_{Si}^2}{\varepsilon_{Si} t_{oxb}})}, \tag{44}$$

$$k_5 = \frac{4\varepsilon_{ox}}{W^2 \varepsilon_{Si} t_{ox}}, \tag{45}$$

$$k_6 = \frac{4\varepsilon_{ox} V'_{gs}}{W^2 \varepsilon_{Si} t_{ox}}, \tag{46}$$

$$k_7 = \frac{4}{W^2} \frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{oxb}} V'_{sub} + \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{oxb}}\right) V'_{gs}}{(2t_{Si} + \frac{\varepsilon_{ox} t_{Si}^2}{\varepsilon_{Si} t_{oxb}})}, \tag{47}$$

$$k_8 = \frac{4}{W^2} \frac{\left[\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{oxb}}\right) + \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{oxb}}\right]}{(2t_{Si} + \frac{\varepsilon_{ox} t_{Si}^2}{\varepsilon_{Si} t_{oxb}})}. \tag{48}$$

(a.4) Tailor expansion

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots \tag{49}$$

The Tailor expansion of the exponential term in Eq. 20 is as follows:

$$e^{\frac{q(C\varphi_f(x)+D)}{kT}} = 1 + \frac{q(C\varphi_f(x) + D)}{kT}. \tag{50}$$

Appendix B

Subthreshold swing

$$\frac{d\varphi_f}{dV_{gs}} = \frac{dM}{dV_{gs}} \exp((\alpha')^{1/2} x) + \frac{dN}{dV_{gs}} \exp(-((\alpha')^{1/2} x)) - \frac{d\beta'/dV_{gs}}{\alpha'}, \tag{51}$$

where

$$\frac{dM}{dV_{gs}} = \frac{-dD/dV_{gs}}{C} + \frac{d\beta'/dV_{gs}}{\alpha'} - \frac{\frac{-dD/dV_{gs}}{C} + \frac{d\beta'/dV_{gs}}{\alpha'} - (\frac{-dD/dV_{gs}}{C} + \frac{d\beta'/dV_{gs}}{\alpha'}) \exp(\Gamma)}{\exp(-\Gamma) - \exp(\Gamma)}, \tag{52}$$

$$\frac{dN}{dV_{gs}} = \frac{\frac{-dD/dV_{gs}}{C} + \frac{d\beta'/dV_{gs}}{\alpha'} - (\frac{-dD/dV_{gs}}{C} + \frac{d\beta'/dV_{gs}}{\alpha'}) \exp(\Gamma)}{\exp(-\Gamma) - \exp(\Gamma)}, \tag{53}$$

$$\frac{d\beta'}{dV_{gs}} = \frac{\frac{8}{W^2}(-k_1 z + k_9 z^2) - 2k_9 + \frac{8}{W^2} y^2 k_9}{1 + k_1 z - k_4 z^2 - k_5 z y^2 + k_8 z^2 y^2} + \frac{dD}{dV_{gs}} \frac{q^2 n_i}{C\varepsilon_{Si} kT}, \tag{54}$$

$$k_9 = \frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{oxb}}\right)}{(2t_{Si} + \frac{\varepsilon_{ox} t_{Si}^2}{\varepsilon_{Si} t_{oxb}})}, \tag{55}$$

$$\frac{dD}{dV_{gs}} = -k_1 z + k_9 z^2 + k_5 z y^2 - \frac{4}{W^2} k_9 z^2 y^2. \tag{56}$$

References

1. Iwai, H.: Roadmap for 22 nm and beyond. Microelectron. Eng. **86**, 1520–1528 (2009)
2. Collaert, N., De Keersgieter, A., Dixit, A., Ferain, I., Lai, L.-S., Lenoble, D., Mercha, A., Nackaerts, A., Wong, H.-S.P., Boeuf, F.:Multi-gate devices for the 32 nm technology node and beyond. In: Solid-State Device Research Conference, pp. 143–146 (2007)
3. Lemnios, Z.J., Radack, D.J., Zolper, J.C.:The future of silicon-on-insulator (SOI) technology in microelectronic systems. In: Proceedings of the International SOI Conference, pp. 9–13 (2004)
4. Cristoloveanu, S., Ferlet-Cavrois, V.: Introduction to SOI MOSFETs: Context, radiation effects, and future trends. Int. J. High Speed Electron. Syst. **14**(2), 465–487 (2004)
5. Ortiz-Conde, A., García-Sánchez, F. J.:Multi-gate 3-D SOI MOSFETs as the mainstream technology in high speed CMOS applications. In: Proceedings of the 11th IEEE International Symposium on EDMO, pp. 115–121 (2003)
6. Colinge, J.P.: FinFETs and Other Multi-Gate MOSFETs. Springer, Berlin (2008)
7. Son, A., Kim, J., Jeong, N., Choi, J., Shin, H.: Improved explicit current-voltage model for long-channel undoped surrounding-gate metal oxide semiconductor field effect transistor. J. Appl. Phys. **48**, 412–413 (2009)
8. Frank, D.J., Dennard, R.H., Nowak, E., Solomon, P.M., Taur, Y., Wong, H.-S.P.: Device scaling limits of Si MOSFETs and their application dependencies. Proc. IEEE **89**(3), 259–288 (2001)
9. Doyle, B., Arghavani, R., Barlage, D., Datta, S., Doczy, M., Kavalieros, J., Murthy, A., Chau, R.: Transistor elements for 30 nm physical gate lengths and beyond. Intel Technol. J. **6**(2), 42–54 (2002)
10. Fossum, J.G., Trivedi, V. P., Wu, K.: Extremely scaled fully depleted SOI CMOS. In: Proceedings of the IEEE International SOI Conference, pp. 135–136 (2002)
11. Fossum, J.G.: Physical insights on nanoscale multi-gate CMOS design. Solid State Electron. **51**(2), 188–194 (2007)
12. Tsormpatzoglou, A., Tassis, D.H., Dimitriadis, C.A., Ghibaudo, G., Collaert, N., Pananakakis, G.: Analytical threshold voltage model for lightly doped short-channel tri-gate MOSFETs. Solid State Electron. **57**(1), 31–34 (2011)
13. Kloes, A., Weidemann, M., Iniguez, B.: Analytical 3D approach for modeling the electrostatic potential in triple-gate SOI MOSFETs. In: Proceedings of the IEEE Conference on Electron Devices Solid-State Circuits EDSSC, pp. 103–106 (2007)
14. Ferain, I., Colinge, C., Colinge, J.: Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. Nature **479**(7373), 310–316 (2011)
15. Colinge, J.: Multiple-gate SOI MOSFETs. Solid State Electron. **48**(6), 897–905 (2004)

16. Cartwright, J.: Intel enters the third dimension. Nature. (2011). doi:10.1038/news.2011.274. http://www.nature.com/news/2011/110506/full/news.2011.274.html
17. Ghani, T., Mistry, K., Packan, P., Thompson, S., Stettler, M., Tyagi, S., Bohr, M.: Scaling challenges and device design requirements for high performance sub 50 nm gate length planar CMOS transistors. In: VLSI Symposium on Digest of Technical Papers, pp. 174–175 (2000)
18. Pao, H.C., Sah, C.T.: Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors. Solid State Electron. **9**(10), 927–937 (1966)
19. Yu, B., Song, J., Yuan, Y., Lu, W., Taur, Y.: A unified analytic drain-current model for multiple-gate MOSFETs. IEEE Trans. Electron Devices **55**(8), 2157–2163 (2008)
20. Duarte, Sung-Jin Choi, J.P., Moon, Dong-Il, Ahn, Jae-Hyuk: A universal core model for multiple-gate field-effect transistors. Part I: charge model. IEEE Trans. Electron Devices **60**(2), 840–848 (2013)
21. Duarte, Sung-Jin Choi, J.P., Moon, Dong-Il, Ahn, Jae-Hyuk: A universal core model for multiple-gate field-effect transistors. Part II: Drain current model. IEEE Trans. Electron Devices **60**(2), 848–854 (2013)
22. Tsormpatzoglou, A., Dimitriadis, C., Clerc, R., Pananakakis, G., Ghibaudo, G.: Semianalytical modeling of short-channel effects in lightly doped silicon trigate MOSFETs. IEEE Trans. Electron Devices **55**(10), 2623–2631 (2008)
23. Abd El Hamid, H., Guitart, J.R., Kilchytska, V., Flandre, D., Iniguez, B.: A 3-D analytical physically based model for the sub-threshold swing in undoped trigate FinFETs. IEEE Trans. Electron Devices **54**(9), 2487–2496 (2007)
24. Akarvardar, K., Mercha, A., Cristoloveanu, S., Gentil, P., Simoen, E., Subramanian, V., Claeys, C.: A two-dimensional model for interface coupling in triple-gate transistors. IEEE Trans. Electron Devices **54**(4), 767–775 (2007)
25. Sun, Xin, Liu, Tsu-Jae King: Scale-length assessment of the trigate. IEEE Trans. Electron Devices **56**(11), 2840–2842 (2009)
26. Young, K.K.: Short-channel effect in fully-depleted SOI MOSFETs. IEEE Trans. Electron Devices **36**(2), 399–402 (1989)
27. Tsormpatzoglou, A., Dimitriadis, C.A., Clerc, R., Rafhay, Q., Pananakakis, G., Ghibaudo, G.: Semi-analytical modeling of short-channel effects in Si and Ge symmetrical double-gate MOSFETs. IEEE Trans. Electron Devices **54**(8), 1943–1952 (2007)
28. Atlas User's Manual, Device Simulation Software, software version, **5**, Silvaco, Santa Clara (2008)
29. Vimala, P., Balamurugan, B.: Analytical model for nanoscale tri-gate SOI MOSFETs including quantum effects. IEEE Trans. Electron Devices **2**(1), 1–7 (2014)
30. Tosaka, Y., Suzuki, K., Sugii, T.: Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET's. IEEE Electron Device Lett. **15**(11), 466–468 (1994)