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A silicon doped hafnium oxide ferroelectric p–n–p–n SOI tunneling field–effect transistor with steep subthreshold slope and high switching state current ratio

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In this paper, a silicon–on–insulator (SOI) p–n–p–n tunneling field–effect transistor (TFET) with a silicon doped hafnium oxide (Si:HfO2) ferroelectric gate stack is proposed and investigated via 2D device simulation with a calibrated nonlocal band–to–band tunneling model. Utilization of Si:HfO2 instead of conventional perovskite ferroelectrics such as lead zirconium titanate (PbZrTiO3) and strontium bismuth tantalate (SrBi2Ta2O9) provides compatibility to the CMOS process as well as improved device scalability. By using Si:HfO2 ferroelectric gate stack, the applied gate voltage is effectively amplified that causes increased electric field at the tunneling junction and reduced tunneling barrier width. Compared with the conventional p–n–p–n SOI TFET, the on–state current and switching state current ratio are appreciably increased; and the average subthreshold slope (SS) is effectively reduced. The simulation results of Si:HfO2 ferroelectric p–n–p–n SOI TFET show significant improvement in transconductance (~9.8X enhancement) at high overdrive voltage and average subthreshold slope (~35% enhancement over nine decades of drain current) at room temperature, indicating that this device is a promising candidate to strengthen the performance of p–n–p–n and conventional TFET for a switching performance. © 2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). [http://dx.doi.org/10.1063/1.4962969]

Incessant downscaling in the metal oxide semiconductor (CMOS) device is facing critical issues such as leakage current, short–channel effects (SCEs) and high power consumption. Tunneling field–effect transistors (TFETs) are of interest as an alternative transistor design for future ultralow voltage domain because of their low off–state leakage current (Ioff) and low subthreshold slope (SS). Since current are controlled by the band–to–band tunneling (BTBT) mechanism on the source–channel interface, TFETs can achieve subthreshold slope less than 60 mV/decade at room temperature, which allows for a more aggressive reduction of the threshold and supply voltages.1–4 However, planar silicon–based TFETs have very low on–state current (Ion) compared to the conventional MOSFETs (typically 3–5 decades) due to poor band–to–band tunneling efficiency, which is a serious drawback in the circuit applications. In order to improve on–state current of TFETs, several techniques have been adopted such as heterostructures,3 band–gap engineering,5 low band–gap and high mobility materials,6 multiple gate,7 vertical direction tunneling,8 extended source,9 source–pocket doping (p–n–p–n)10 and ferroelectric gate stack.11–13 The integration14 and scaling issues15 are biggest challenges for further utilization of conventional perovskite ferroelectrics such as lead zirconium titanate (PbZrTiO3) and strontium bismuth tantalate (SrBi2Ta2O9). Recently, the ferroelectric behaviour of HfO2–based thin films are known.16 The discovered ferroelectric properties of HfO2 dielectrics yield the

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potential to overcome these limitations renewed the interest in ferroelectric field effect transistors (FeFET). The main advantage the silicon doped hafnium oxide (Si:HfO$_2$) ferroelectric is its full compatibility with the standard CMOS process and improved scaling potential even nanometre range (5–30 nm). The gate stack height of Si:HfO$_2$ devices can be extremely reduced because of a significantly lower dielectric constant of ~25 (for conventional perovskite ferroelectrics ~200–300) and significantly higher coercive field strength of ~1 MV/cm (for conventional perovskite ferroelectrics ~50 kV/cm). Therefore, it causes gate stack aspect ratios more suitable for scaling. Although there have been reports on the design and fabrication of ferroelectric PbZrTiO$_3$ gate stack TFETs, p–n–p–n SOI TFET with the Si:HfO$_2$ ferroelectric gate stack has not been reported yet.

It is worth mentioning that the negative capacitance (NC) can be understood in terms of simple positive feedback loop, where a simple capacitive ($C_D$) with a feedback factor ($\alpha_f$). Therefore, the effective charge ($Q$) stored in the system for an applied voltage ($V$) is given by:

$$Q = \left( \frac{C_0}{1 - \alpha_f C_0} \right) V$$

where $C_{eff}$ is the effective capacitance. It becomes negative when the feedback is strong enough such that $\alpha_f C_0 > 1$ that is normally unstable but is effectively stabilized when placed in series with normal capacitors. Therefore, by putting semiconductor ($C_s$) and insulator ($C_{ins}$) capacitors in series with ferroelectric capacitor ($C_{ferro}$), the body factor (for the capacitive coupling between the gate and channel) can be expressed based on the equivalent capacitance model of the ferroelectric-insulator-semiconductor gate stack structure as:

$$\frac{\partial V_S}{\partial \psi_s} = 1 + \frac{C_s}{C_{ferro} + C_{ins}}$$

The $C_{ferro}$ is effectively a negative capacitor because the slope of the polarization versus electric field is negative around the origin of coordinates. Therefore, negative capacitance effect of ferroelectric layer is beneficial for body factor that will be less than unity.

In this paper, the integration of coupling the Si:HfO$_2$ ferroelectric is applied to p–n–p–n SOI TFETs in order to further improve the performance. The ferroelectric gate stack results negative capacitance effect which is beneficial for energy band bending and assists in the BTBT probability enhancement and reduction in tunneling barrier width due to the applied gate voltage amplification. Results indicate that it can achieve much steeper subthreshold slope (~37.7 mV/decade) and around 1 orders of magnitude higher on–state current while maintaining off–state current compared with p–n–p–n SOI TFET.

The cross–sectional views of the conventional and Si:HfO$_2$–based metal–ferroelectric–insulator–semiconductor SOI p–n–p–n tunneling field–effect transistor (MFIS–SOI p–n–p–n TFET) with a poly–Si/TiN/SiHfO$_2$/interface oxide/Si gate stack structure are shown in Fig. 1. The device parameters for conventional SOI p–n–p–n TFET, used in this study, are similar to that defined in Ref. 24 and are as follows: source doping concentration $N_A = 1 \times 10^{20}$ cm$^{-3}$, drain doping concentration $N_D = 1 \times 10^{18}$ cm$^{-3}$, channel doping concentration $N_A = 1 \times 10^{16}$ cm$^{-3}$, silicon film thickness ($t_{Si}$) = 15 nm and channel length ($L_{ch}$) = 27 nm. The n–type source–pocket doping concentration is $1 \times 10^{19}$ cm$^{-3}$ with width ($W$) of 3 nm in order to remain fully depleted for proper working of p–n–p–n TFET. Titanium nitride (TiN) was used as a gate electrode to reduce gate depletion effect and resistance. The device parameters of MFIS–SOI p–n–p–n TFET are same as given above except that the 30 nm thick Si:HfO$_2$ served as the ferroelectric layer. The interfacial buffer layer embedded between the silicon film and the ferroelectric layer is SiO$_2$ with permittivity of $\varepsilon = 3.9 \varepsilon_0$, which reduced the effective voltage drop over the ferroelectric layer. The fabrication process steps of such gate stack are similar to that described for fabricated Si:HfO$_2$–based FeFET in Ref. 28.

Two–dimensional device simulations are done using the Silvaco ATLAS device simulator. For achieving the high accuracy, the band–to–band tunneling model based on a nonlocal path tunneling
approach was used for all simulations. It is worth noting that the nonlocal band–to–band tunneling model is calibrated to the experimentally measured results by tuning the effective electron and hole masses as done in our earlier works.\textsuperscript{9,10,24} The Auger recombination, band–gap narrowing and Shockley–Read–Hall (SRH) recombination models were also included to describe the recombination, generation and carriers’ lifetimes in the highly doped regions. Meanwhile, the concentration and field dependent mobility models and trap–assisted–tunneling models were also used.\textsuperscript{10,24} In order to model the ferroelectric effects, the ferroelectric permittivity model has been implemented and in this way the permittivity used in Poisson’s Equation is given the following functional form:\textsuperscript{29}

\[
\varepsilon(E) = \varepsilon_{\text{ferro}} \cdot \frac{\varepsilon_{\text{ps}}}{2\delta} \cdot \sec h^2 \left( \frac{E - \varepsilon_{\text{ec}}}{2\delta} \right)
\]  (3)
where \( E \) is the electric field, \( \text{ferro.epsf} \) is the permittivity, \( \text{ferro.ps} \) is the saturation polarization, \( \text{ferro.ec} \) is the coercive field and \( \delta \) is given by:

\[
\delta = \text{ferro.ec} \left[ \log \left( \frac{1 + \frac{\text{ferro.pr}}{\text{ferro.ps}}}{1 - \frac{\text{ferro.pr}}{\text{ferro.ps}}} \right) \right]^{-1}
\]  

(4)

where \( \text{ferro.pr} \) is the remnant polarization. The values of the \( \text{ferro.epsf} \), \( \text{ferro.ps} \), \( \text{ferro.pr} \) and \( \text{ferro.ec} \) parameters for 30 nm thick Si:HfO\(_2\) are 25, \( 2.005 \times 10^{-6} \) C/cm\(^2\), \( 2 \times 10^{-6} \) C/cm\(^2\) and \( 0.9 \times 10^5 \) V/cm, respectively.\(^{16,21}\)

Figure 2 (a) shows the overdrive voltage (\( V_{\text{GS}}-V_{\text{TH}} \), where \( V_{\text{TH}} \) is the threshold voltage) dependent drain current (\( I_{\text{DS}} \)) for MFIS and conventional SOI p–n–p–n TFETs with gate length of 30 nm biased at \( V_{\text{DS}} = 1 \) V. In order to much better analysis and comparison of the performance parameters, the subthreshold slope was defined as the average slope between the off–state current and threshold current as below:\(^2,30\)

\[
SS = \frac{V_{\text{th}} - V_{\text{off}}}{\log \frac{I_{\text{th}}}{I_{\text{off}}}}
\]  

(5)

where \( V_{\text{th}} \) is the threshold voltage and defined here by the constant current method at the point of \( I_{\text{DS}} = 1.5 \times 10^{-9} \) A/\( \mu \)m, \( I_{\text{off}} \) is defined to be the drain current at onset \( V_{\text{GS}} \), while \( I_{\text{on}} \) is defined at

![Image](https://example.com/image.png)

**FIG. 2.** The overdrive voltage (\( V_{\text{OV}} \)) dependence of (a) drain current in linear and logarithm scales and (b) transconductance for the MFIS and conventional SOI p–n–p–n TFETs with gate length of 30 nm at \( V_{\text{DS}} = 1 \) V.
$V_{GS} = V_{off} + 1$ V and $V_{DS} = 1$ V. These definitions are used in the rest of this paper. It can be seen that by introducing Si:HfO$_2$ ferroelectric layer, MFIS SOI p–n–p–n TFETs have a higher on–state current around 1 decade ($1.61 \times 10^{-6}$ and $1.05 \times 10^{-7}$ A/μm for MFIS and conventional SOI p–n–p–n TFETs, respectively) while maintaining off–state current, resulting in higher switching state current ratio of $\sim 7.32 \times 10^{11}$ as compared to conventional SOI p–n–p–n TFETs ($6.48 \times 10^{10}$). Because the applied gate voltage is effectively amplified by negative capacitance effect of Si:HfO$_2$ ferroelectric layer with high permittivity, the band bending at the tunneling junction becomes so steep, which significantly reduced the tunneling barrier width. Therefore, the MFIS SOI p–n–p–n TFETs have a higher drain current due to the increased tunneling probability. In addition, smaller SS of 37.7 mV/decade can be achieved in the MFIS SOI p–n–p–n TFET in comparison with that of conventional SOI p–n–p–n TFET (58.5 mV/decade) because of increased effective BTBT probability. In Fig. 2 (b), a comparison is made between the transconductances ($g_m$) of the MFIS and conventional SOI p–n–p–n TFETs as a function of the overdrive voltage ($V_{OV}$). As seen, the conductance of MFIS SOI p–n–p–n TFET increased by 880% (~9.8X enhancement) at high $V_{OV}$ compared to that of the conventional SOI p–n–p–n TFETs because it has a higher on–state current.

In order to achieve better performance, we optimize the Si:HfO$_2$ ferroelectric thickness ($t_{ferro}$). Five different values of $t_{ferro}$, as 5, 10, 15, 20, and 25 nm, are used for this purpose. Table I summarize the extracted ferroelectric and device performance parameters of the MFIS SOI p–n–p–n TFET with varying $t_{ferro}$ biased at $V_{DS} = 1$ V. Because the ferroelectric permittivity of Si:HfO$_2$ increased by decreasing the ferroelectric thickness, the on–state current and switching state current ratio is appreciably increased. On the other hand, devices with thinner layer of Si:HfO$_2$ ferroelectric have steeper SS because of higher effective BTBT probability due to steeper band bending at the source–channel interface. As can be observed from Table I, the SS values decreased from 37.01 mV/decade to about 23.51 mV/decade as the ferroelectric layer thickness was decreased from 25 nm to 5 nm, respectively. In the optimized condition, the SS decreased by 60%, and the on–state current enhanced by around two orders of magnitude compared to those of the conventional SOI p–n–p–n TFET. The most important advantage of using thinner layer of Si:HfO$_2$ ferroelectric is the possibility of overcoming the scaling limitations of conventional perovskite ferroelectrics and then it is suitable for ultralow power applications.

In order to investigate whether the Si:HfO$_2$ ferroelectric effect was present when the feature size of the devices decreased, the performances of the MFIS SOI p–n–p–n TFET with different gate lengths were also examined. Except gate length, all parameters are kept as same in these simulations. The Si:HfO$_2$ ferroelectric thickness is 5 nm. Figure 3 (a) shows the performance comparison of the on–state and off–state currents as a function of gate length at $V_{DS} = 1$ V. It is evident that the tunneling from source to drain regions increases as the gate length decreases from 90 to 15 nm, whereas variation in off–state current is the dominant. This can be explained based on the fact short-channel effects such as DIBL and charge sharing play a dominant role as gate length scale down. Therefore, off–state current increases significantly. Figure 3 (b) shows the plot for switching state current ratio and subthreshold slope as a function of different gate length. Since off–state current increases with scaling down of gate length, switching state current ratio decreases and subthreshold slope degrades, as observed in Fig. 3 (b).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$t_{ferro} = 5$ nm</th>
<th>$t_{ferro} = 10$ nm</th>
<th>$t_{ferro} = 15$ nm</th>
<th>$t_{ferro} = 20$ nm</th>
<th>$t_{ferro} = 25$ nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>ferro.epsf</td>
<td>33.75</td>
<td>32</td>
<td>30.25</td>
<td>28.5</td>
<td>26.75</td>
</tr>
<tr>
<td>ferro.ps (C/cm$^2$)</td>
<td>11.37</td>
<td>9.5</td>
<td>7.63</td>
<td>5.75</td>
<td>3.88</td>
</tr>
<tr>
<td>ferro.pr (C/cm$^2$)</td>
<td>10.75</td>
<td>9</td>
<td>7.25</td>
<td>5.5</td>
<td>3.75</td>
</tr>
<tr>
<td>ferro.ec (V/cm)</td>
<td>1.15</td>
<td>1.1</td>
<td>1.05</td>
<td>1</td>
<td>0.95</td>
</tr>
<tr>
<td>I$_{on}$ (A/μm)</td>
<td>$2.28 \times 10^{-5}$</td>
<td>$1.08 \times 10^{-5}$</td>
<td>$9.28 \times 10^{-6}$</td>
<td>$4.65 \times 10^{-6}$</td>
<td>$2.26 \times 10^{-6}$</td>
</tr>
<tr>
<td>I$_{off}$ (A/μm)</td>
<td>$3.84 \times 10^{-18}$</td>
<td>$3.57 \times 10^{-18}$</td>
<td>$3.30 \times 10^{-18}$</td>
<td>$3.01 \times 10^{-18}$</td>
<td>$2.77 \times 10^{-18}$</td>
</tr>
<tr>
<td>I$<em>{on}$/I$</em>{off}$</td>
<td>$5.94 \times 10^{12}$</td>
<td>$3.03 \times 10^{12}$</td>
<td>$2.81 \times 10^{12}$</td>
<td>$1.54 \times 10^{12}$</td>
<td>$8.16 \times 10^{11}$</td>
</tr>
<tr>
<td>SS (mV/decade)</td>
<td>23.51</td>
<td>25.06</td>
<td>28.99</td>
<td>35.81</td>
<td>37.01</td>
</tr>
</tbody>
</table>
FIG. 3. (a) on–state and off–state currents and (b) switching state current ratio and subthreshold slope for a MFIS and conventional SOI p–n–p–n TFETs with gate length varying from 15 to 90 nm at $V_{DS} = 1$ V.

To summarize, using 2D device simulation with calibrated nonlocal band–to–band tunneling model, a SOI p–n–p–n TFET with a Si:HfO$_2$ ferroelectric gate stack is proposed and analyzed in this paper. The results show that the MFIS SOI p–n–p–n TFET offer important advantages over conventional SOI p–n–p–n TFET in terms of increased on–state current, transconductance and switching state current ratio; and steeper average subthreshold slope. These improved performances are mainly because of the increase in band bending at the tunneling junction induced by the NC effect of Si:HfO$_2$ ferroelectric layer with high permittivity, which increased the BTBT probability and led to an abrupt switching behavior. The transfer characteristics affected by Si:HfO$_2$ ferroelectric thickness were also evaluated. By optimizing ferroelectric layer thickness, the SS is decreased by 60% compared to that of the conventional SOI p–n–p–n TFET. In this way, the on–state current and $g_m$ is enhanced by two orders of magnitude and $\sim 56.6X$, respectively. The MFIS SOI p–n–p–n TFET is expected to be a suitable candidate to overcome the main challenges of perovskite-type ferroelectrics for the state-of-the-art technology nodes of ultralow power devices.

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9 S. Marjani and S. E. Hosseini, Superlattices and Microstructures 76, 297 (2014).
14 S. Marjani and S. E. Hosseini, Superlattices and Microstructures 76, 297 (2014).
18 S. Marjani and S. E. Hosseini, Superlattices and Microstructures 76, 297 (2014).